CROSSTALK NOISE REDUCTION USING DRIVER SIZING OPTIMIZATION IN VLSI RC GLOBAL INTERCONNECTS USING 90NM PROCESS TECHNOLOGY

[1]Vikas Maheshwari, [2]Anushree

[1]*Deptt. Of ECE, Amity School of Engineering & Technology, Amity University Madhya-Pradesh, Gwalior, M.P., INDIA*
[2]*Deptt. of ECE, Hindustan College of Science and Technology, Mathura, U.P., INDIA*
[1]*maheshhhwarivikas1982@gmail.com, [2]anushree.ece@gmail.com*

ABSTRACT

In this paper noise avoidance in closed form crosstalk noise model for on-chip VLSI RC interconnects using 2π model is presented. In this crosstalk noise model we consider the case when step input is applied to the aggressor which is adjacent to the victim net and further simplified it, then find out the closed form formulae for noise pulse width and noise amplitude for RC interconnect. Various noise avoidance approaches can be used for crosstalk noise reduction. This paper presents crosstalk noise reduction using driver sizing optimization. Sensitivity expressions of driver resistance to peak noise and noise width are used in this work.

Keywords- Noise Modelling, Crosstalk, On-Chip RC Interconnect, Step Input, VLSI.

I. INTRODUCTION

Due to the advancement in VLSI technology feature size is reduced which affects the crosstalk noise problem and also affects the design's timing and functionality goals [1-2]. As a result of this chip area is reduced which degrades the performance of VLSI circuits such as logic failure, unwanted coupling voltage between two adjacent wires, timing delay etc. Decreasing feature size also increases crosstalk noise which is produced due to the parasitic coupling between interconnects. The amount of this crosstalk noise can be calculated by using circuit and layout techniques [3]. Coupling capacitance is high; it is the sum of area capacitance and the fringing capacitances of a wire. According to the trends, the role of this coupling capacitance will be more dominant in the future as feature sizes shrink. Due to this coupling capacitance crosstalk noise is induced in the circuit, which reduces the performance and reliability of the circuit. This may also induce unwanted voltage spikes in neighboring nets. An aggressor net is physically adjacent to a victim net and may be modeled as being connected with the help of a distributed coupling capacitance.

In the current technology, noise analysis and avoidance are becoming equally important or in some cases, more important than the timing and power analysis. Crosstalk noise exhibits a negative impact on the reliability of the VLSI circuits. In these circuits, it is very common to have wires running adjacent to another known as aggressor and victim

nets. The net on which noise is being induced is called the victim net; whereas, the net that induces this noise is called the aggressor net. In deep submicron design, the parasitic coupling effects become significant due to the greater proximity of adjacent wires and the increase in the switching speeds of the signals. Hence it has become necessary to consider the crosstalk between parallel RC interconnects lines [4]. Crosstalk is a well-known phenomenon in integrated circuit design. Crosstalk noise may cause various undesirable effects such as overshooting, undershooting, glitches, increasing and reducing a signal delay. In [5-6] various telegraph equations are directly solved and an analytical formula for peak noise in capacitively coupled bus lines is obtained. The work in [7] derives bounds for crosstalk noise using a lumped RC model, but it assumes a step input for aggressor. Extensions to [7] are made in [8-10] to consider a saturated ramp input and π-circuit to represent the distributed nature of on-chip VLSI interconnect. But most of these models fail to represent the distributed nature of an RC network. The model proposed in [11] considers an Elmore delay like peak noise model for general RC trees but it assumed an infinite ramp input. The peak noise obtained in [11] may even be larger than the supply voltage. Devgan's metric

has been improved in [12]. One recent work shown in [10] is capable to handle distributed RC network and saturated ramp input. In [13-14], an improved 2-π model is introduced which considers the coupling location at victim net and distributed RC characteristics for victim net. In [15] a improved 2-π model of ramp input for crosstalk noise in time domain is derived then various noise reduction techniques are explained. This paper presents idea about crosstalk noise reduction using sensitivity expressions to driver resistance. This technique is known as driver sizing. Some crosstalk reduction techniques are also discussed in [16-19] for RC VLSI Interconnections.

Remaining part of the paper is synchronized as follows: section 2 describe proposed crosstalk noise model, noise avoidance technique using driver sizing is described in section 3. Section 4 illustrates the simulation results and finally section 5 concludes this paper.

II. PROPOSED CROSSTALK NOISE MODEL

In this section, we first present the 2-π model approach and derive its analytical time-domain waveform when unit step input is applied at the aggressor net. Then we will calculate expressions for peak noise (amplitude) and noise width. The noise avoidance technique known as driver sizing is presented with thee help of various sensitivity expressions.

A. 2-Π MODEL AND ITS ANALYTICAL WAVEFORM

For explaining the crosstalk noise model, the 2-π model is explained first. In this explanation, victim net is a RC interconnection line. An aggressor line is placed near the victim net, as shown in Figure 1(a) and unit step input voltage pulse is applied at the coupling location on aggressor net. In Figure 1(a), L_s represents the interconnect length of victim net before the coupling. Similarly, L_c and L_e represent the interconnect length of victim net at the coupling and after the coupling, respectively. 2-π model is reduced to a 2-π type RC model as shown in Figure 1(b). This reduction of 2-π model is very useful while calculating the value of crosstalk noise at the receiver end. This model contains two π type RC circuits, known as 2-π model. One RC circuit is located before the coupling and the other is after the coupling. The victim driver is modelled by an effective resistance R_d and other RC parameters are C_X, C_1, R_S, C_2, R_e and C_L. The values of these parameters are computed from the geometric information from Figure 1(b) in the following manner:

The node 2 is known as coupling node; this is set to be the centre of the coupling portion of the victim net i.e. $(L_s+L_c)/2$ from the source. Let the

upstream and downstream interconnect resistance/capacitance at node 2 be R_s/C_s and R_e/C_e, respectively. Then capacitance values are set to be $C_1 = C_s/2$, $C_2 = (C_s+C_e)/2$ and $C_L = C_e/2+C_1$.

In some cases one lumped RC for the victim net can be used, but 2-π model can model the coarse distributed RC characteristics. The resulting 2-π model can be solved analytically.
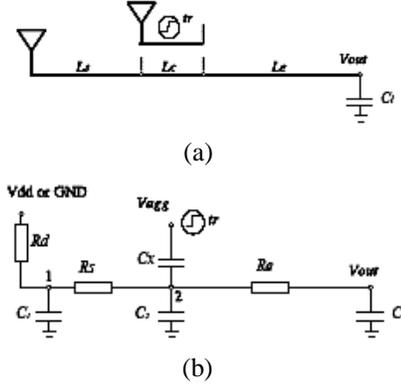

(a)

(b)

Figure 1. (a) Layout of a Victim Net and Aggressor above it; (b) 2-π Model Crosstalk Noise Model

From Figure 1(b), the impedance at node 1, Z_1 satisfying the following,

$$\frac{1}{Z_1} = \frac{1}{R_d} + sC_1 \tag{1}$$

Then at node 2, we have

$$\frac{1}{Z_2} = \frac{1}{(Z_1 + R_s)} + sC_2 + \frac{1}{R_e + \frac{1}{sC_L}} \tag{2}$$

$V_2(s)$ denotes the s-domain voltage at node 2, then

$$V_2(s) = \frac{Z_2}{Z_2 + \frac{1}{sC_L}} V_{agg}(s) \tag{3}$$

The output voltage V_{out} in the s-domain is

$$V_{out}(s) = V_2(s) \frac{\frac{1}{sC_L}}{R_e + \frac{1}{sC_L}} \tag{4}$$

Substituting Z_1, Z_2, and V_2 into $V_{out}(s)$ yields,

$$V_{out}(s) = \frac{a_2 s^2 + a_1 s}{s^3 + b_2 s^2 + b_1 s + b_0} V_{agg}(s) \tag{5}$$

where the co-efficients are

$$a_2 = \frac{K_1}{K_2}$$

$$a_1 = \frac{(R_d + R_s)C_x}{K_2}$$

$$b_2 = \frac{((C_2 + C_x)(R_e C_L(R_d + R_s) + R_d R_s C_1) + R_d R_e C_1 C_L + C_L R_d R_s C_1)}{K2}$$

$$b_1 = \frac{((R_d + R_s)(C_x + C_2 + C_L) + (R_e C_L + R_d C_1))}{K_2}$$

$$b_0 = \frac{1}{K_2}$$

$$K_1 = C_x R_d R_s C_1$$

$$K_2 = R_d R_s C_1 C_L R_e (C_x + C_2)$$

(6)

The transfer function H(s) can be expressed into the poles/residues form as,

$$H(s) = \frac{a_2 s^2 + a_1 s}{s^3 + b_2 s^2 + b_1 s + b_0} \equiv \frac{k_1}{s - s_1} + \frac{k_2}{s - s_2} + \frac{k_3}{s - s_3} \quad (7)$$

The three poles s_1, s_2 and s_3 are the three roots of $s^3 + b_2 s^2 + b_1 s + b_0 = 0$, which can be obtained analytically using standard mathematical techniques. The time domain function of each pole/residue is

$$f_i(t) = k_i e^{s_i t} \quad \text{where} \quad (i = 1, 2, 3)$$

(8)

For the aggressor with unit step input with normalized $V_{dd} = 1$, i.e.

$$V_{agg} = \begin{cases} 1 & t \geq 0 \\ 0 & \text{otherwise} \end{cases} \quad (9)$$

its Laplace transform is,

$$V_{agg}(s) = \frac{1}{s} \quad (10)$$

Then for each pole/residue pair, the s-domain output is given by,

$$V_{out}(s) = \frac{k_i}{(s - s_i)} V_{agg}(s) \quad (11)$$

From (3) and (4),

$$V_{out}(s) = -\frac{k_i}{s_i} \frac{1}{s} + \frac{k_i}{s_i} \frac{1}{(s - s_i)} \quad (12)$$

So, the time domain expression of the output voltage is $v_{out}(t) = -\frac{k_i}{s_i}(1 - \exp[s_i t])$ (for i=1, 2, 3) (13)

Therefore, the final noise voltage is simply the summation of the voltage waveform from each pole/residue pair.

$$v_{out}(t) = v_{out1}(t) + v_{out2}(t) + v_{out3}(t) \quad (14)$$

Equation (14) gives the final noise voltage waveform. The 2π model has been tested extensively and its waveform from (14) can be shown to be almost identical compared to HSPICE simulations.

B. CLOSED FORM NOISE AMPLITUDE AND WIDTH

In this subsection, formulae for noise amplitude and noise width are obtained. This is achieved when we will further simplify the original 2π model.

1) NOISE AMPLITUDE CALCULATION

On simplifying equation (2) using dominant-pole approximation method,

$$V_{out}(s) \approx \frac{a_1 s}{b_1 s + b_0} . V_{agg}(s) \quad (15)$$

where

$$V_{agg}(s) = \frac{1}{s} \quad (16)$$

So,

(17)

$$V_{out}(s) \approx \frac{t_x}{t_v\left(s + \frac{1}{t_v}\right)}$$

where the co-efficient are,

$$t_x = (R_d + R_s)C_x \quad (18)$$

$$t_v = (R_d + R_s)(C_x + C_2 + C_L) + (R_e C_L + R_d C_1) \quad (19)$$

The term t_x represents the RC delay term from the upstream resistance of the coupling element times the coupling capacitance. The term t_v represents distributed Elmore delay of victim net.

The output voltage shown in (6) can be expressed in time domain and given in (20).

$$v_{out}(t) \approx \frac{t_x}{t_v} \exp\left[-t/t_v\right] \quad (20)$$

where $t \geq 0$.

From the noise expression shown in (20), it is evident that noise monotonically decreases as $t \geq 0$. The value of noise will be maximum at t=0. This maximum value of noise can be calculated by putting t=0 in (20).

So,

$$v_{max} \approx \frac{t_x}{t_v} \quad (21)$$

Equation (21) represents the maximum amplitude of noise which is obtained at t=0.

2) NOISE WIDTH CALCULATION

The noise width for a noise pulse is defined to be the length of time interval so that the noise spike voltage v is larger than or equal to v_t where v_t represents the threshold voltage.

From (20),

$$v_{out}(t) \approx \frac{t_x}{t_v} \exp\left[-t/t_v\right] \quad (22)$$

So, $t = t_v \ln\frac{1}{v_{out}}.\frac{t_x}{t_v}$ (23)

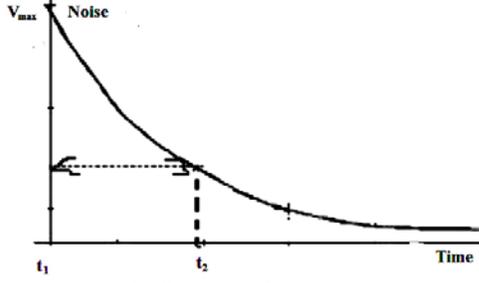Noise width is the width of time interval between t_1 and t_2.

Figure 2. Illustration of the Noise Width

The value of t_2 can be calculated using equation (23). Hence, t_2 can be derived as,

$$t_2 = t_v \ln \frac{1}{v_{out}} \frac{t_x}{t_v}$$

(24)

At t_2, the noise voltage is v_t. So,

$$t_2 = t_v \ln \frac{1}{v_t} \frac{t_x}{t_v}$$

(25)

Noise width is given by,

$$t_{width} = t_2 - t_1$$

(26)

Substituting the values of t_1 and t_2 from equations (24) and (25)

$$t_{width} = t_v \ln \frac{1}{v_t} \frac{t_x}{t_v}$$

(27)

In this paper, we assume the value of threshold voltage v_t to be half of the value of the peak noise voltage v_{max}.

i.e. $v_t = \dfrac{v_{max}}{2}$

(28)

From (21), (27) and (28),

$$t_{width} = t_v \ln 2$$

(29)

This expression represents the width of the noise voltage waveform.

Note that when the time increases beyond t_2, the noise voltage becomes very less. In the above calculation we ignored the effect of that noise. In some conditions peak noise exceeds certain threshold voltage but remains immune to the noise. This can be expressed clearly by some noise amplitude versus noise width plots.

III. NOISE AVOIDANCE TECHNIQUE USING DRIVER SIZING

Driver sizing can help to reduce the peak crosstalk noise, since a strong driver is more capable to sustain a noise spike. Our model does indicate some situation under which increasing driver size (i.e., reduce R_d) may help to reduce the peak noise and noise width. It also indicates the situation under which increasing

driver size may not help to reduce the peak noise and noise width. If we consider the case where the aggressor driver is sized down, its effective conductance decreases thus as a result of this it induces less amount of noise on a victim net driver. This can be explained with the help of sensitivity expressions of peak noise and noise width to driver resistance R_d.

$$\frac{\partial v_{max}}{\partial R_d} = \frac{C_x}{t_v} - \frac{t_x}{t_v^2}(c_x + c_1 + c_2 + c_L)$$

(30)

$$\frac{\partial t_{width}}{\partial R_d} = c_x \cdot \frac{t_v}{t_x} + \left[\ln\left(\frac{1}{v_t} \cdot \frac{t_x}{t_v}\right) - 1 \right](c_x + c_1 + c_2 + c_L)$$

(31)

These above sensitivity expressions discuss the effect of the driver resister size on the maximum noise amplitude and noise width in the RC interconnection lines.

IV. SIMULATION RESULT AND DISCUSSIONS

In this paper we are using the value of parameters R, and C using 90 nm technologies. So the exact values of the parameter R and C using 90 nm technologies [1] are given in Table 1.

TABLE 1: RC Parameters of a Minimum Sized Wire in a 90 nm Technology

Parameter(s)	Value/mm
Resistance(R)	13Ω/mm
Capacitance(C)	0.45pF/mm

Expressions given by equations (21) and (29) represent the analytical and closed form formulae for maximum noise amplitude and width of noise voltage for proposed 2-π model. These expressions are verified and tested on randomly generated multi-pin nets with general RC tree structures and the efficiency of the proposed models are justified when compared to SPICE simulations. To obtain high fidelity and to detect the corner scenarios, we run our 2π model on 1000 randomly generated circuits with realistic parameters in a 90 nm technology. For the test circuits, the driver resistance R_d is from 100 to 500 $\Omega\cdot$, the loading capacitance C_L is from 10 to 100fF , the length parameters L_s, L_c, and L_e are from 1 to 2500 μm, the wire width/spacing is either 1x or 2x minimum width/spacing, and the aggressor slew is from 50 to 500 ps.

Table 2 discusses the comparative study in between proposed model crosstalk noise voltage with SPICE crosstalk values for different aggressor slews for randomly selected parameter values. From Table 2, it can be analyzed that error presented by this model is less than 1% on average compared with SPICE simulation, for peak noise crosstalk voltage.
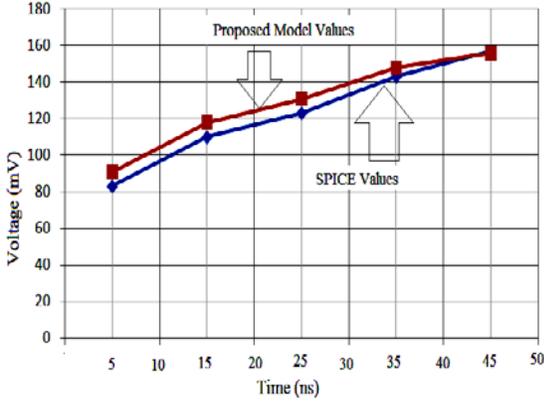
Figure 3. Comparison of Peak Noise Voltage obtained from Proposed Model and SPICE with T_s=100 ps
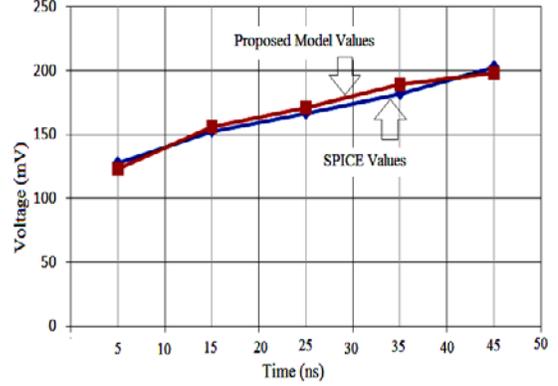

Figure 4. Comparison of Peak Noise Voltage obtained from Proposed Model and SPICE with T_s=200 ps

TABLE 2: Comparison of Proposed Crosstalk Noise Voltage with SPICE result values for different Aggressor Slew in a 90 nm Technology

R_{D1} (Ω)	R_{D2} (Ω)	C_L (fF)	T_s=100		T_s=200		T_s=500	
			SPICE Values (mV)	Proposed Model Values (mV)	SPICE Values (mV)	Proposed Model Values (mV)	SPICE Values (mV)	Proposed Model Values (mV)
100	100	10	83	91	128	123	146	146
100	150	30	110	118	153	156	169	164
200	250	50	123	131	167	171	193	201
300	350	70	143	148	182	189	217	221
400	500	100	157	156	203	198	231	239

TABLE 3: Comparison of Proposed Noise Width with SPICE result values for different Aggressor Slew in a 90 nm Technology

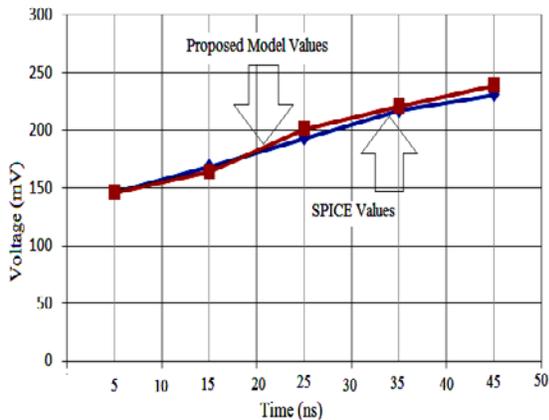| R_{D1} (Ω)	R_{D2} (Ω)	C_L (fF)	T_s=100		T_s=200		T_s=500	
			SPICE Values (ns)	Proposed Model Values (ns)	SPICE Values (ns)	Proposed Model Values (ns)	SPICE Values (ns)	Proposed Model Values (ns)
100	100	10	4.54	3.89	7.23	7.83	11.23	11.94
100	150	30	6.21	6.54	8.87	9.25	12.89	13.45
200	250	50	7.59	7.43	10.65	11.34	14.54	14.84
300	350	70	8.52	9.01	12.38	12.93	15.89	15.92
400	500	100	12.34	11.96	15.28	14.78	18.38	19.24

Figure 4. Comparison of Peak Noise Voltage obtained from Proposed Model and SPICE with T_s=500 ps

Table 3 discusses the comparative study in between proposed model noise width with SPICE values for different aggressor slews for randomly selected parameter values.

V. CONCLUSION

In this paper presents a reduction and optimizations of crosstalk and driver sizing in much improved 2-π model using 90nm process technology parameters. In this paper we consider a step input signal for the excitation of aggressor line. Different sensitivity expressions are derived for the driver sizing and spacing. By considering the signs of sensitivity expressions, effect of driver sizing spacing (aggressor net and victim net) on crosstalk noise amplitude and width can be examined.

REFERENCES

[1] Semiconductor Industry Association, National Technology Roadmap for Semiconductors, (2014).

[2] J.Venkateswara Rao, A.V.N.Tilak, "A Bus Encoding to Reduce Crosstalk Noise Effect in System on Chip," International Journal of VLSI design & Communication Systems (VLSICS), 2, 110-118 (2011).

[3] Shikha Singh,V. Sulochana Verma, "Reduction of Crosstalk Noise and Delay in VLSI Interconnects Using Schmitt Trigger as a Buffer and Wire Sizing," Advances in Intelligent Systems and Computing, 178,677-686 (2013)

[4] Pritam Bhattacharjee, Arindam Sadhu,"VLSI Transistor andInterconnect Scaling Overview", Journal of Electronic Design Technology, STM Journal, 5, 1-15 (2014).

[5] Vikas Maheshwari, Anushree, Rajib Kar, Durbadal Mandal, A.K. Bhattacharjee," Noise Modelling for RC Interconnects in Deep Submicron VLSI Circuit for Unit Step Input" Journal of Electron Devices, 11, 632-636 (2011)

[6] Pekka Miettinen, Mikko Honkala, Janne Roos, and Martti Valtonen, "Sparsification of Dense Capacitive Coupling of Interconnect Models," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 21, 1955–1959 (2013).

[7] A.B. Kalpana, P.V. Hunagund, "Circuit Model for Interconnect Crosstalk Noise Estimation in High Speed Integrated Circuits," Advance in Electronic and Electric Engineering, 3, 907-912 (2013).

[8] Ahlam Guen Bouazza, Benyounes Bouazza, "Crosstalk Noise and Signal Propagation Delay Analysis in Submicron CMOS Integrated Circuits," 6th International Conference on Sciences of Electronics, Technologies of Information and Telecommunications (SETIT), Orient Palace Sousse, Tunisia, pp. 155-160, 21 - 24 March (2012).

[9] LI Jianwei, DONG Gang, WANG Zeng, YE Xiaochun, "Statistical Interconnect Crosstalk Noise Model and Analysis for Process Variations," Chinese Journal of Electronics, 24, 83-87 (2015).

[10] Feng Shi, Xuebin Wu, Zhiyuan Yan, " New Crosstalk Avoidance Codes Based on a Novel Pattern Classification," IEEE Trans on VLSI, 21,1892 – 1902 (2013).

[11] Irfanullah Nariyal, S. Roy, S., Masud M.M., Ijaz B., Braaten B.D.,"Analysis of the Noise Voltage Coupling (Crosstalk) Between Right-Handed and Composite Right/Left-Handed (CRLH) Transmission Lines on Printed Circuit Boards" IEEE Trans on EMC, 55, 1-10 (2013).

[12] M. Kavicharan, N. S. Murthy, N. Bheema Rao," A closed-form delay estimation model for current-mode high speed VLSI interconnects," IEEE Technological Advances in Electrical, Electronics and Computer Engineering (TAEECE),pp. 502-506, Konya, 9-11 May, (2013)

[13] P. V. Hunagund, A. B. Kalpana, "Crosstalk Interconnect Noise Optimization Technique Using Wire Spacing and Sizing for High Speed Integrated Circuits," IACSIT International Journal of Engineering and Technology, 3, 684-688, (2011).

[14] P. V. Hunagund, A. B. Kalpana, "Crosstalk Noise Modeling for RC and RLC interconnects in deep submicron VLSI circuits," Journal of computing , 2, 60-65 (2010).

[15] V. Maheshwari, Anushree, Saupayan Mazumdar, R. Kar, D. Mandal, A.K. Bhattacharjee, "2-π Crosstalk Noise Model for Deep Submicron VLSI Global RC Interconnects,"IEEE International Conference on Electronics Design,Systems and Applications, pp-225-229, Kuala Lumpur, Malaysia, 5-6 November (2012).

[16] Anushree, Vikas Maheshwari, "Crosstalk Noise Reduction using Wire Spacing in VLSI RC Global Interconnects", Journal of Electron Devices, France, 20, 1755-1760, (2014).

[17] Vikas Maheshwari, Naomi Joshi,Er Anushree, Rajib Kar,Durbadal Mandal, Anup Kr. Bhattacharjee, "4-π Crosstalk Noise Model for Deep Submicron VLSI Global RC Interconnects", IEEE Symposium on Humanities, Science and Engineering Research (SHUSER-2012), Kuala Lumpur, Malaysia, pp. 355-360, June 24-27, (2012).

[18] Vikas Maheshwari, Anushree, Rajib Kar, Durbhadal Mandal, A.K. Bhattacharjee, "Noise Modelling for RC Interconnects in Deep Submicron VLSI Circuit for Unit Step Input", Journal of Electron Devices, 11, 632-636, (2011).

[19] Kausik B K, Sarkar S, Agarwal R P, Joshi R C, "An Analytical Approach to Dynamic Crosstalk in Coupled Interconnects".Microelectronics journal, 41, 85-92 (2010).

.