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# Electrical Characterization of Au Schottky Contacts on N-Type 4H-SiC

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#### Abstract

Gold Schottky contacts on n-type 4H-SiC were fabricated. Physical and electrical characteristics were analyzed through standard current-voltage (I-V) and capacitance-voltage (C-V) measurement methods. Schottky contacts were deposited using gold layers of thickness 200nm and the annealing treatments have been performed up to 400 °C using a rapid thermal annealing process (RTA). The Schottky barrier height, ideality factor and doping concentration were calculated using I-V and C-V for both asdeposited and annealed contacts at room temperature. A barrier height of 1.46eV and 1.49eV was obtained for as deposited contacts by I-V and C-V measurement methods respectively.

Keywords: Schottky Diodes, rapid thermal annealing, Schottky barrier height (SBH), Ideality factor.

# I. INTRODUCTION

Silicon Carbide (SiC) is one of the most promising semiconductor materials for imminent generation of power devices. This is mainly due to intrinsic properties of Silicon Carbide such as high breakdown field strength, a high value of saturated electron drift velocity, reasonable electron mobility and high thermal conductivity. These properties make this material superior to other semiconductors like Si, GaAs, AlN etc. The promising properties of SiC for the fabrication of high quality devices depend to a large extent on the quality of the metal-SiC contact. 4H-SiC has been chosen for the fabrication of Schottky barrier diodes (SBDs), primarily because its superior electrical properties like bandgap and electron mobility than the other polytypes of SiC [1]-[3].

A lot of experimental and theoretical studies have been carried out in recent years to illustrate the current transport contact Carbide. Schottky 4H-Silicon Metal/semiconductor interface plays a critical role in performance of all electronic

Investigation of this contact for various metal contacts and

understanding of these properties. Although several studies related to Schottky contacts have been carried out during the last two decades [4]-[10], the current transport and the temperature dependence of the barrier height in 4H-SiC Schottky diodes remain a topic of current interest. SiC Schottky diodes mostly found to illustrate non-ideal current-voltage (I-V) characteristics and exhibit an anomalous deviation in barrier height (fB) and ideality factor (h) with respect to changing temperature [11]. Several publications on the fabrication of 4H-SiC Schottky barrier diodes using various metal contacts are available [6]-[12]. However, to our knowledge there is little information available on Au/4H-SiC Schottky contacts. Au/SiC is an interesting interface as Au form neither silicides nor carbides with SiC. That is why we planned to

under various conditions is essential for a clear

## II. FABRICATION AND CHARACTERIZATION OF DIODE

investigate Au/4H-Sic Schottky diodes.

The starting material used for the fabrication of Schottky diodes was n-type 4H-SiC (0001), 8° off Si face from Cree Inc. The substrate was n+-type with a donor concentration of  $1\times10^{18}$ cm<sup>-3</sup> and having specific resistivity of  $0.020\Omega$ cm on which a 48-µm thick lightly doped (N<sub>D</sub>=9×10<sup>14</sup> cm<sup>-3</sup>) n-

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type 4H-SiC epi-layer was grown. Schematic of the diode is shown in figure.1. Prior to metal deposition for making Schottky contacts on front side of samples, the samples were degreased in organic solvents like acetone, trichloroethylene and methanol successively. Immediately before the deposition of gold the samples were etched in an aqueous solution of 10% HF for 20s followed by rinsing in de-ionized (DI) water and blow drying. Au films were deposited using e-beam metallization technique through a metal contact mass at a pressure of 6×10<sup>-7</sup>Torr. A 200 nm thick layer of gold was deposited on Si face of 4H-SiC for making the Schottky contact which led to the fabrication of circular diodes with diameters of 1mm.

The forward current-voltage (I-V) characteristics were measured at room temperature with Keithley model 236 Source Measure Unit (SMU) from 0V-5V and the capacitance-voltage (C-V) characteristics were measured using Agilent LCR meter at frequencies of 1 MHz and 100 kHz and a voltage sweep of -5 to 1 V.

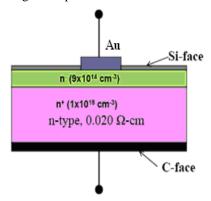


Figure 1. Schematic crossectional diagram of Schottky barrier diode

#### III. RESULTS AND DISCUSSION

#### A. The current-voltage characteristics

According to thermionic-emission theory, the experimental current-voltage (I-V) characteristics of forward biased Schottky contacts are expressed as [15]- 16]

$$I = AA^*T^2 \exp(\frac{-q\phi_B}{kT})[\exp(\frac{qV}{nkT}) - 1]$$
 (1)

$$I_{S} = AA^{*}T^{2} \exp(-\frac{q\phi_{B}}{kT})$$
 where (2)

represents the reverse saturation current, q is the electron charge, A is the area of contact,  $A^* = 146 A/cm^2 K^2$  for 4H-SiC, is the Richardson's constant,  $\phi_B$  is the barrier height, k is the Boltzmann constant, T is absolute temperature, V is the forward bias voltage and n is the ideality factor which is calculated from the slope of the linear region of the forward bias lnJ-V characteristics through the relation:

$$n = \frac{q}{kT} \frac{dV}{d(\ln J)} \tag{3}$$

Ideality factor n is unity for an ideal diode. Higher values of n can be attributed to the presence of thin oxide interfacial layer, inhomogeneities in barrier and series resistance [8]. Among all these barrier inhomogeneity is the main cause for non-ideal behavior [12]. I-V measurement is one of the most commonly used techniques to determine the transport mechanism in Schottky barrier diodes. In order to get more insights into the current transport mechanism through Au/4H-SiC system, I-V measurements were carried out after every thermal anneal process in the temperature range from 100-400°C. Fig. 2 shows forward I-V characteristic for as-deposited and thermally annealed Au/4H-SiC Schottky diodes.

For the calculation of barrier height the current density J was plotted on a logarithmic scale versus the applied voltage V. The resulting plot exhibits a linear region in the low voltage range of the semi-log plot. The Barrier height was calculated from the equation [16, 19]

$$\phi_B = \frac{kT}{q} \ln(\frac{A^* T^2}{J}) \tag{4}$$

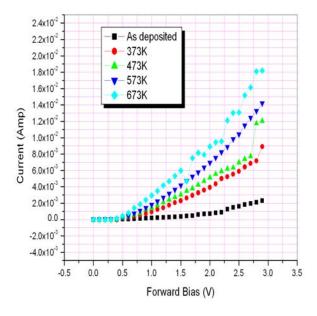


Figure 2. Forward I-V characteristics of Schottky diodes after different annealing temperature

Fig.3 shows a current density-voltage (J-V) plot (characteristics) of a typical Au/4H-SiC Schottky diode of diameter 1mm for as-deposited and various annealing temperatures. The barrier height of as deposited diode is 1.46eV. After annealing in the temperature range from 100-400°C for 20 min in nitrogen ambient, the barrier heights

improved with the maximum value of 1.78eV. Ideality factor was calculated from the slope of linear region of current density-voltage (J-V) characteristics of the diode which was 1.85 for as deposited diode. The value of n was then calculated for various annealing temperatures and the results are shown in table 1.

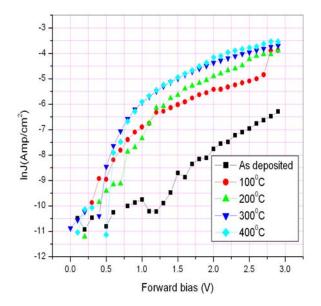


Figure 3. J-V characteristics of Schottky diodes after different annealing temperature

Table 1. Electrical parameters of Au/4H-SiC Schottky diodes extracted from I-V and C-V characteristics measured after RTA at different temperatures

Temperature in <sup>0</sup> C	I-V Barrier Height (eV)	C-V Barrier Height (eV)	Ideality Factor (n)
As-deposited	1.46	1.49	1.85
100	1.51	1.56	1.68
200	1.63	1.67	1.24
300	1.74	1.78	1.20
400	1.78	1.81	1.01

Fig.4 shows the variation in barrier height and ideality factor of Au/4H-SiC Schottky with respect to annealing temperature obtained from the measurements through I-V characteristics. This plot illustrates that barrier height increases and ideality factor decreases with the increase in annealing temperature. Similar results were reported by Perez et al for Ni/Ti Schottky contacts on 4H-SiC [11]. The observation that the ideality factor is larger than unity even at higher temperatures can be explained by inhomogeneities of the Schottky barrier as already reported in [17].

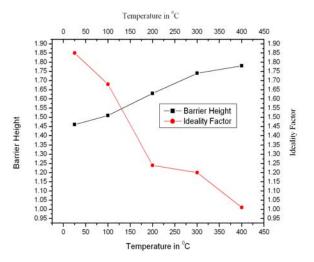


Figure 4. Dependence of I-V Barrier height and Ideality factor on Temperature

### **B.** Capacitance-voltage characteristics:

When capacitance-voltage (C-V) measurements are carried out at sufficiently high frequency, the charge at the interface states cannot follow the a.c. signal. This will occur when the time constant is too long to allow the charge to move in and out of the states in response to applied signal. Thus, depletion region capacitance of Schottky barrier diode can be expressed as [18]

$$\frac{1}{C^2} = \frac{2(V_{bi} + V_r - kt/q)}{q\varepsilon_e \varepsilon_0 A^2 N_D}$$
 (5)

where  $V_{bi}$  is the built-in voltage which can be determined from the extrapolation of the  $1/C^2$  versus V plot to the voltage axis,  $V_r$  is the reverse voltage, A is the area of the diode,  $\epsilon_s$  is the static dielectric constant equal to 9.66 for 4H-SiC [19],  $\epsilon_0 = 8.85 \times 10^{14}$  F/cm and  $N_D$  is the concentration of the donors. The  $N_D$  is related to the slope of  $1/C^2$  versus V curve and can be obtained from the relation given below

$$N_D = \frac{2}{q\varepsilon_s \varepsilon_0 A^2} \left[ \frac{1}{d(C^{-2})/dV} \right]$$
 (6)

The barrier height deduced from capacitance-voltage measurement is calculated from

$$\phi_B = V_{bi} + V_n + \frac{kT}{q} - \Delta\phi \tag{7}$$

where  $V_n$ , referred to as the Fermi level potential, is the energy difference between the Fermi level and the bottom of the conduction band, and can be given by  $V_n = kT/q[ln(N_c/N_D)]$ . Thus, Eq. (7) can be rewritten by neglecting the image-force barrier lowering ( $\Delta \Phi$ ) as

$$\phi_B = V_{bi} + \frac{kT}{q} \left[ 1 + \ln \frac{N_C}{N_D} \right] \tag{8}$$

where  $N_C$  is the effective density of states in the conduction band and is taken equal to  $1.7X10^{19} cm^{-3}$ [19].

Figure 5 shows the reverse bias 1/C<sup>2</sup> versus V plots for the Au/4H-SiC SBD as a function of temperature at a frequency of 1 MHz. The linear 1/C<sup>2</sup> versus V plots indicate a constant donor concentration in the depletion layer and absence of metal-semiconductor interaction. Moreover, the linear behavior of the curves can be explained by the fact that the interface states and the inversion layer charge can not follow the a.c. signal at 1.0 MHz and consequently do not contribute appreciably to the diode capacitance. The V<sub>bi</sub> and N<sub>i</sub> values are obtained from the intercepts and the slopes of the extrapolated 1/C<sup>2</sup> versus lines with the V axis, respectively. Then, the values of barrier height are calculated using Equ. (8) and are tabulated in table 1. From C-V measurements doping concentration of the epilayer was calculated to be equal to 1.45X10<sup>15</sup>cm<sup>-3</sup> is in good agreement with the values given by manufacturer. Schottky barrier height values are higher for C-V measurements, as barrier heights deduced from two techniques are not same. This is because the differential capacitance is determined by the width of the depletion region which depends only on diffusion voltage and the donor density and barrier height is given by equ. (8) which does not include image force barrier lowering. Thus C-V method essentially gives flat band barrier height. The difference between barrier heights obtained from I-V and C-V measurements is explained due to existence of traps in substrate, effect of image force and barrier inhomogeneities.

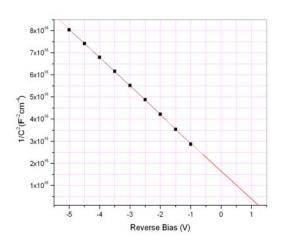


Figure 5. 1/C<sup>2</sup> vs. voltage plot of the Au/4H-SiC Schottky barrier diode

#### IV. CONCLUSION

The current and capacitance transport mechanism in Au/4H-SiC Schottky contacts with different thermal anneals in temperature range from 100-400°C have been reported in this paper. Au/4H-SiC Schottky diodes were characterized by I-V and C-V measurement techniques to extract Schottky parameters like barrier height, ideality factor and doping concentration of the epilayer. Barrier height calculated on as-deposited contacts was 1.46 and 1.49eV from I-V and C-V techniques respectively. Diodes showed non-ideal behavior at room temperature having ideality factor of 1.85. Rapid Thermal annealing appears to be an essential step to reduce the non-ideality.

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