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Low-Power 2:1 Multiplexer Circuit Design Using Sense-amplifier Logic Style

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Abstract
Recently reported an enormous increase in structured and unstructured data which has to be stored and transferred at fast-speed with least propagation delay. Sense-amplifier circuits are used for designing of memories. Multiplexer are combinational circuit used for communication of parallel input data into serial output data. In this paper 2:1 multiplexer circuit using various sense-amplifier logic styles have been realized. This paper also shows the comparison study of various different sense-amplifier circuits with respect to power, delay and power-delay product using BSIM 3V3 Tanner EDA tool over a range of voltage on 90nm technology.

Keywords: Sense-amplifier circuits, multiplex circuit, CMOS, low-voltage low-power logic styles, robustness, VLSI circuit design.

I. INTRODUCTION

THE increasing demand for low-power very large scale integration (VLSI) can be addressed at different design levels, such as the architectural, circuit, layout and the process technology level [1]. At the circuit design level, considerable potential for power savings exists by means of proper choice of a logic style for implementing combinational circuits. This is because all the important parameters governing power dissipation, switching capacitance, transition activity, and short-circuit currents are strongly influenced by the chosen logic style. Depending on the application, the kind of circuit to be implemented and the design technique used different performance aspects become important, disallowing the formulation of universal rules for optimal logic styles. The power dissipation characteristics of various existing logic styles are compared qualitatively and quantitatively by actual logic gate implementations and simulations under realistic circuit arrangements and operating conditions [2]. Section II gives a short introduction to the most important sense amplifier logic styles and compares them qualitatively. Results of quantitative comparisons based on simulations of different logic style as well as implementation on multiplexer are given in Section III. Some conclusions are finally drawn in Section IV.

II. LOGIC STYLE

A. Impact of Logic Style

The logic style used in logic gates basically influences the speed, size, power dissipation and the wiring complexity of a circuit. The circuit *delay* is determined by the number of inversion levels, the number of transistors in series, transistor sizes (i.e., channel widths) and intra- and inter-cell wiring capacitances. Circuit *size* depends on the number of transistors and their sizes and on the wiring complexity. *Power dissipation* is determined by the switching activity and the node capacitances (made up of

gate, diffusion and wire capacitances) the latter of which in turn is a function of the same parameters that also control circuit size. Finally, the *wiring complexity* is determined by the number of connections and their lengths and by whether single-rail or dual-rail logic is used. All these characteristics may vary considerably from one logic style to another and thus make the proper choice of logic style crucial for circuit performance. As far as cell-based design techniques (e.g., standard-cells) and logic synthesis are concerned, *ease-of-use* and *generality* of logic gates is of importance as well. *Robustness* with respect to voltage and transistor scaling as well as varying process and working conditions, and *compatibility* with surrounding circuitries are important aspects influenced by the implemented logic style.

B. Logic Style Requirements for Delay

According to the formula

$$\mathbf{t_{pd} \propto (C/I)\,\Delta V}$$

The delay (t_{pd}) of logic gate depends on its output current I, load capacitance C and output voltage swing ΔV. Faster circuits families attempt to reduce one of these terms. nMOS transistor provide more current than pMOS for the same sizes and capacitance, so nMOS network are preferred. Observe that the logical effort is proportional to the C/I term because it is determined by the input capacitance of a gate that can deliver a specified output current.

C. Logic Style Requirements for Low Power

According to the formula

$$P_{dyn} = V_{DD}^2 \cdot f_{clk} \cdot \sum_n \alpha_n \cdot c_n + V_{DD} \cdot \sum_n i_{sc_n}$$

The dynamic power dissipation of a digital CMOS circuit depends on the supply voltage V_{dd}, the clock frequency f_{clk}, the node switching activities α_n, the node capacitances c_n, the node short circuit currents i_{scn} and the number of nodes η. A reduction of each of these parameters results in a reduction of dissipated power.
However, clock frequency reduction is only feasible at the architecture level, whereas at the circuit level frequency f_{clk} is usually regarded as constant in order to fulfil some given throughput requirement. All the other parameters are influenced to some degree by the logic style applied. Thus, some general logic style requirements for low-power circuit implementation can be stated at this point.

1) Switched capacitance reduction:
Capacitive load, originating from transistor capacitances (gate and diffusion) and interconnect wiring, is to be minimized. This is achieved by having as few transistors and circuit nodes as possible and by reducing transistor sizes to a minimum. In particular, the number of (high capacitive) inter-cell connections and their length (influenced by the circuit size) should be kept minimal. Another source for capacitance reduction is found at the layout level [3], which, however is not discussed in this paper. Transistor downsizing is an effective way to reduce switched capacitance of logic gates on noncritical signal paths [4]. For that purpose, a logic style should be robust against transistor downsizing, i.e., correct functioning of logic gates with minimal or near-minimal transistor sizes must be guaranteed (*ratio less* logic).

2) Supply voltage reduction:
The supply voltage and the choice of logic style are indirectly related through delay-driven voltage scaling. That is, a logic style providing fast logic gates to speed up critical signal paths allows a reduction of the supply voltage in order to achieve a given throughput. For that purpose, a logic style must be robust against supply voltage reduction, i.e., performance and correct functioning of gates must be guaranteed at low voltages as well. This becomes a severe problem at very low voltages of around 1V and lower, where noise margins become critical [5], [6].

3) Switching activity reduction:
Switching activity of a circuit is predominantly controlled at the architectural and registers transfer level (RTL). At the circuit level, large differences are primarily observed between static and dynamic logic styles. On the other hand, only minor transition activity variations are observed among different static logic styles and among logic gates of different complexity, also if glitching is concerned.
4) Short-circuit current reduction:
Short-circuit currents (also called dynamic leakage currents or overlap currents) may vary by a considerable amount between different logic styles. They also strongly depend on input signal slopes (i.e., steep and balanced signal slopes are better) and thus on transistor sizing. Their contribution to the overall power consumption is rather limited but still not negligible (≈ 10–30%), except for very low voltages Vdd ≤ Vtn + Vtp, where the short-circuit currents disappear. A low-power logic style should have minimal short-circuit currents and, of course, no static currents besides the inherent CMOS leakage currents.

D. Logic Style Requirements for Ease-of-Use
For ease-of-use and generality of gates, a logic style should be highly robust and have friendly electrical characteristics, that is *decoupling* of gate inputs and outputs (i.e., at least one inverter stage per gate) as well as good *driving capabilities* and full *signal swings* at the gate outputs, so that logic gates can be cascaded arbitrarily and work reliably in any circuit configuration. These properties are prerequisites for cell-based design and logic synthesis, and they also allow for efficient gate modelling and gate-level simulation. Furthermore, logic style should allow the efficient implementation of arbitrary logic functions and provide some regularity with respect to circuit and layout realization. Both low-power and high-speed versions of logic cells (e.g., by way of transistor sizing) should be

supported in order to allow flexible power-delay tuning by the designer or the synthesis tool.

E. Sense-Amplifier Circuits

Sense amplifier magnifies small differential input voltages into larger output voltages. They are commonly used in memories where differential bit lines have enormous capacitive loads. Due to of large load, the bit lines swing slowly. To reduce this delay, the bit line voltages are first equalized. As they are driven apart, the sense amplifier can detect a small swing and bring it up to normal logic levels. This reduces the ΔV term in delay formula; in other words, it reduces the delay by avoiding waiting for a full swing on the bit lines. Sense amplifier circuits offer potential for reducing delay in heavily loaded logic circuits. Some general sense-amplifier logic styles are as follows.

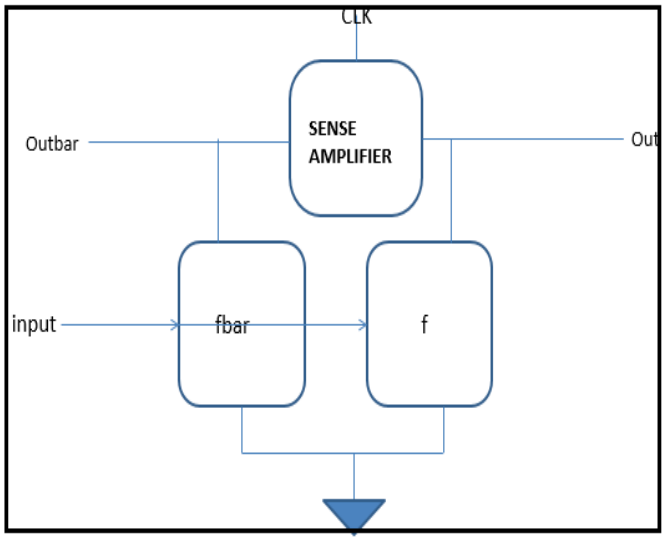

Fig. 1. Circuit arrangement for simulation of sense-amplifier circuits

1) Sample Set Differential Logic(SSDL)

Sample set differential logic (ssdl) modifies dual-rail domino logic by adding a clocked sense amplifier and modifying the clocking [7]. Rather than using precharge and evaluation phases, SSDL uses *sample* and *set* phases. During sample, clk is low and both the precharge and evaluation transistors are ON. One of the internal nodes(X or Xbar) is precharged high while other experiences contention between the prechage transistor and pull-down stack so its output settles somewhere below Vdd. Static power is consumed through the sample phase. During set when clk is high, prcharge and evaluate transistors turn OFF and the clocked sense amplifier turns ON. The amplifier tends to pull the lower of the two internal nodes down to gnd. At first, it tends to pull down the other side as well, so it is helpful to have a keeper to restore the high level.

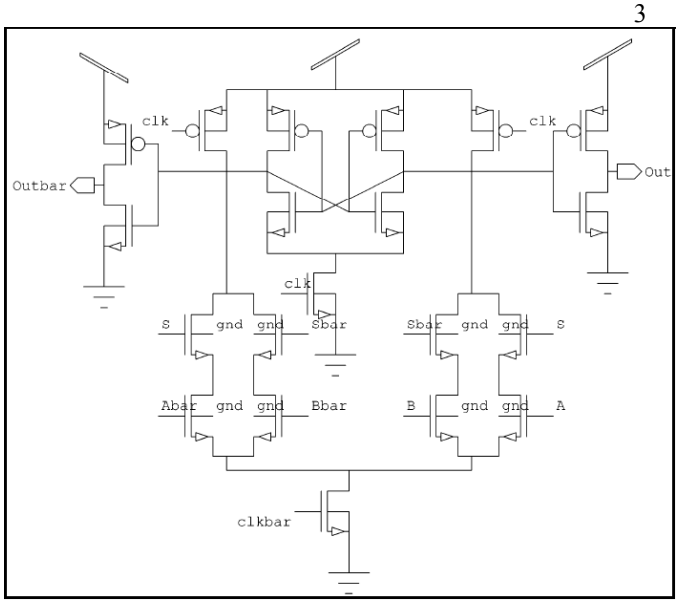

Fig. 2. Schematic of SSDL circuit

2) Enable/Disable CMOS Differential Logic (ECDL)

Enable/disable CMOS Differential Logic (ecdl) improves on SSDL by eliminating the static power consumption [8], [9]. The sense amplifier is made from a pair of cross-coupled clocked inverters. The cycle is again divided into two phases of operation *enable* and *disable.* When clk is high, the gate is disabled. Both outputs are pulled low and the pull-up stack is turned OFF. When clk fall, the gate is enabled. The cross-coupled pMOS transistors are both initially ON and attempt to pull the outputs high. One output will be held down by its pull-down stack and will lag. Positive feedback will pull one output fully low. The sense amplifier rising delay is somewhat longer than in SSDL because it pulls high through two series pMOS transistors.

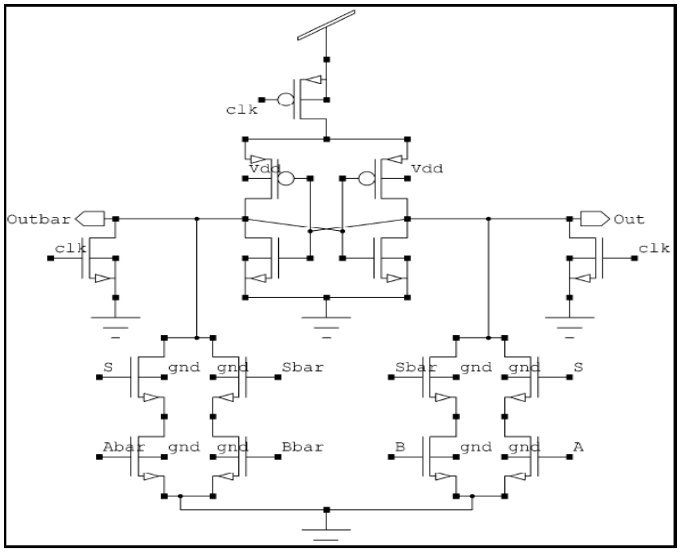

Fig. 3. Schematic of ECDL circuit

3) Latched CMOS Differential Logic (LCDL)

Latched CMOS differential logic (lcdl) adds a sense amplifier directly to the output nodes of a dual-rail domino gate and includes n-latches on the outputs [10]. The topology is similar to SSDL, but the noninverted clock is used for evaluation. The sense amplifier fires at exactly the same time as the dual-rail gate, so there is a serious risk of amplifying noise rather than signal. This can be overcome with a second clock to delay firing the amplifier.

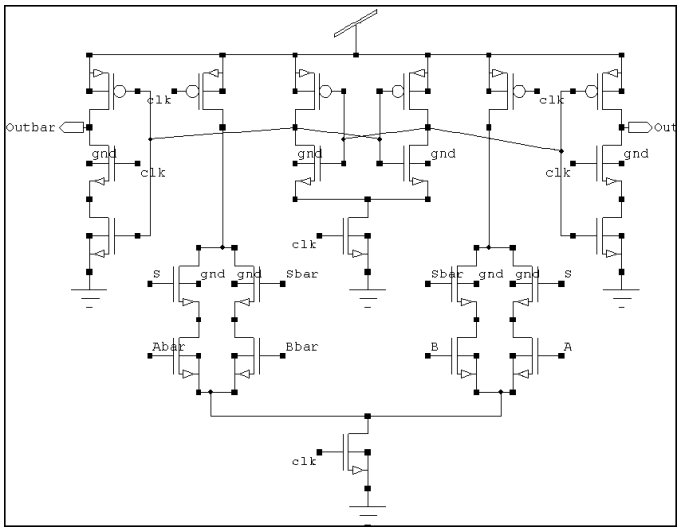

Fig. 4. Schematic of LCDL circuit

4) Differential Current Switch Logic (DCSL)

Differential circuits can consume significant power because one the output transitions every cycle. *Differential circuit switch logic (DCSL)* seeks to reduce the power consumption of internal nodes and offer higher speed by swinging the pull-down networks through a small voltage [11]. This is done by adding a pair of feedback transistors N1 and N2 to the SSDL and ECDL structure to cut off the pull-down networks before the internal nodes rise far above 0.

DCSL1 is a "precharge high" circuit related to SSDL and LCDL. When the clock is low, the outputs precharge high. When the clock rises, the circuit begins evaluation. As one side or the other pulls low, the sense amplifier accelerates the transition. N1 or N2 turns off to prevent the internal nodes of the pull-down stack on the other side from rising too much.

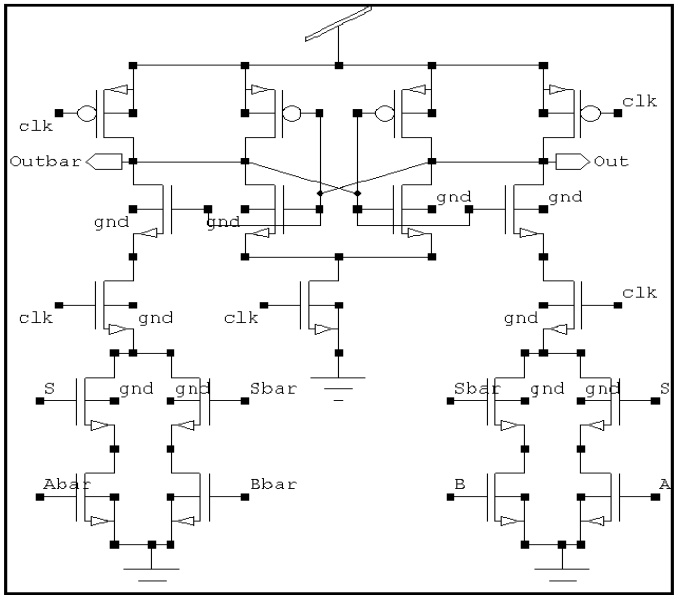

Fig. 5. Schematic of DCSL1 circuit

DCSL2 is a "precharge low" circuit related to ECDL. It again adds N1 and N2 to prevent the internal nodes from rising too much. DCSL3 improves on DCSL2 by replacing the two predischarge transistors with a single equalization transistor.

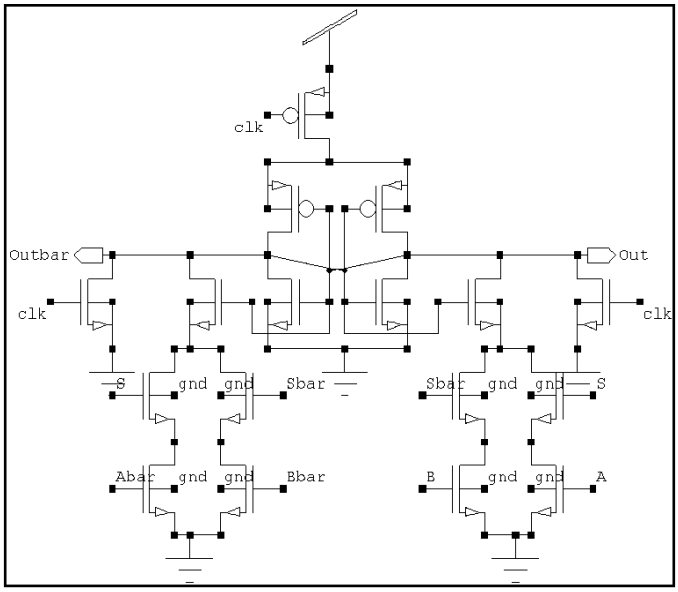

Fig. 6. Schematic of DCSL2 circuit

Sense amplifiers fire at same time as the outputs begin to fall; DCSL is sensitive to amplifying noise instead of signal. It performs for Vdd < 5Vt. LVDCSL operates better at low voltages but uses a complex sense amplifier [12].

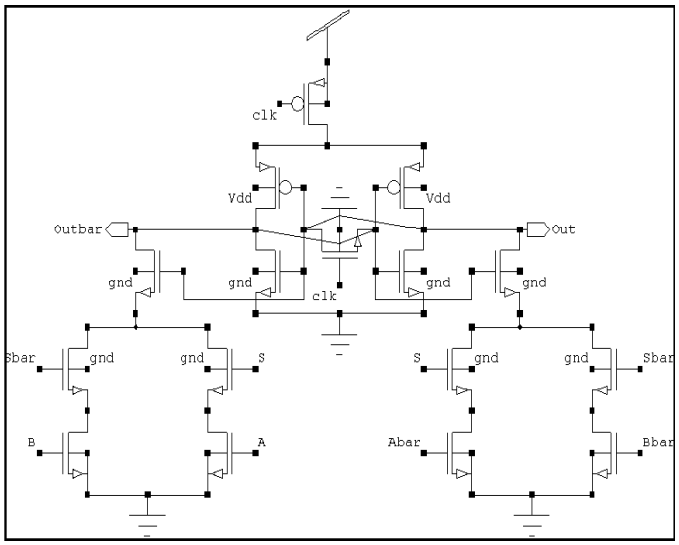

Fig. 7. Schematic of DCSL3 circuit

III. SIMULATION AND ANALYSIS

A.SIMULATION ENVIRONMENT

All the circuits have been simulated using BSIM 3V3 90nm technologies on Tanner EDA tool. All the simulations have been done on exactly same input patterns to ensuring of impartial testing environment and performed on range of voltage varying from 1.6v to 2.4v.

B.PERFORMANCE ANALYSIS

Fig. 8 depicts the power consumption vs Vdd for different 2:1 multiplexer circuits. DCSL 2 circuit implementation of 2:1 multiplex shows the least power consumption. Fig. 9 shows maximum power consumption vs Vdd and Fig. 10 shows minimum power consumption vs Vdd. Fig 11 shows delay vs Vdd for 2:1 multiplex circuit realized using different sense-amplifier logic styles. Here LCDL circuit shows least delay among all other design technique. Table 1 depicts the Power Delay Product over a range of Power Supply voltages and as it is shown in the table that DCSL1 circuit for 2:1 multiplexer shows minimum Power Delay Product for range of voltage values taken in consideration for low power circuits. Fig.12 shows Power delay Product vs. Vdd line graph for all 6 sense-amplifier logic circuit implemented for 2:1 multiplexer circuits

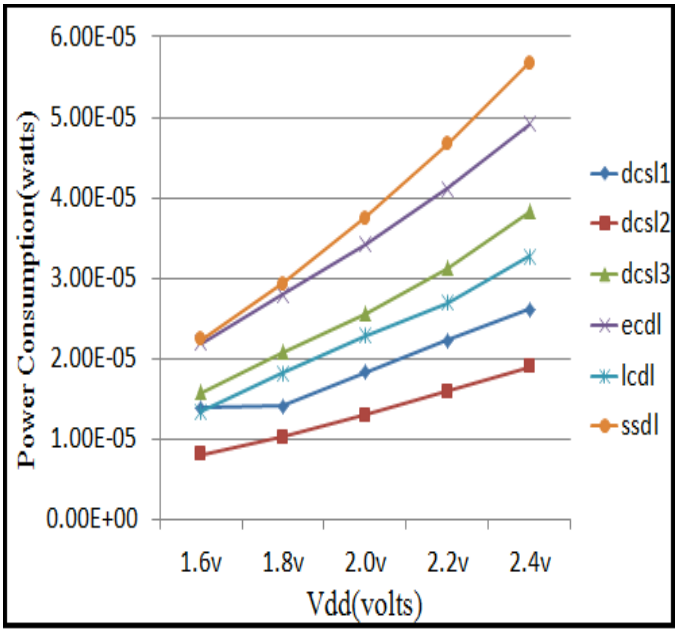

Fig. 8. Power Consumption vs Vdd for dcsl1, dcsl2, dcsl3, ecdl, lcdl, ssdl based Multiplexers circuits.

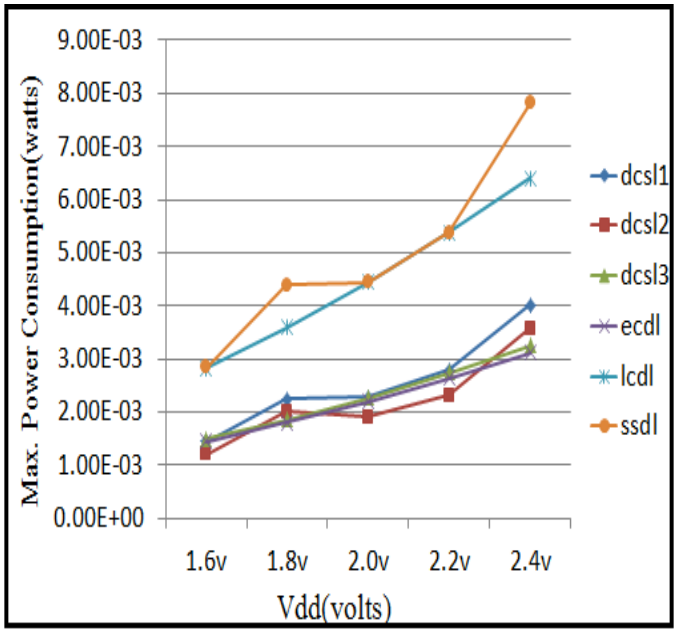

Fig. 9. Maximum Power Consumption vs Vdd for dcsl1, dcsl2, dcsl3, ecdl, lcdl, ssdl based Multiplexers circuits.

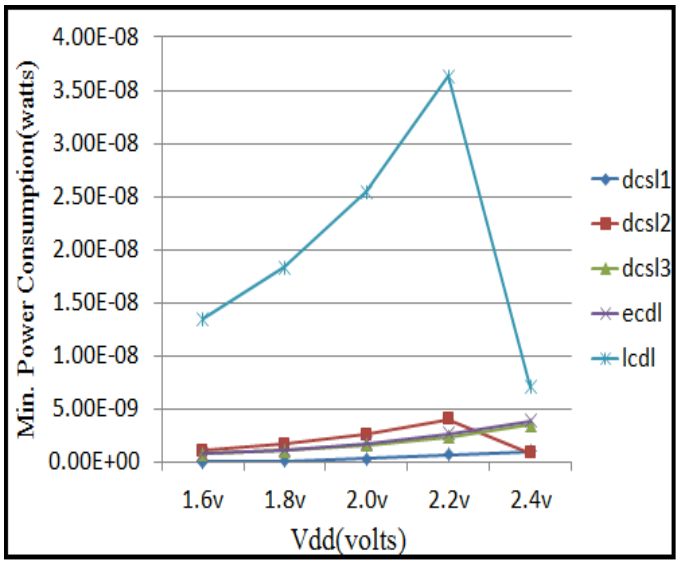

Fig. 10. Minimum Power Consumption vs Vdd for dcsl1, dcsl2, dcsl3, ecdl, lcdl based Multiplexers circuits.

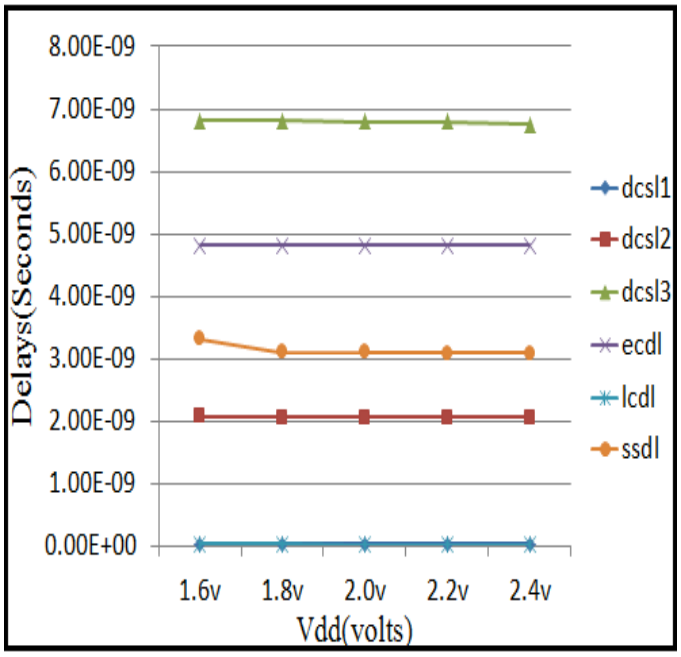

Fig. 11. Delay vs Vdd for dcsl1, dcsl2, dcsl3, ecdl, lcdl, ssdl based Multiplexer circuit.

Table 1
Power Delay Product (watt-sec) Comparison of different 2:1 Multiplex circuits.

Voltage applied	DCSL1	DCSL2	DCSL3	ECDL	LCDL	SSDL
1.6v	2.902455e-016	1.663829e-014	1.06750e-014	1.053270e-013	3.08324e-016	6.92572e-014
1.8v	3.355915e-016	2.09362e-015	1.41109e-013	1.340488e-013	3.51057e-016	9.0629e-014
2.0v	4.107194e-016	2.66157e-015	1.73359e-013	1.6391260e-013	3.904369e-016	1.160364e-013
2.2v	4.76210e-016	3.27356e-015	2.123926e-013	1.976947e-013	4.17805e-016	1.442815e-013
2.4v	5.434619e-016	3.873517e-015	2.59783e-013	2.359571e-013	4.68556e-016	1.752884e-013

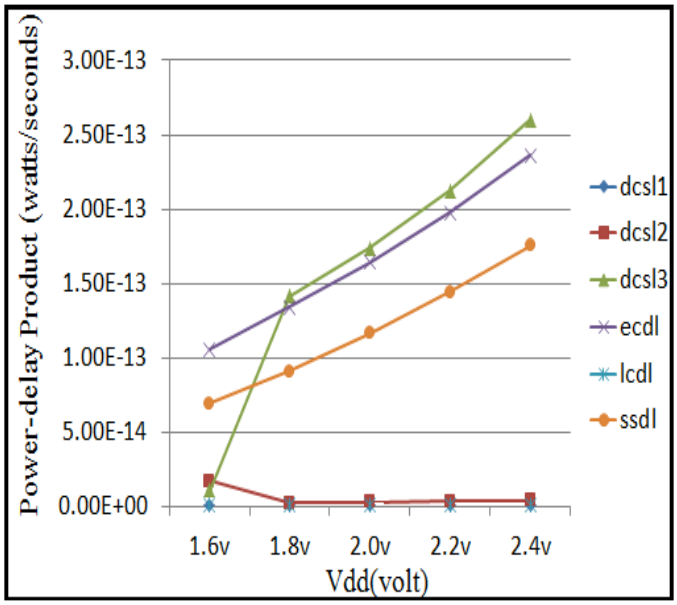

Fig. 12. Power delay product vs Vdd for dcsl1, dcsl2, dcsl3, ecdl, lcdl, ssdl of 2:1 Multiplex circuit.

IV. CONCLUSION

In this digital era, there is an enormous wide spread increase of the internet and communication system. By the survey content published in 2012 by CSC shows that by 2020 there would be 4300% increase in annual data generation [13]. To store this large amount of data, we require memory devices. Sense-amplifier circuits are specifically used for application in designing of memory cells. In this work by performing comprehensive comparison of various sense-amplifier circuit designed over the years and implemented them using 2:1 multiplex circuits. It has been concluded that Differential Current Switch Logic (DCSL) 1 is the most suitable logic circuit to design fast-speed, power efficient with reduced propagation delay memories.

REFERENCES

[1] A. P. Chandrakasan and R. W. Brodersen, *Low Power Digital CMOS Design*, Kluwer, Norwell, MA, 1995

[2] R. Zimmermann and R. Gupta, "Low-power logic styles : CMOS versus CPL", in *Proc. 22nd European Solid-State Circuits Conf.*, Neuchâtel, Switzerland, Sept. 1996, pp. 112–115.

[3] C. Piguet, J.-M. Masgonty, P. Mosch, C. Arm, and V. von Kaenel, "Low- power low-voltage standard cell libraries", in *Proc. Low Voltage – Low Power Workshop, ESSCIRC'95*, Lille, France, Sept. 1995.

[4] R. Rogenmoser, H. Kaeslin, and N. Felber, "The impact of transistor sizing on power efficiency in submicron CMOS circuits", in *Proc. 22nd European Solid-State Circuits Conf.*, Neuchâ tel, Switzerland, Sept. 1996, pp. 124–127.

[5] C. Piguet, J.-M. Masgonty, S. Cserveny, and E. Dijkstra, "Low-power low-voltage digital CMOS cell design", in *Proc. PATMOS'94*, Barcelona, Spain, Oct. 1994, pp. 132–139.

[7] T.Grotjhon and B.Hoefflinger, "ample-set differential logic (SSDL) for comlex high-speed VLSI,"JSSC, vol. SC-21, no. 2, April 1986, pp. 367-369.

[8] S.Lu "Implementation of iterative networks with cmos differential logic," JSSC, vol. 23, no. 4, Aug. 1998, pp. 147-150.

[9] S.Lu and M.Erecegovac, "Evaluation of two-summand adders implemented in ECDL CMOS differential logic," JSSC, vol. 26, no. 8, Aug. 1991, pp.1152-1160.

[10] C.Wu and K.Cheng,"Latched CMOS differential logic (LCDL) for complex high-speed VLSI," JSSC, vol. 26, no. 9, Sep. 1991, pp.1324-1328.

[11] D.Somasekhar and K.Roy, "Differential current switch logic: a low power DCVS logic family," JSSC, vol. 31, no. 7, July 1996, pp. 981-991.

[12] D.Somasekhar and K.Roy, "LVDCSL: a high fan-in, high-performance, low-voltage differential current switch logic family," IEEE Trans.VLSI, vol. 6, no. 4, Dec 1998, pp.573-577.

[13] csc.com, 'Big Data Universe Beginning to Explode', 2012. [Online]Available: http://www.csc.com/insights/flxwd/78931big_data_universe_beginning_to_explode.

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