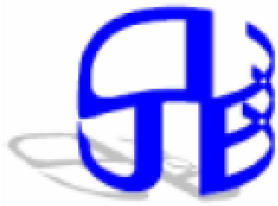

Journal of Electron Devices, Vol. 9, 20011, pp. 325-334

© JED [ISSN: 1682 -3427 ]

Journal of Electron Devices
www.jeldev.org

# Fast & Low-Power Consuming SRAM Design by Fast Precharging Using Equalizer and Sense Circuit

**Hussain Mohammed Dipu Kabir[1], Syed Bahauddin Alam**
**Bangladesh University of Engineering and Technology**
**Email: [1] dipu0506@yahoo.com**

Received 21 December 2010, accepted 30 December 2010

***Abstract*-** **This paper presents a fast and low-power Static Random Access Memory (SRAM) design. SRAM are widely used in computer systems and many portable devices. Proposed SRAM is faster because of precharging at a desired voltage. For the most recent CMOS technologies leakage power dissipation has become a major concern. According to the International Technology Roadmap for Semiconductors (ITRS), leakage power dissipation may eventually dominate total power consumption as technology feature sizes shrink. To reduce overall power consumption we have to concern on both static and dynamic power consumption. Firstly, an equalizer with sense circuit was used to precharge bit-lines near voltage ($V_{DD}$ - $V_t$). It reduces both static and dynamic power consumption. Aspect ratio of equalizer is high for fast precharging. Though we are precharging at desired voltage circuit is simpler than conventional SRAM.**

***Index Terms*—SRAM, Equalizer, Precharge, Sense circuit, Read, Write.**

## I. INTRODUCTION

Static Random Access Memory is a type of RAM used in various electronic applications including toys, automobiles, digital devices and computers. Static RAM or SRAM only holds its contents while power is applied [1]. It differs from dynamic RAM is that DRAM must use refresh cycles to keep its contents alive. SRAM holds data/memory as a static image as indicated by the name, until written over or lost from powering down.

Static Random Access Memories (SRAMs) are commonly embedded into system-on-chip (SoC) designs to store programs and data [2], [3]. Many efforts have been made to improve the efficiency of the SRAM. Improvements are reducing area, static power consumption, dynamic power consumption, propagation delay etc. [4], [5]. Power consumptions and area can be easily minimized by reducing process parameter λ. This processes parameter is reducing day by day and this reduction becomes saturated. For faster circuits static power consumption is higher. For faster SRAM design dual threshold is used in following papers [6], [7]. Main problem of these SRAM circuits is higher leakage of low $V_t$ devices. Higher leakage results in higher static power consumption. For designing static circuits static power consumption is important. So, devices of nominal threshold (Low threshold) should be avoided.

Replica column schemes have been frequently used in SRAM for word-line pulse and sense amplifier controls to reduce the timing skew in data-sensing for synchronous SRAMs [8]-[11] across various process, voltage and temperature (PVT) conditions. Bit-lines needed to be charged before read and write operation. Before reading and writing operation both bit-lines are charged to $V_{DD.}$ Row select or column select is high depending on read and write operation. A long bit-line precharge time in the write operation and a wide word-line pulse width in the read operation consume most of the cycle time, especially for large-capacity SRAMs. For this dual-mode self-timed technique is introduced in [12]. 4T RAM cells consume less power than 6T cells [13] but 4T cells are appropriate for only designing DRAM. 4T cells are unable to store 0 for long period [14].

There has been a significant increase in the demand for low power and high performance digital VLSI circuits. Designers are implementing very high-order scaling of both device dimensions and supply voltage [15]. Due to growing requirement of memory large number of memory cells are placed in a single column. The main problem of larger memory cells is the large bitline capacitance. Large capacitance corresponds to huge dynamic power. Relatively much smaller power is consumed when bitlines are precharged near to Vinv. Major part of dynamic power corresponds due to precharging. When no power is consumed due to precharge dynamic power consumption reduces by a high factor.

Proposed SRAM is simpler than conventional SRAM cells. Operation of proposed cell is faster and low power

consuming. Both static and dynamic power is reduced in proposed SRAM. We can say proposed cell gives all improvement that we need. They are reducing area, reducing dynamic and static power and reducing propagation delay.

## II. Mathematical Background

The proposed system based on following concepts-

- Dynamic dissipation
- Sub-threshold leakage current
- Inversion voltage

Equation for dynamic power dissipation is as equation (1),

$$P_g = \frac{1}{2} C_L . \Delta V^2 \qquad (1)$$

Vo = Logic Voltage Swing [14]

From this equation dynamic power reduces in reducing voltage swing. When voltage swing reduces by a factor of 2 power consumption reduces by factor of 4.

Equation for sub-threshold current is as equation (2), [16], [17]-

$$I_D(sub) = I_s e^{(\frac{e(V_{gs}-V_t)}{kT})} . [1 - e^{(\frac{-eV_{ds}}{kT})}] \qquad (2)$$

From this equation leakage current reduces slightly in deducing $V_{ds}$. Though this reduction is very small we are getting it as a bi-product. Static current of any CMOS circuit is equal to sum of static currents of all PMOS or NMOS device. That means sum of current through NMOS devices is equal to sum of all current through PMOS devices. As NMOS leakage current is reduced static power is reduced.

Inversion voltage is an important factor for designing faster and low power-consuming circuits. When SRAM cell's sense is switched to high from low, both Bit and Bit' is high (approx. $V_{dd}$) with a slight difference. Sense amplifier increases this voltage difference and makes one high and another low. To perform this operation an intermediate condition arises. Both voltages of Bit and Bit' reduces at first because both PMOS of sense circuit is OFF and all NMOS are ON. One voltage reduces slightly faster then other voltage because $V_{gs}$ of two NMOS are slightly different. When one voltage reaches below inversion voltage, their logic is determined and one voltage reduces and another voltage goes to high.

When we are calculating delay, counting should be started when column select is high for write operation and when row select is high for read operation. Counting should be stopped when one bit-line has voltage lower than inversion voltage and another bit-line has voltage higher than inversion voltage.

Fig. 1 shows timing diagram when bit-lines are precharged to $V_{DD}$ and Fig. 2 shows timing diagram when bit-lines are precharged to ($V_{DD} - V_t$). Curves are plotted using Microwind software.

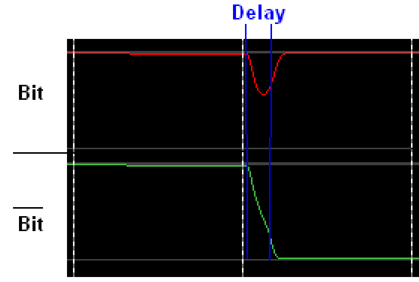


Fig 1: Timing Diagram when precharged to $V_{DD}$.

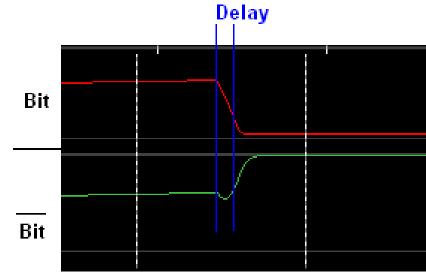


Fig 2: Timing Diagram when precharged to ($V_{DD} - V_t$).

According to these figure both Bit and Bit' are precharged near inversion voltage circuit will be faster and low dynamic power consuming.

The sub-threshold propagation delay [18] [20] with a load capacitance Cg is defined as eqn. (3).

$$t_d = \frac{kC_g V_{DD}}{I_o e^{(V_{gs}-V_t)/nV_{th}}} \qquad (3)$$

k is the delay fitting parameter.

## III. PROPOSED SYSTEM

Fig. 3 shows the arrangement of proposed SRAM cell. Normally Bit and $\overline{\text{Bit}}$ are precharged using PMOS and precharged to $V_{DD}$. PMOS passer good 1 but poor 0 and for this it is used for precharging to high voltage. In proposed system a PMOS equalizer is used because voltages of bit-lines after precharging is higher than $V_{DD}/2$.

The figure contains one bit memory cell for explaining operation. After completing one read or write (R/W) operation sense is low and bit-lines contains previous value. Then both bit-lines are precharged using Equalizer (EQ). One PMOS pass transistor is used as Equalizer. When precharge is high bit-lines are precharged to about $V_{DD}/2$. As threshold voltage of PMOS is lower than $V_{DD}/2$ both PMOS will be ON and voltage of both bit-lines will become ($V_{DD}$ - Vt), within a very short time. This voltage will rise slightly after some period due to sub-threshold leakage current of PMOS transistors.

In this proposed system inversion voltage of sense circuit is near to ($V_{DD} – V_t$) for reducing dynamic power and delay. Inversion voltage increases in increase of $\beta_n/\beta_p$. For NMOS and PMOS of equal size this ratio is greater than 1 and due to this ratio inversion voltage is higher than $V_{DD}/2$; near to ($V_{DD} – V_t$).

Fig. 4 presents the voltages of bitlines during precharge. After one R/W operation one of bitline is high and another is low. When Equalizer MOS is ON both voltages are charged to VDD/2 and both PMOSes of sense circuit are Turned ON. For this voltage of bitlines increases slightly. In this case we used VDD = 1.2v and Vt _ 0.3v and according to figure voltage of precharge bitlines become approximately 0.92v at stable condition.

*A. Proposed Write operation*

Following steps should be performed sequentially for writing data to cell.
* De-activating Precharge
* Activating column select
* Activating sense
* Achieving row select
* De-activating row select, column select and sense
* Activating Precharge

*B. Proposed Read operation*

Following steps should be performed sequentially for reading data from cell.
* De-activating Precharge
* Activating row select
* Activating sense
* Achieving column select
* De-activating row select, column select and sense
* Activating Precharge

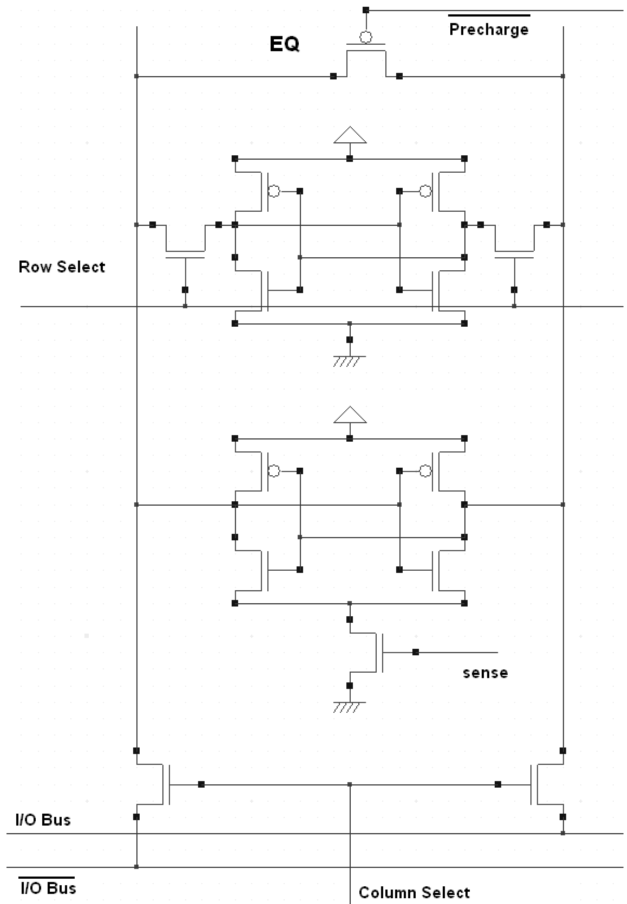

Fig. 3: Proposed SRAM cell

*C. Adjustment of inversion voltage*

Inversion voltage of an inverter is the voltage over which voltage input is treated to be logic high and under which voltage input is treated to be logic low.In this proposed system inversion voltage of sense circuit is near to ($V_{DD}$-$V_t$) for reducing dynamic power and delay. Inversion voltage increases in increase of _n=_p. For NMOS and PMOS of equal size this ratio is greater than 1 and due to this ratio inversion voltage is higher than VDD/2. In conventional system size of PMOS is made 2.5 times larger than size of NMOS to make Vinv = VDD=2 In proposed system size of NMOS is 2.5 times larger than size of PMOS. For this inversion voltage is very near to ($V_{DD}$-$V_t$).

As bit-lines are precharged previously near inversion voltage no time is consumed for precharging. For write operation when column select is activated input low changes voltage of corresponding bit-line below inversion voltage within a short time. Then sense amplifier is activated for driving memory cell inverters. Time-gap between activating row select and column select for read/write operation is reduced in proposed system. Time needed for driving cell inverters is same to conventional system.

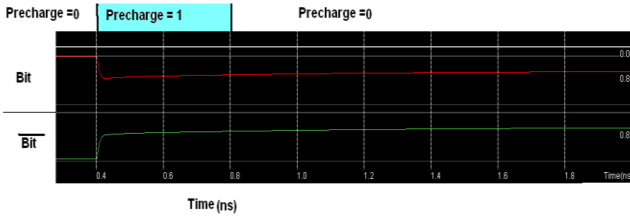


Fig. 4. Precharging near to ($V_{DD}$ - $V_t$) using Equalizer

## IV. SIMULATION RESULT

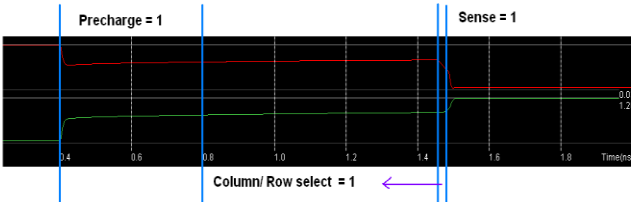


Fig. 5. Charging of bitlines according to input (data-line or SRAM cell) in proposed method

Fig. 5 shows the complete wave-shape of charging bit-lines. Precharge is set for 0.2ns at t = 0.4ns. Column-select (for write operation) row-select (for read operation) is set for .03ns at t = 1.45ns. Sense amplifier is turned ON at t = 1.48ns. Bitlines are precharged at $V_{DD}$- $V_t$ as bitlines are equalized during precharge. At t = 1.45ns row/column select line is turned ON and bitlines are getting voltage. Within 0.03ns one value of bitlines is lower than inversion voltage and another value is higher than inversion voltage. At t = 1.48ns sense amplifier is turned ON. The work of sense amplifier is to differentiate two voltages of slight difference in value.

The proposed precharging is faster and low power consuming. Conventionally after achieving column or row select both voltages of bitlines are very near to VDD. When sense is turned high both NMOS are turned ON. Both transistors draw a high current. One of them draws higher current than other one according to eqn. (4).

$$I_d(sat.) \propto (V_{gs} - V_t)^2 \tag{4}$$

Both voltages decrease. One voltage decreases faster than other one due to this current difference. Bitline voltages are set after a larger period as shown in Fig. 1.

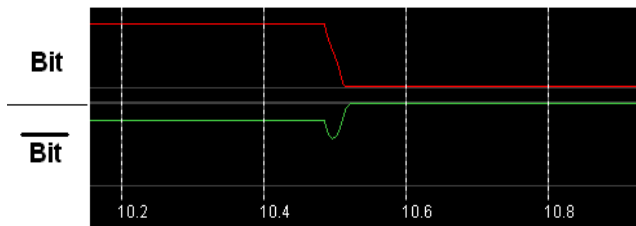


Fig. 6. Situation while read/write operation is performed after long time precharging

## V. RESULT ANALYSIS AND WORST CASE SCENARIO

### *A. Worst case*

Capacitances of bitlines are much larger than capacitance of unit cell memory. When R/W operation is performed long time after precharging, bitlines become precharged near VDD. Due to low capacitance of memory cell, cell may cause very small voltage difference between bitlines. Sense amplifier differentiates these voltages. In this case charging of bitlines according to data of unit cells is similar to the operation of conventional SRAM cells. It is causing larger delay and consuming larger power. This phenomena is shown in Fig. 6.

### *B. Solution*

As both PMOS are ON after precharging voltages of bitlines increases with time. To solve this problem precharging should be performed just before R/W operation. Fig. 7 shows the complete waveshape of corrected system. In this corrected system equalizer is set 0.05ns before read/write operation. In this figure equalizer is high at 10.4ns, row select/column select is high at t = 10.45ns and sense amplifier is activated at t = 10.48ns. Voltages of bitlines reaches to their final value at t = 10.51ns(approx.).

To overcome the worst case scenario it is needed to change the read and write operations. Corrected read/write operations should be as followed.

*1) Corrected Write Operation:* Following steps should be performed sequentially for writing data to cell.

*Activating Precharge for 0.05ns(small period)
*De-activating Precharge
* Activating column select
* Activating sense
* Achieving row select
* De-activating row select, column select and sense

*2) Corrected Read operation:* Following steps should be performed sequentially for reading data from cell.

*Activating Precharge for 0.05ns(small period)
*De-activating Precharge
* Activating row select
* Activating sense
* Achieving column select
* De-activating row select, column select and sense

The difference between corrected operation and primarily proposed operation is the time of precharging. Initially it is proposed that precharge should be performed after R/W operation. In corrected proposal precharge should be performed (small time) before R/W operation.

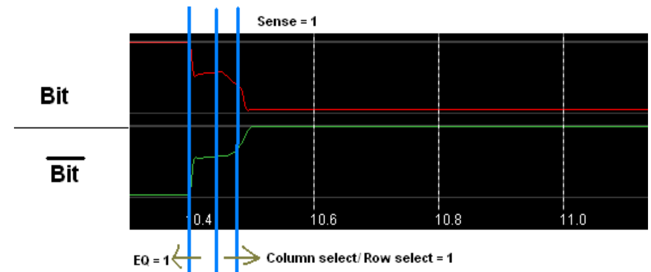

Fig. 7. Solution of the problem

## VI. COMPARISON

Table I shows comparison among various proposed SRAM cells with present SRAM cell. A lot of advancement for SRAM has proposed and implemented. The proposed system in compared with conventional SRAM cell, with [7] and [20]. Quite bitline architecture [20] is similar to proposed technique in prospect of precharging, but they used only equalizer for precharging. Quite bitline architecture presents a low static-power consuming SRAM; area of SRAM is slightly lower as two PMOS are not needed.

In proposed technique dynamic power consumption is lowest and R/w speed is highest. No extra circuitry is added for this improvement. Average R/W time for Quite-bitline architecture is 1.8ns; conventional SRAM is also needed 1.8ns for R/W. In proposed system this time is equal to 10.51ns - 10.40ns = 0.11ns (0.05ns for precharging, 0.03ns for driving bitlines using unit memory cell, 0.03ns for sense amplifier to charge bitlines).

TABLE I
COMPARISON

| | Static Power | Dynamic Power | R/W Speed | Area |
|---|---|---|---|---|
| Conventional SRAM | Average | Average | Average | Average |
| Dual Threshold | Higher | Lower | Higher | Slightly Higher |
| Quiet Bitline | *Lowest* | Average | Average | Slightly Lower |
| Proposed System | Lower | *Lowest* | *Highest* | Slightly Lower |

## CONCLUSION

In this paper a fast & low-power consuming SRAM is designed. At first we proposed a new precharge technique with a new precharge arrangement. The technique is efficient for reducing power consumption, reducing speed of R/W operation, reducing delay and reducing area of SRAM. In analyzing worst case scenarios, we got an unexpected situation for which proposed system is not working efficiently in delay minimization and dynamic power minimization. We proposed a corrected system for reducing dynamic power and delay.

## REFERENCES


[1] B. Prince, Semiconductor Memories. New York: Wiley, 1991.

[2] K. Takeda, Y. Aimoto, N. Nakamura, H. Toyoshima, T. Iwasaki, K. Noda, K. Matsui, S. Itoh, S. Masuoka, T. Horiushi, A. Nakagawa, K. Shimogawa, and H. Takahashi, "A 16-Mb 400-MHz loadless CMOS four-transistor SRAM macro," IEEE J. Solid-State Circuits, vol. 35, pp. 1631–1640, Nov. 2000.

[3] S.-M. Yoo, J. M. Han, E. Hag, S. S. Yoon, S.-J. Jeong, B. C. Kim, J.-H. Lee, T.-S. Jang, H.-D. Kim, C. J. Park, D. H. Seo, C. S. Choi, S.-I. Cho, and C. G. Hwang, "A 256 M DRAM with simplified register control for low power self refresh and rapid burn-in," in Symp. VLSI Circuits Dig. Tech. Papers, 1994, pp. 85–86.

[4] N. Karmakar, M. Z. Sadi, M. K. Alam and M. S. Islam, "A Novel Dual Sleep Approach to Low Leakage and Area Efficient VLSI Design", IEEE-RSM Proc. 2009, Kota Bahru, Malaysia.

[5] Y. Morita, H. Fugiwara, H. Noguchi, Y. Iguchi, "Improving the Speed and Power of Compilable SRAM using Dual-Mode Self-Timed Technique", IEICE Trans. Electron, vol. E90-C, no. 10, October 2007.

[6] K. Itoh, A. R. Fridi, A. Bellaouar, and M. I. Elmasry, "A deep sub-V, single power-supply SRAM cell with multi-V , boosted storage node and dynamic load," in Symp. VLSI Circuits Dig. Tech. Papers, June 1996, pp. 132–133.

[7] C. C. Wang, P. M. Lee, and K. L. Chen- "An SRAM Design Using Dual Threshold Voltage Transistors and Low-Power Quenchers", IEEE Journal of solid-state circuits, vol. 38, no. 10, pp. 1712-1720,October 2003

[8] K. Ando et. al., "A 0.9-ns-access, 700MHz SRAM macro using a configurable organization technique with an automatic timing adjuster, "IEEE Symp. VLSI Circuits, Digest of Technical Papers, pp. 182–183, 1998

[9] B. S. Amrutur and M. A. Horowitz, "A Replica Technique for Wordline and Sense Control in Low-Power SRAM's," IEEE Journal of Solid- State Circuits, vol. 33, no 8 „ pp. 1208-1219, Aug. 1998.

[10] Kenichi Osada et al., "Universa-Vdd 0.65-2.0-V 32-kB Cache Using a Voltage-Adapted Timing-Generation Scheme and a Lithographically Symmetrical Cell," IEEE Journal of Solid-State Circuits, vol.36, no 11 „ pp. 1738-1744, Nov. 2001.

[11] M.-F. Chang, K.-A. Wen and D.-M. Kwai, "Supply and substrate noise tolerance using dynamic tracking clusters in configurable memory designs," in Proc. IEEE Int'l Symp. Quality Electronic Design, pp. 297- 302, Mar. 2004.

[12] M. F. Chang, S. M. Yang, K. T. Chen, H. J. Liao and R. Lee" Improving the Speed and Power of Compilable SRAM using Dual-Mode Self-Timed Technique", IEEE-2007, pp. 57-60.

[13] A. A. Mazreah , M. R. Sahebi, M. T. Manzuri and S. J. Hosseini, "A Novel Zero-Aware Four-Transistor SRAM Cell for High Density and Low Power Cache Application", International Conference on Advanced Computer Theory and Engineering, pp. 571-575, 2008

[14] D. A. Puncknell, K Eshraghian, "Basic VLSI Design", 3rd edition 2009-2010.

[15] Valmiki Mukherjee, Saraju P. Mohanty, Elias Kougianos,"Gate Leakage Current Analysis in READ/WRITE/ IDLE States of a SRAM Cell"in Region 5 Conference, 2006 IEEE, pp. 196 - 200 , 7-9 April 2006.

[16] D. A. Neamen, Semiconductor Physics and Devices, Basic Principles, 3rd edition 2003.

[17] B. H. Calhoun and A. Chandrakasan,"Analyzing Static Noise Margin for Sub-threshold SRAM in 65nm CMOS", in Solid-State Circuits Conference, 2005. ESSCIRC 2005. Proceedings of the 31st European, pp. 363 - 366, 12-16 Sept. 2005 .

[18] B. H. Calhoun, A. Wang, A. Chandrakasan, Modeling and Sizing for Minimum Energy Operation in Subthreshold Circuits, IEEE Journal of Solid-State Circuits, Vol. 40, No. 9, pp. 1178-1786, Sep. 2005.

[19] Moradi, F. Wisland, D.T. Aunet, S. Mahmoodi, H. T. V. Cao,"65NM sub-threshold 11T-SRAM for ultra low voltage applications"in SOC Conference, 2008 IEEE International, pp. 113 - 118 , 17-20 Sept. 2008.

[20] S. P. Cheng, S. T. Hung, "A Low-Power SRAM Design Using Quiet-Bitline Architecture" IEEE International Workshop on Memory Technology, Design, and Testing (MTDT05), pp. 135 - 139 , Taipei, 5-5 Aug. 2005.