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An Analytical model of the Bulk-DTMOS transistor

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ABSTRACT: In a Bulk-DTMOS transistor, source substrate junction is slightly forward biased due to which few mobile charge carriers are also present in source substrate depletion region. Conventional SPICE models are based on complete depletion approximation which is more valid for reverse biased p-n junctions. Therefore they are not appropriate for simulating circuits implemented with Bulk-DTMOS transistors. In this paper an analytical model for Bulk-DTMOS transistor is proposed by taking into account the presence of mobile charge carriers in source substrate junction. Analytical results of the proposed model are compared with SPICE model and results indicate that the proposed model can be used for more accurate simulation of Bulk-DTMOS based circuits.

Keywords: Modeling, Microelectronics, Bulk-DTMOS, body bias

I. INTRODUCTION: CMOS circuits have scaled downward aggressively in each technology generation to achieve higher integration density and performance. With the current nanoscale technology trends in CMOS circuits, effective solutions have to be sought to reduce leakage power which is expected to dominate the chip's total power consumption in the near future. These solutions must be sought in all design abstraction levels: system and architectural level, circuit level, and process/device level. Body biasing technique is a circuit level approach to reduce leakage in scaled CMOS circuits. Dynamic threshold MOSFET (DTMOS) transistor utilizes dynamic body bias because in DTMOS, substrate (or body) and gate of MOSFET are tied together as shown in fig. 1, therefore input gate voltage forward biases the source substrate junction and owing to the body effect threshold voltage (V_{th}) decreases in the ON state and when the gate is turned off, V_{th} returns to its original high value in equilibrium. DTMOS has proven to be an excellent alternative for the implementation of ultra-low power and high-performance circuits. This technique is popular in both Silicon-On-Insulator (SOI) and bulk CMOS technology. DTMOS in SOI technology was introduced in 1994. In 1996, aggressive technological improvements led to successful fabrication of first bulk DTMOS [8, 9] whose current representatives show impressive figures of merit regarding gate delay-power consumption products, well above those of conventional CMOS. Since the first introduction of DTMOS in 1994, many novel and interesting proposals have been made regarding this device for both SOI and Bulk CMOS technology but the modeling in bulk technology is still in early stage.

In most of the circuit implementation SPICE models are used for simulation. SPICE models are based on the depletion approximation, which are valid for reverse biased p-n

junctions. As in DTMOS source substrate junction is slightly forward biased, therefore due to presence of mobile charge carriers models based on depletion approximation are not appropriate for modeling of DTMOS and may introduce errors in DTMOS parameters like mobility, threshold voltage etc. [6]. The remainder of the paper proceeds as follows. In section II analytical model for Bulk DTMOS transistor is developed. In section III SPICE simulation and analytical results of the proposed model are given. Conclusions are summarized in section IV.

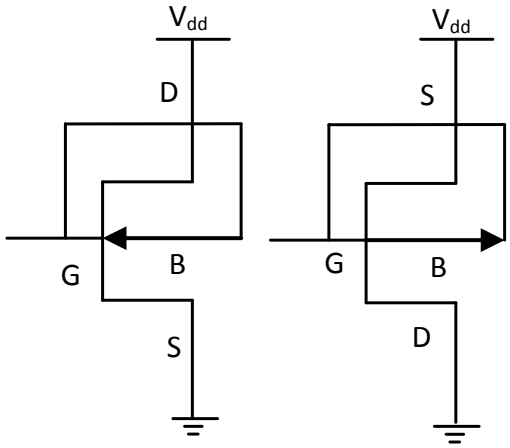

Fig.1: NMOS & PMOS transistors based on DTMOS circuit Topology

II. The Proposed Analytical Model for Bulk-DTMOS transistor

Generally MOSFETs used in circuit applications must be biased with negative or zero V_{BS} in order to suppress the leakage current flowing from source to substrate [1].

From threshold voltage equation of MOSFET we can see that

$$V_{th} \propto \sqrt{(2\emptyset_F - V_{BS})} \tag{1}$$

Models that are currently available in SPICE are not suitable for DTMOS as they are suitable for reverse or zero biasing of V_{BS} and are based on depletion-region approximation within the source (-channel)-substrate depletion layer[10,11]. For all the values of $V_{BS} > 2\emptyset_F$ this term becomes meaningless and circuit simulation program fails to converge and thus large errors can be expected for more positive values of V_{BS}. To avoid this problem of non convergence MOS models use an approximate term to replace eq.(1).For example

PSPICE Model

$$\sqrt{(2\emptyset_F - V_{BS})} \cong \frac{\sqrt{(2\emptyset_F)}}{\left(1+0.5\frac{V_{BS}}{2\emptyset_F}\right)} \tag{2}$$

BSIM Model

$$\sqrt{(2\emptyset_F - V_{BS})} \cong \sqrt{(2\emptyset_F)} \quad (3)$$

These approximations may cause significant errors for positive V_{BS} biases. Any MOSFET has an intrinsic BJT embedded in its structure as shown in figure 2.

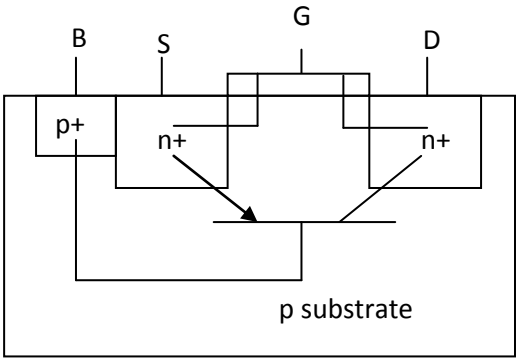

Fig.2: Intrinsic BJT embedded in MOSFET structure

It is assumed that the MOSFET current flows close to the channel surface and bulk parasitic BJT current flows through the bulk region, therefore the interaction between these two currents can be neglected. Hence DTMOS, to the first order approximation, can be considered as parallel combination of surface MOSFET and bulk parasitic BJT embedded in MOSFET's structure. Thus the total DTMOS current I_{DTMOS}

$$I_{DTMOS} = I_{BJT} + I_{MOSFET} \quad (4)$$

The Pao sah result has been used as a starting point in deriving approximate closed form relationship for bulk-DTMOS transistor as Pao-Sah formulation is continuously valid in all biasing regions including weak inversion and saturation and the model is valid when source substrate junction is forward biased.

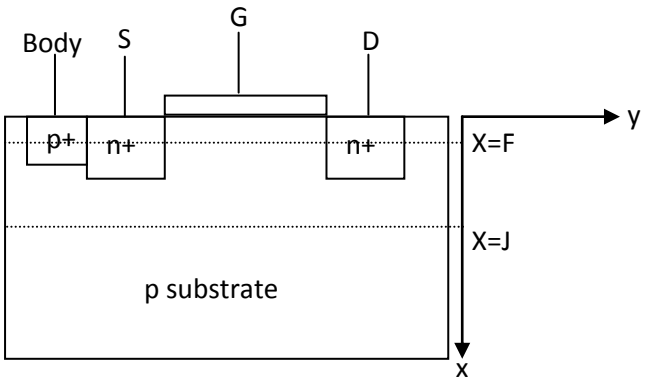

Fig.3: N-channel MOSFET structure

The Pao-Sah result [4, 5] for the drain current I_D flowing in an n-channel MOSFET can be written as

$$I_D = \frac{Z\mu_n C_o}{2L}\left(\frac{K_s\, x_o}{K_o\, L_D}\right)\left(\frac{KT}{q}\right)^2 \int_{U_{Source}}^{U_{Drain}} d\xi \int_{U_F}^{U_{surface}} \frac{e^{U-U_F-\xi}}{F(U,U_F,\xi)}\, dU \tag{5}$$

q is electronic charge, Z is channel width, L is channel length, μ_n is electron effective mobility in the surface channel, L_D is intrinsic Debye length, K is Boltzmann's constant, T is temperature, C_O is oxide capacitance per unit area = $\frac{K_o\,\epsilon_0}{x_o}$, K_O is oxide dielectric constant, x_o is oxide thickness, ϵ_o is permittivity of free space, K_S is semiconductor dielectric constant. Function F is given as

$$F(U,U_F,\xi) \equiv \left[e^{U_F}(e^{-U}+U+1)+e^{-U_F}\left(e^{U-\xi}-U-e^{-\xi}\right)\right]^{\frac{1}{2}} \tag{6}$$

where U is normalized electrostatic potential in the semiconductor, U_{Source} is value of U at y=0 that is at source, U_{Drain} is value of U at y=L that is at drain, $U_{surface}$ is value of U at x=0 that is at surface, U_F is value of U at x=F below oxide semiconductor interface close to channel. y is coordinate parallel to oxide surface of MOSFET and x is coordinate directed into the semiconductor with x=0 at the oxide semiconductor interface as shown in figure 3.Electrostatic potentials in the semiconductor are given as

$$U = \frac{E_{i(bulk)} - E_{i(x)}}{KT} \tag{7}$$

$$U_{Drain} = \frac{V_{Drain}}{\left(\frac{KT}{q}\right)} \tag{8}$$

$$U_{Source} = \frac{V_{Source}}{\left(\frac{KT}{q}\right)} \tag{9}$$

$$U_F = \frac{E_{i(bulk)} - E_F}{KT} = ln\left(\frac{N_A}{n_i}\right) \tag{10}$$

where V_{Drain} is Drain voltage, V_{Source} is Source Voltage. Ideal device gate voltage i.e. i.e. gate voltage less the flat band voltage is given as

$$V'_{G=}\frac{KT}{q}\left[U_{surface}+\left(\frac{K_s\,x_o}{K_o\,L_D}\right)F(U_{surface},U_F,\xi)\right] \quad (11)$$

$U_{surface}$ can be obtained by solving (11) iteratively. Gate electrostatic potential as given as

$$U_{Gate}=\frac{V'_G}{\left(\frac{KT}{q}\right)} \quad (12)$$

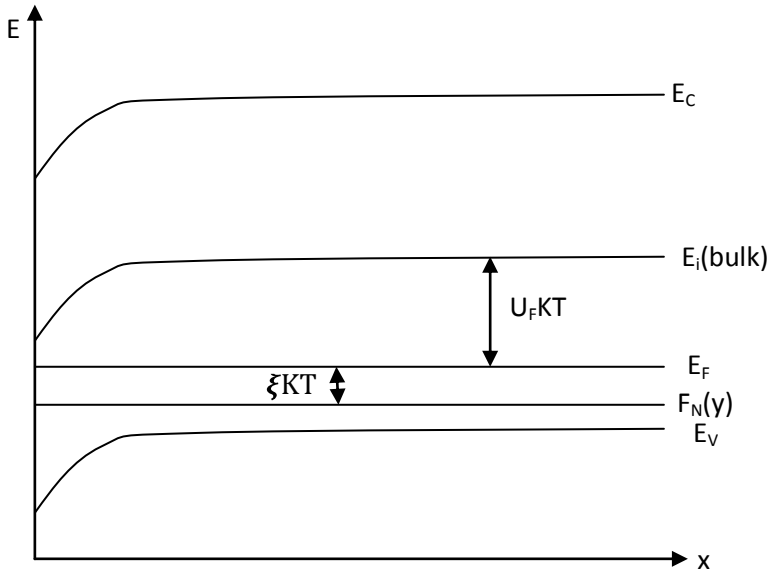

Fig.4: Band diagram of N-channel MOSFET

ξ is given as

$$\xi=\frac{E_F-F_N(y)}{KT} \quad (13)$$

E_i(bulk) is intrinsic Fermi energy level in bulk of semiconductor, E_F is bulk Fermi energy
F_N(y) is the electron quasi-Fermi level in the surface channel, N_A is bulk acceptor doping, n_i is intrinsic carrier concentration

The double integral Pao-Sah equation (5) can be evaluated numerically. However utilizing Brew's charge sheet approximation [12] one can reach an analytical formula for the drain current. All the electrons are considered to lie inside the inversion layer which is a sheet of infinitesimal thickness (considered zero) just below the gate oxide. But for DTMOS model

Brew's charge sheet approximation cannot be used as this approximation implies that the depletion region is free of electrons whereas in DTMOS case some electrons are present due to slight forward bias of source substrate junction.

Pao-Sah equation gives the value of total current which is located close to the silicon-oxide interface. In DTMOS as source-body junction is forward biased and electrons are injected from source into the bulk, therefore these injected electrons also contribute total current. To take into account the effect of injected electrons, the limits of integral should be changed as shown in following equation.

$$I_D = \frac{Z\mu_n C_o}{2L}\left(\frac{K_s\, x_o}{K_o\, L_D}\right)\left(\frac{KT}{q}\right)^2 \int_{U_{Source}}^{U_{Drain}} d\xi \int_{U_J}^{U_{surface}} \frac{e^{U-U_F-\xi}}{F(U,U_F,\xi)}\, dU \tag{14}$$

where U_J is value of U at x=J below oxide semiconductor interface considering depletion region depth also and hence injected electrons as shown in figure 3. Adding and subtracting a term in the numerator of (14) we get

$$I_{DTMOS} = \frac{Z\mu_n C_o}{2L}\left(\frac{K_s\, x_o}{K_o\, L_D}\right)\left(\frac{KT}{q}\right)^2 \left[\int_{U_{Source}}^{U_{Drain}} d\xi \int_{U_J}^{U_{surface}} \frac{e^{U-U_F-\xi}-e^{-U_F-\xi}+e^{-U_F-\xi}}{F(U,U_F,\xi)}\, dU\right] \tag{15}$$

i.e.

$$I_{DTMOS} = \frac{Z\mu_n C_o}{2L}\left(\frac{K_s\, x_o}{K_o\, L_D}\right)\left(\frac{KT}{q}\right)^2 \left[\int_{U_{Source}}^{U_{Drain}} \int_{U_J}^{U_{surface}} \frac{e^{U-U_F-\xi}-e^{-U_F-\xi}}{F(U,U_F,\xi)}\, dU\, d\xi + \int_{U_{Source}}^{U_{Drain}} \int_{U_J}^{U_{surface}} e^{-U_F-\xi}\, dU\, d\xi\right] \tag{16}$$

Changing the integration over U to x we get

$$I_{DTMOS} = \frac{Z\mu_n C_o}{2L}\left(\frac{K_s\, x_o}{K_o\, L_D}\right)\left(\frac{KT}{q}\right)^2 \left[\int_{U_{Source}}^{U_{Drain}} \int_{U_J}^{U_{surface}} \frac{e^{U-U_F-\xi}-e^{-U_F-\xi}}{F(U,U_F,\xi)}\, dU\, d\xi + \int_{U_{Source}}^{U_{Drain}} \int_{0}^{x_J} e^{-U_F-\xi}\, dx\, d\xi\right] \tag{17}$$

i.e.

$$I_{DTMOS} = \frac{Z\mu_n C_o}{2L}\left(\frac{K_s\, x_o}{K_o\, L_D}\right)\left(\frac{KT}{q}\right)^2 \left[\int_{U_{Source}}^{U_{Drain}} \int_{U_J}^{U_{surface}} \frac{e^{U-U_F-\xi}-e^{-U_F-\xi}}{F(U,U_F,\xi)}\, dU\, d\xi + e^{-U_F} \int_{U_{Source}}^{U_{Drain}} \int_{0}^{x_J} e^{-\xi}\, dx\, d\xi\right] \tag{18}$$

i.e.

$$I_{DTMOS} = \frac{Z\mu_n C_o}{2L}\left(\frac{K_s\, x_o}{K_o\, L_D}\right)\left(\frac{KT}{q}\right)^2 \left[\int_{U_{Source}}^{U_{Drain}} \int_{U_J}^{U_{surface}} \frac{e^{U-U_F-\xi}-e^{-U_F-\xi}}{F(U,U_F,\xi)}\, dU\, d\xi + e^{-U_F}\, x_J\, (e^{-U_S} - e^{-U_D})\right] \tag{19}$$

i.e.

$$I_{DTMOS} = \left[\frac{Z\mu_n C_o}{2L}\left(\frac{K_s\, x_o}{K_o\, L_D}\right)\left(\frac{KT}{q}\right)^2 \int_{U_{Source}}^{U_{Drain}} \int_{U_J}^{U_{surface}} \frac{e^{U-U_F-\xi}-e^{-U_F-\xi}}{F(U,U_F,\xi)}\, dU\, d\xi\right] + \left[\frac{Z\mu_n C_o}{2L}\left(\frac{K_s\, x_o}{K_o\, L_D}\right)\left(\frac{KT}{q}\right)^2 e^{-U_F}\, x_J\, (e^{-U_{Source}} - e^{-U_{Drain}})\right] \tag{20}$$

As Intrinsic Debye length $L_D = \frac{KT\epsilon_S}{2q^2 n_i}$ (21)

therefore

$$\left[\frac{Z\mu_n C_o}{2L}\left(\frac{K_s x_o}{K_o L_D}\right)\left(\frac{KT}{q}\right)^2 e^{-U_F} x_J \left(e^{-U_{Source}} - e^{-U_{Drain}}\right)\right] = \left[\frac{Z\mu_n C_o}{L}\left(\frac{K_s x_o}{K_o}\right) KT\, L_D (n_i e^{-U_F}) x_J \left(e^{-U_{Source}} - e^{-U_{Drain}}\right)\right]$$

i.e.

$$\left[\frac{Z\mu_n C_o}{2L}\left(\frac{K_s x_o}{K_o L_D}\right)\left(\frac{KT}{q}\right)^2 e^{-U_F} x_J \left(e^{-U_{Source}} - e^{-U_{Drain}}\right)\right] = \left[\frac{Z\mu_n C_o}{L}\left(\frac{K_s x_o}{K_o}\right) KT\, L_D (n_{po}) x_J \left(e^{-U_{Source}} - e^{-U_{Drain}}\right)\right] \quad (22)$$

Where n_{po} is the equilibrium electron density in the bulk. Thus equation (22) represents collector current of BJT with source as the emitter and substrate (or body) as the base.

Substituting (22) into (15) we get

$$I_{DTMOS} = I_D + I_{BJT} \quad (23)$$

i.e.

$$I_{DTMOS} = \left[\frac{Z\mu_n C_o}{2L}\left(\frac{K_s x_o}{K_o L_D}\right)\left(\frac{KT}{q}\right)^2 \int_{U_{Source}}^{U_{Drain}} \int_{U_J}^{U_{surface}} \frac{e^{U-U_F-\xi} - e^{-U_F-\xi}}{F(U,U_F,\xi)} dU\, d\xi\right] + \left[\frac{Z\mu_n C_o}{L}\left(\frac{K_s x_o}{K_o}\right) KT\, L_D (n_{po}) x_J \left(e^{-U_{Source}} - e^{-U_{Drain}}\right)\right] \quad (24)$$

Now the double integral in (24) can be reduced to closed form approximation by following all the assumptions and equations as in [5]. Thus we get

$$I_D = \left[\frac{Z\mu_n C_o}{L}\left\{\left(V_G' + \frac{KT}{q}\right)(V_{SL} - V_{S0}) - \frac{1}{2}(V_{SL}^2 - V_{S0}^2) + V_B^2\left[\sqrt{(U_{Drain} - 1)} - \sqrt{(U_{Source} - 1)} - \frac{2}{3}(U_{Drain} - 1)^{\frac{3}{2}} + \frac{2}{3}(U_{Source} - 1)^{\frac{3}{2}}\right]\right\}\right] \quad (25)$$

V_{S0} is given as

$$V_{S0} = \left(\frac{KT}{q}\right)(2U_F) \tag{26}$$

From (10) we can write (26) as

$$V_{S0} = \left(\frac{KT}{q}\right)\left(2ln\left(\frac{N_A}{n_i}\right)\right) \tag{27}$$

V_{SL} is given as

$$V_{SL} = \left(\frac{KT}{q}\right)(2U_F + U_{Drain})$$

i.e.

$$V_{SL} = V_{S0} + V_{Drain} \tag{28}$$.

V_B is given as

$$V_B^2 = \left(\frac{KT}{q}\right)^2 \left(\frac{K_s x_o}{K_o L_D}\right)\sqrt{\frac{N_A}{n_i}} \tag{29}$$

Therefore (24) can be written as

$$I_{DTMOS} = \left[\frac{Z\mu_n C_o}{L}\left\{\left(V_G' + \frac{KT}{q}\right)(V_{SL} - V_{S0}) - \frac{1}{2}(V_{SL}^2 - V_{S0}^2) + V_B^2\left[\sqrt{(U_{Drain} - 1)} - \sqrt{(U_{Source} - 1)} - \frac{2}{3}(U_{Drain} - 1)^{\frac{3}{2}} + \frac{2}{3}(U_{Source} - 1)^{\frac{3}{2}}\right]\right\}\right] + \left[\frac{Z\mu_n C_o}{L}\left(\frac{K_s x_o}{K_o}\right) KT\, L_D(n_{po})x_J\, \left(e^{-U_{Source}} - e^{-U_{Drain}}\right)\right] \tag{30}$$

III RESULT AND DISCUSSION: The equation (30) forms the core of the proposed model. Assuming Z=10µm, L=1 µm, x_o=10nm, N_A=10^{16}/cm^3 X_J = 0.2 µm, n_{po} approximately same as n_i in this equation for 1µm CMOS technology and various approximations, I_{DTMOS} is plotted against V_{Drain} for constant V_G' as predicted by the proposed model in fig.5.

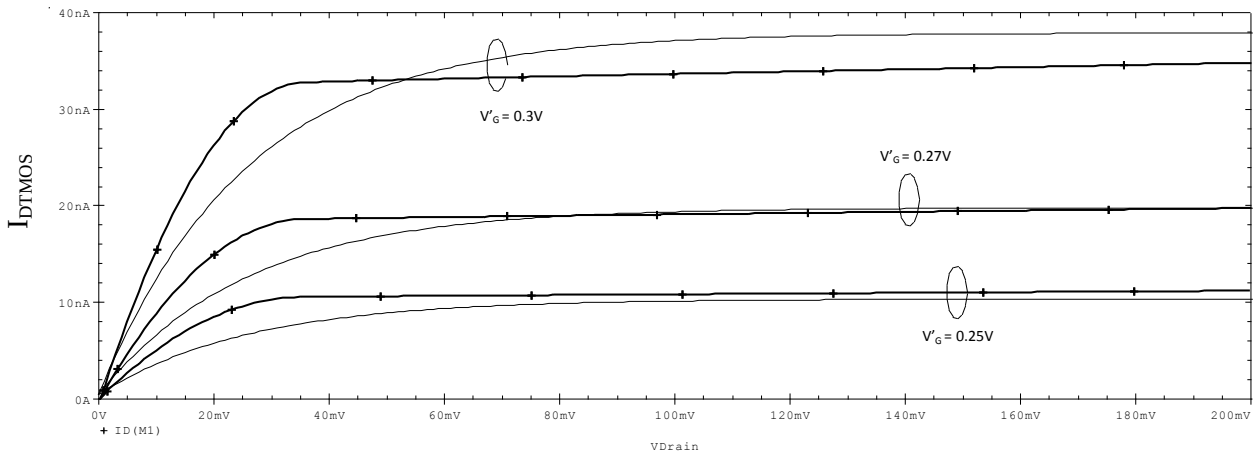

Fig.5: Bulk-DTMOS transistor current I_{DTMOS} versus drain voltage V_{Drain} for 1 μm CMOS technology, (analytical result: solid lines (------) and dotted lines (……) for SPICE simulation).

IV. CONCLUSION: We have modified the Pao-sah model so that it can be applied to bulk-DTMOS transistor. Thus DTMOS transistor can be modeled as parallel combination of BJT and MOSFET for lower values of body ,bias (< 0.4 V).The accuracy of the proposed model has been evaluated by comparing the analytical and SPICE simulation results. Although the theory used for developing the proposed model is valid for long channel devices but it can be utilized in establishing models for short channel devices.

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