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The Influence of Metal Gate Work Function on Short Channel Effects in Atomic-layer Doped DG MOSFETs

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Abstract

The Atomic-layer doped (p-type) Double Gate MOSFETs with different metal gate work functions are simulated to obtain the transport characteristics and short channel effects. Two dimensional quantum transport equations and Poisson equations are used to compute DG MOSFET characteristics. Reduction of short channel effects are observed in atomic-layer doped (p-type) DG MOSFET with different metal gates. Drain induced barrier lowering (DIBL) is reduced, subthrehold leakage current is decreased, I_{on}/I_{off} ratio is increased to 10^4 orders and threshold voltage (V_T) is increased linearly with metal gate work functions 4.2 to 4.5 eV.

Keywords:-DG MOSFET, Metal Work Function, High–κ Dielectric, Short Channel Effects.

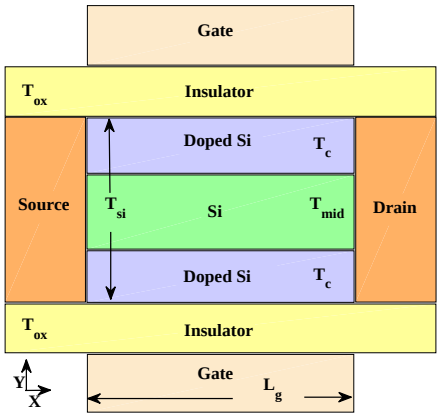

Figure 1: A double gate MOSFET structure with atomic-layer doping. The 2D simulation domain is the portion excluding the top and bottom rectangles marked as Gate.

1 Introduction

The undoped double-gate MOSFET becomes one of the most promising candidates to scale CMOS devices fit into the next generation. This is because DG MOSFETs exhibit better on-off switching, smaller short channel effect, less mobility degradation and free of dopant fluctuation compared to the traditional bulk MOSFETs [1, 2]. DG MOSFETs have other several advantages: ideal 60 mV/dec subthreshold slope, scaling by silicon film thickness without high doping, effective control of short channel effects by the screening effect of the bottom gate, setting of threshold voltage by gate work functions, etc. The threshold voltage of the DG MOSFET is dominantly determined by the work function of the gate material; it is possible to avoid channel doping and associated fluctuation effects [3].

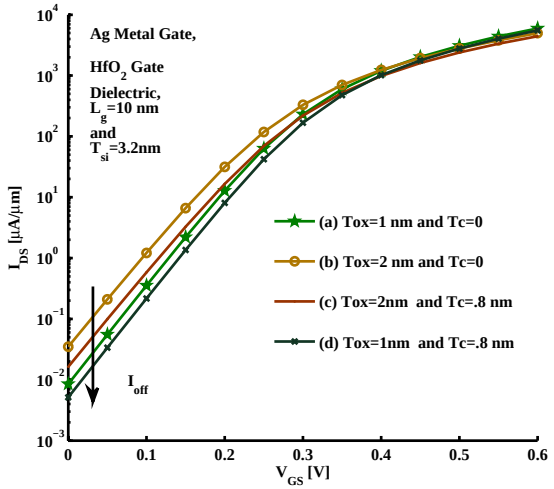

Figure 2: Transfer characteristics of the DG MOSFET device, with Ag metal gate, HfO_2 gate dielectric, T_{ox}=1 or 2 nm, T_{Si}=3.2 nm and L_g=10 nm,(a, b) T_c=0, (c, d) T_c=0.8 nm.

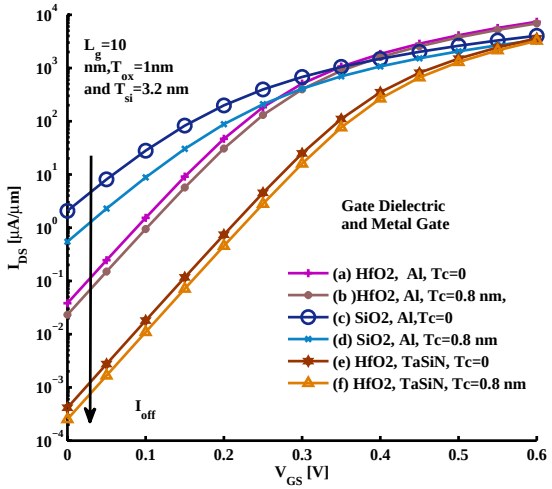

Figure 3: Transfer characteristics of the DG MOSFET device, with Al or TaSiN metal gate, HfO_2 or SiO_2 gate dielectric, T_{ox}=1 nm, T_{Si} = 3.2 nm and L_g = 10 nm,(a, c, e) T_c = 0, (b, d, f) T_c = 0.8 nm.

It is reported that in the 25 nm FET with a thin gate oxide, control of the threshold voltage by increasing depletion charges has many disadvantages, like carrier mobility degradation, large threshold voltage fluctuation due to random dopant distribution and large subthreshold slope [4]. The threshold voltage(V_T) depends not only on the gate work functions, but also on the silicon and gate oxide thicknesses [5]. In order to tailor the V_T, it is important that the gate material should have a tunable work function [6]. A key technological challenge for DG MOSFET is to find gate materials with proper work functions for the desired threshold voltages [7]. Therefore, a gate material with a work function that places its Fermi level close to the middle of the silicon band gap is desired so that the work function difference between the gate electrode and the near-intrinsic silicon film can be adjusted to optimize the threshold voltages of both n- and p-channel devices in a CMOS circuit.

At zero gate voltage, the position of the silicon bands is largely determined by the gate work function, because as long as the thin silicon is lightly doped and the depletion charge is negligible, the bands remain essentially flat throughout the thickness of the film [3]. To control the threshold voltage of MOSFETs, heavy body doping is not compatible with the fully depleted body design which suppresses the floating body effect, improves mobility, and suppresses the dopant fluctuation effect. The threshold voltage requirements pose a severe challenge to the process technology for appropriate gate materials with the tunable work functions that would be compatible with the CMOS process. The threshold voltage can be tuned by the silicon body thickness and the gate work function without substrate doping [8, 9].

The work function of a metal gate electrode has been tuned by, boron-doped poly-$Si_{0.5}$ $Ge_{0.5}$ gate [10], various low-resistance refractory metals and metal silicides (such as tungsten, molybdenum, tungsten silicide, and molybdenum silicide) [11], tunable work function Si_xGe_{1-x} gate [6], high temperature stable germanided NiGe gate [12], metal gates (TiN,

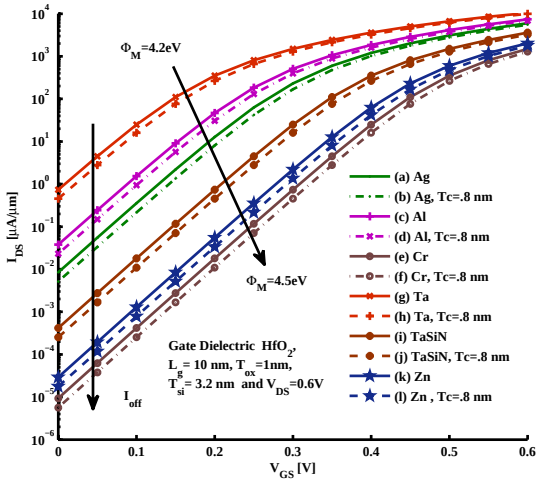

Figure 4: Transfer characteristics of the DG MOSFET device, with Ag, Al, Cr, Ta, TaSiN or Zn metal gate, HfO_2 gate dielectric, $T_{ox} = 1$ nm, $T_{Si} = 3.2$ nm and $L_g = 10$ nm,(a, c, e, g, i, k) $T_c = 0$, (b, d, f, h, j, l) $T_c = 0.8$ nm.

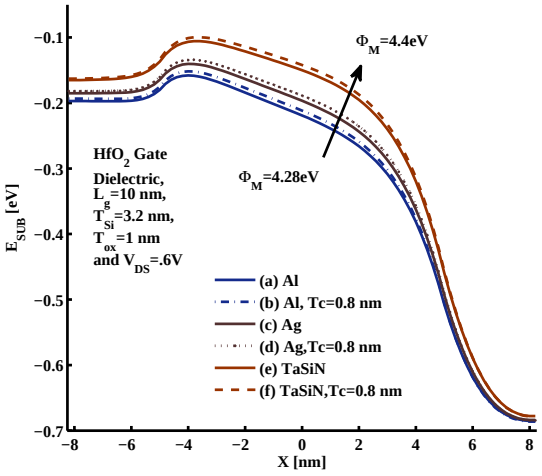

Figure 5: First subband energy vs position along the length of the undoped, atomic-layer doped DG MOSFET with different metal gate (Ag, Al and TaSiN), where: $T_{ox} = 1$nm, $L_g = 10$ nm and $T_{si} = 3.2$ nm, (a, c, e) $T_c = 0$, (b, d, f) $T_c = 0.8$ nm.

TaN) [13, 14] and stacking two metals with different metal combinations on both SiO_2 and HfO_2 gate dielectrics [15].

Trends in silicon technology research show that Si has an enormous potential to achieve terascale integration. Downscaling of device dimensions is essential for the development of terascale integrated circuits based on CMOS Transistors. In order to achieve terascale integration, the double gate metal oxide semiconductor field effect transistor is scaled to a gate oxide thickness of about 1 nanometer, silicon channel thickness to 3 nanometers, and channel length reduced to 10 nanometers [16]. Use of the high–κ dielectric will allow a less aggressive gate dielectric thickness reduction while maintaining the required gate overdrive (gate voltage minus threshold voltage) at low supply voltages. When the gate overdrive diminishes, it will lead to a reduction in the drain current. As the physical gate length is scaled, ideally the gate dielectric equivalent oxide thickness is also scaled correspondingly to control short-channel effects and to increase the saturation current drive. Using high–κ dielectric, the physical thickness of the dielectric layer can be kept large, thereby reducing the gate leakage current, while maintaining the same value of capacitance [17]. There are many materials systems under consideration which have potential to replace SiO_2 as the gate dielectric material. Of the various high–κ dielectric materials, SiO_xN_y, Al_2O_3, HfO_2, La_2O_3, and ZrO_2 have generated a lot of interest due to their high dielectric constant and adequate barrier height [18].

In this work, metal gates Ta, Al, Ag, Ti, TaSiN, Zn and Cr, dielectrics such as SiO_2, HfO_2 and p-type atomic-layer doped channel, were considered in computation of the quantum transport current in DG MOSFET with physical oxide thickness 1nm or 2nm. Two dimensional quantum transport equations and Poisson equations are used to compute DG MOSFET characteristics, self consistently.

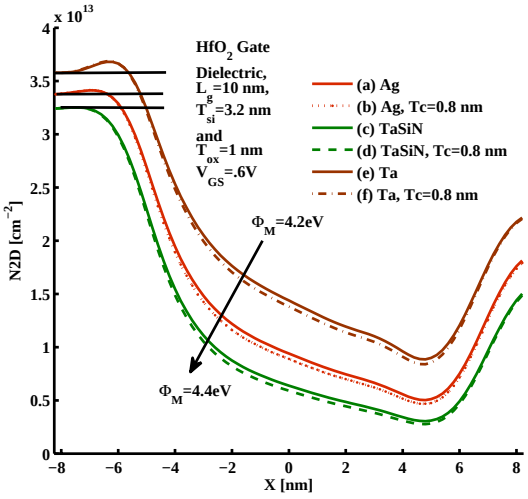

Figure 6: 2D Electron density vs position along the length of the undoped, atomic-layer doped DG MOSFETs with metal gate (Ag, Ta and TaSiN), where: T_{ox} = 1 , L_g = 10 nm and T_{si} = 3.2 nm,(a, c, e) T_c = 0, (b, d, f) T_c = 0.8 nm.

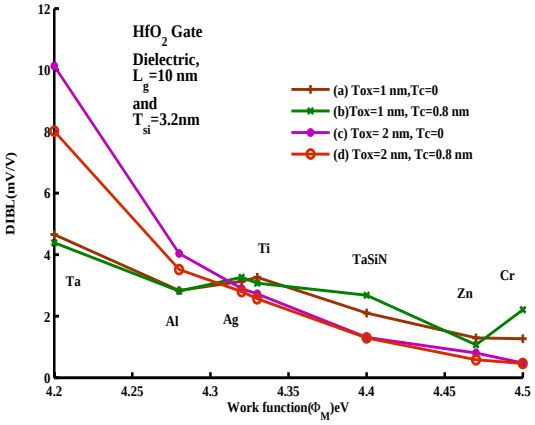

Figure 7: DIBL as a function of metal gate work function for undoped and atomic-layer doped DG MOSFET, where: T_{ox} = 1 and 2 nm, L_g = 10 nm and T_{si} = 3.2 nm,(a, c) T_c=0, (b, d) T_c = 0.8 nm.

2 Method of Analysis

In the simulation scheme we employ the 3D effective mass Hamiltonian which is split into a longitudinal part and a transverse part, since the width of the device is large compared to the other dimensions of the device. As pointed out previously [19], the MOSFET can then be considered as essentially a 2D charge sheet, enabling one to write the transverse eigen states as plane waves. The 3D Hamiltonian can then effectively be reduced to 2D longitudinal Hamiltonian H, if each transverse mode energy is added to the longitudinal energy to get the total energy, which can be written as

$$H = -\frac{\hbar^2}{2m_x^\star}\frac{\partial^2}{\partial x^2} - \frac{\hbar^2}{2m_y^\star}\frac{\partial^2}{\partial y^2} + U_{sc} \qquad (1)$$

where $m_x^\star$, $m_y^\star$ are the effective masses of electrons in the x and y directions respectively. We have added the self-consistent potential U_{SC} to the Hamiltonian. We choose all the six equivalent valleys in the silicon conduction band for this computation.

For the calculation of the gate capacitance with open boundary condition is not sensitive to small changes of the electron effective mass in the gate dielectric region [20]. For the high–κ dielectric materials, in the absence of reliable reference data, effective mass of electrons in dielectric m_{ox} is still widely treated as a fitting parameter and is taken as in gate dielectric region by a constant m_{ox}. Effective electron mass in the gate dielectrics is assumed to be equal to 0.5 m_e and 0.32 m_e for 1 nm and 2 nm gate oxide thickness, where m_e is the free electron mass [20,21]. Conduction band offset to silicon Δ E_c(eV) and dielectric constant (ϵ_r) of the HfO_2 dielectric material used for this computation are 1.5eV and 20 respectively [22–26].

The subbands formed from the strong confinement in the vertical direction are calculated using the uncoupled mode space approach, which is based on the expansion of the 2D active device Hamiltonian in the sub band eigen function space [27]. In the uncoupled mode space approach, we need to solve the 1D Schrödinger equation along the y direction at each x-point of the finite difference grid to obtain the sub band energy levels and eigen functions (modes). The

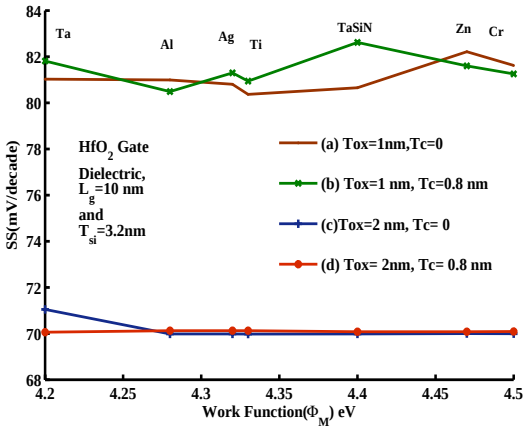

Figure 8: Subthreshold swing as a function of metal gate work function for undoped and atomic-layer doped DG MOSFET, where: T_{ox} = 1 and 2 nm, L_g = 10 nm and T_{si} = 3.2 nm, (a, c) T_c = 0, (b, d) T_c = 0.8 nm.

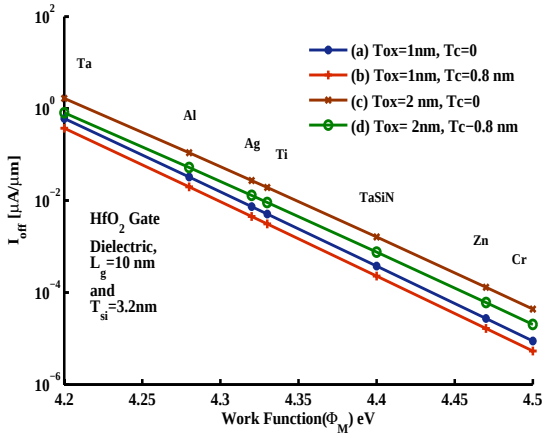

Figure 9: I_{off} as function of metal gate work function for undoped and atomic-layer doped DG MOSFET, where: T_{ox} = 1 and 2 nm, L_g = 10 nm and T_{si} = 3.2 nm,(a, c) T_c = 0, (b, d) T_c = 0.8 nm.

original 2D device Hamiltonian, when expanded in the above mode space, transforms into a 1D Hamiltonian in the transport direction, which can be solved to calculate the electron density $\rho(\vec{r})$ and current within the non–equilibrium Green's function (NEGF) formalism, taking into consideration the effect of coupling of the channel to the source and drain contacts [19]. The self consistent potential U_{sc} is determined from the Poisson equation,

$$\nabla \cdot (\epsilon(\vec{r})\nabla \cdot U_{sc}(\vec{r})) = -\rho(\vec{r}). \qquad (2)$$

The process is repeated till a self consistent solution for electron density is reached. With the converged values of electron density and potential, the drain current is calculated. Uniformly-spaced grids are used in both x and y directions for solving the Poisson equation and the NEGF equations using the finite difference method.

When carriers travel through a semiconductor material, they encounter scattering by various sources, including acoustic and optical phonons, ionized impurities, defects, interfaces, and other carriers. In nano-transistors where the physical gate lengths are smaller than 25 nm which is comparable to the electron mean free path, it is likely not to encounter any scattering events; it can, as a result, move ballistically through the channel. Ballistic models may be sufficient for devices with small gate lengths where scattering can be ignored [28–31].

Transport directions of DG MOSFETs taken for computation on (100) or (110) silicon surfaces are assumed to be [010] or [001] respectively. Inclusion of the wave function penetration into the barrier is efficiently described with this quantum mechanical transport model and induces an additional charge inside the barrier. This charge is self consistently taken into account in this model. We assume metal gates contacts Ta, Al, Ag, Ti, TaSiN, Zn and Cr with work functions 4.2, 4.28, 4.32, 4.33, 4.4, 4.47 and 4.5 eV, and 1 nm or 2 nm thick layers as the top and bottom gate dielectrics (SiO_2 or HfO_2). The source and drain regions included in the finite difference simulation grid are 3.2 nm in extension and have a uniform doping (n-type) of 1×10^{20} cm^{-3}. The channel is made up of atomic-layer doped layers with doping concentration 1×10^{19} cm^{-3} and undoped Si layer for all devices simulated (see Figure 1). The channel length is 10 nm, channel thickness 3.2 nm

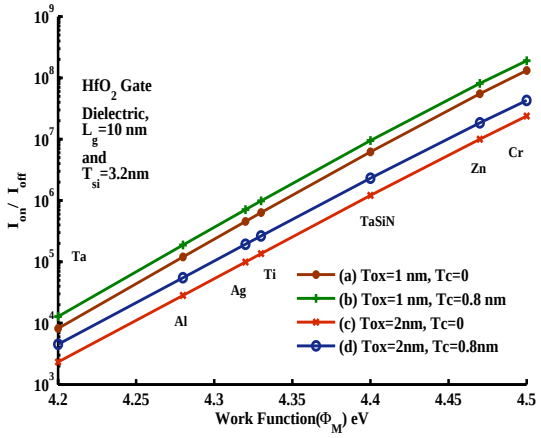

Figure 10: I_{on}/I_{off} as function of metal gate work function for undoped and atomic-layer doped DG MOSFET, where: T_{ox} = 1 and 2 nm, L_g = 10 nm and T_{si} = 3.2 nm, (a, c) T_c = 0, (b, d) T_c = 0.8 nm.

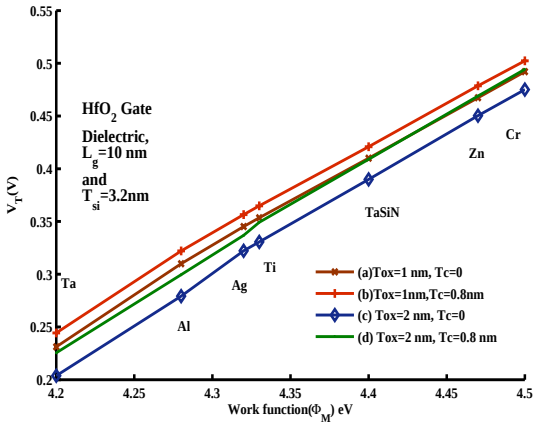

Figure 11: Threshold voltage (V_T) as function of metal gate work function for undoped and atomic-layer doped DG MOSFET, where: T_{ox} = 1 and 2 nm, L_g = 10 nm and T_{si} = 3.2 nm, (a, c) T_c = 0, (b, d) T_c = 0.8 nm.

and atomic-layer doping T_c for studying the variation of DIBL, subthreshold slope (SS), drain current, threshold voltage, subthreshold leakage current and I_{on}/I_{off} with change in dielectric constants.

Silicon dioxide is used as a gate dielectric, due to its electrical isolation in a SiO_2–Si based structure. This electrical isolation is due to the relatively large band gap of SiO_2 (9 eV), making it a good insulator. Although different high–κ dielectric materials are characterized by different values of conduction (valence) band offsets with silicon $\Delta E_c(\Delta E_v)$, dielectric constant (ϵ_r), and electron effective mass in dielectric region m_{ox}, combined effects of these parameters through wave function penetration on gate are taken in to this computation. In order to get the actual influence of high–κ dielectric material in DG MOSFETs characteristics, we used physical dielectric thickness of 1 and 2 nm for all computations instead of effective oxide thickness. If the comparison is done with effective oxide thickness, effect of high–κ dielectric is not reflected in the DG MOSFET characteristics.

The shift in threshold voltages (ΔV_T), corresponding to different V_{DS} = 0.5 V, 0.6 V were calculated employing a modified constant current approximation method. In this method, one calculates the difference ΔV_T between the gate voltages V_{G1} and V_{G2}, corresponding to two different drain voltages V_{D1} and V_{D2}, for some constant current I_D, at the linear portion of the I_{DS}–V_{GS} characteristics. The DIBL is then found from the expression,

$$DIBL = \frac{\Delta V_T}{V_{D2} - V_{D1}}. \quad (3)$$

The subthreshold slope is the change of the gate voltage in the subthreshold region that is required for an order-of-magnitude change of the drain current. The subthreshold slope(SS), is calculated by

$$SS = \frac{\Delta V_{GS}}{\Delta log I_{DS}} \quad (4)$$

at subthreshold region.

3 Results and Discussion

Subthreshold characteristics of the undoped and atomic-layer doped DG MOSFET having channel length L_g = 10 nm, T_{si} = 3.2 nm and T_{ox} = 1 and

2 nm with dielectric HfO_2 and metal gate Ag are shown in figure 2. When the oxide thickness is reduced, effective control of the gate over the channel is increased resulting decrease in subthreshold leakage current (I_{off}) and increase in I_{on} current (Fig.2 curves a & b). Gate control over the channel is further improved by atomic-layer doping thereby I_{off} is reduced (Fig.2 curves a & c and b & d). Due to the atomic-layer doping, effective thickness of the channel is reduced, resulting in the decrease of I_{on}.

Subthreshold characteristics of the undoped and atomic-layer doped DG MOSFET having channel length L_g = 10 nm, T_{si} = 3.2 nm and T_{ox} = 1 nm with dielectrics SiO_2 or HfO_2 and metal gate Al or TaSiN are shown in figure 3. It is clear from the figure 3 (curves a & c) that the subthreshold leakage current (I_{off}) decreases with increase in dielectric constant ϵ_r and the I_{on} current increases with the increase in dielectric constant ϵ_r. When the work function of the metal gate is increased, it results in the decrease in subthreshold leakage current (I_{off}) and decrease in I_{on} current (Fig.3, curves a & e). Subthreshold leakage current I_{off} of the device is further reduced by atomic-layer doping (Fig.3, curves b, d & f).

Subthreshold characteristics of the undoped and atomic-layer doped DG MOSFET having channel length L_g = 10 nm, T_{si} = 3.2 nm and T_{ox} = 1 nm with dielectrics HfO_2 and metal gates Ta, Al, Ag, Ti, TaSiN, Zn and Cr are shown in figure 4. It is clear from the figure 4 (solid curves) that the subthreshold leakage current (I_{off}) decreases rapidly with increase in metal work function Φ_M and the I_{on} current decreases with the increase in metal work function Φ_M. Subthreshold leakage current I_{off} of the device is further reduced by atomic-layer doping (Fig.4, dotted curves).

Lifting of first subband energy at source side along the length of the channel with the increase in metal work function Φ_M are observed in Fig.5, (solid curves). This is due to the increased electric field within the oxide region influencing the potential inside the channel. Lifting of first subband energy in the channel region due to atomic-layer doping is observed in figure 5, (dotted curves).

Lifting of potential profile due to the increase in metal work function Φ_M leads to lowering in electron density in the channel as shown in figure 6, (solid curves). As expected, the electron density for a given channel thickness is lower for p-doped channels in comparison with undoped channels (Fig.6, dotted curves).

The DIBL is calculated from the computed values of I_{DS}–V_{GS} for different values of the metal work function Φ_M and are plotted in figure 7. Higher the metal work function Φ_M, the DIBL value improves. It is observed that as oxide thickness increases, DIBL values also increase (Fig.7, curves a & c). But in the case of p-type atomic-layer-doping, the DIBL value improves slightly (Fig.7, curves b & d).

Figure 8 shows the subthreshold slope as a function of the metal work function Φ_M. Metal work function Φ_M and atomic-layer doping thickness T_c have not much influence on subthreshold slope. It is observed that as oxide thickness increases, subthreshold slope value is decreased (Fig.8, curves a & c).

Leakage current is calculated from I_{DS} and V_{GS} characteristics of DG MOSFET. Figure 9 shows that the increase of the metal work function Φ_M has a very important effect in reducing the leakage currents. When the dielectric thickness T_{ox} is reduced, sharp decrease in leakage current is observed due to increased gate control over the channel (Fig.9, curves a & c). Further improvement of leakage current is realized by atomic-layer doping in the channel (Fig.9, curves a & b and c & d).

The device performance is limited by the relatively low I_{on}/I_{off} ratio for future high speed low power logic applications. Figure 10 shows the improvement of I_{on}/I_{off} ratio with the increase of the metal work function Φ_M. Similar effect is obtained by reducing gate dielectric thickness T_{ox} (Fig. 10, curves a & c). atomic-layer doping in the channel largely complements to increase the I_{on}/I_{off} ratio (Fig.10, curves a & b and c & d).

However, a reduction in the threshold voltage gives rise to an increase in the subthreshold leakage current, which is the current that is conducted through a transistor from its source to drain when the device is intended to be off. Due to this increase in subthreshold leakage current, static power consumption is increased. We used a method of extracting threshold voltage which is the maximum g_m method

in which the drain current is linearly extrapolated to zero at maximum transconductance. Figure 11 shows the threshold voltage as a function of the metal work function Φ_M. Work function Φ_M has linear dependence with V_T for a gate voltage (Fig. 11) . Similar effect is obtained by reducing gate dielectric thickness T_{ox} (Fig. 11, lines a & c). The p-type atomic-layer-doping thickness increases the threshold voltage (Fig. 11, lines b & d).

4 Conclusion

The effects of metal work function and atomic-layer doping on the threshold voltage of the short-channel device is discussed in this paper. The atomic-layer doped (p-type) Double Gate MOSFETs with different metal gate work functions are simulated to obtain the transport characteristics and short channel effects. Reduction of short channel effects are observed in atomic-layer doped (p-type) DG MOSFET with different metal gates. Drain induced barrier lowering (DIBL) is reduced slightly, subthrehold leakage current is decreased to 10^4 orders, I_{on}/I_{off} ratio is increased to 10^4 orders and threshold voltage (V_T) is increased linearly in 1 nm dielectric thickness T_{ox} with metal gate work functions 4.2 to 4.5 eV. Results show that in atomic-layer doped DG MOSFETs, threshold voltage can be tuned by the metal gate work functions.

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