Journal of Electron Devices, Vol. 7, 2010, pp. 214-224

© JED [ISSN: 1682 -3427]

Journal of Electron Devices
www.jeldev.org

Analytical Estimation of Breakdown Voltage and Power Dissipation of Double Implanted MOSFET on 6H Silicon Carbide Wafer with Linearly Graded Profile

Munish Vashishath[1,*] and Ashoke K. Chatterjee[2]
[1] Department of Electrical and Electronics Engineering, YMCA Institute of Engineering, Faridabad, India 121006
[2] Department of Electronics and Communication Engineering, Thapar Institute of Engineering and Technology, Patiala, India, 147004
*Correspondence: [1]munish.vashishath@gmail.com

Accepted 30 November-2009

Abstract: Silicon Carbide (SiC) has revolutionized the semiconductor power devices. It is a wide band gap semiconductor with an energy gap wider than 2eV and possesses extremely high power high voltage switching characteristics, high thermal, chemical and mechanical stability. This paper describes the device structure of vertical DIMOSFET with linearly graded profile in the drift region with a low doping of 10^{14} per cc near the source to higher values near the drain. The effect of a linearly graded drift region in a 6H-SiC vertical DIMOSFET on the power dissipation of the device has been discussed. The profile used has a low peak doing level at the top near the source and increases linearly towards the drain. The mathematical calculations of depletion region width as well effective doping concentration was done separately. The drift region defines the blocking voltage capabilities. In this paper the breakdown voltage upto 6.75 to 10 kV is reported with linearly graded profile.

1.0 Introduction:

There are large numbers of material and electronic properties which make SiC a promising material for high power devices, such as wide bandgap (~ 3eV), high breakdown field of 3MV/cm and good thermal conductivity (3W per cm K). Some of the prominent devices are the inversion and accumulation mode DIMOSFET's [1-2] and accumulation mode UMOS [3-4] have already being successfully developed and tested. For vertically oriented majority carrier devices, the specific- on-resistance, $R_{on\text{-}sp}$ has been shown to have a theoretical minimum value, under punch through conditions, given by

$$R_{on-sp} = \left(\frac{3}{2}\right)^3 \frac{V_B^2}{\mu_n \varepsilon_S E_C^3} = \frac{3.375 V_B^3}{\mu_n \varepsilon_s E_C^3} \qquad (1)$$

where $R_{on\text{-}sp}$ is the resistance-area product expressed in Ω-cm^2, μ_n is the electron mobility perpendicular to the surface, ε_s is the permittivity of the semiconductor, E_c is the crtical field for avalanche breakdown normal to the surface and V_B is the breakdown or blocking voltage of the drift region. The critical field E_c in SiC is almost and order of magnitude higher tan in Silicon. Hence, even if the electron mobility in SiC is lower than in silicon, the high value of E_c gives a substantially a lower value of specific on resistance, typically 400 times less. These parameters and their variations have been extensively analyzed by Cooper et al [5].

The most notable among the DIMOSFET's are those that have been made on 6H-SiC wafer and are the accumulation channel DIMOSFET developed at the University of North Carolina in 1997[6]. This increased the effective channel mobility and reduced the magnitude of R_{on-sp} to 18 mΩ-cm^2. The other parameters that affects the inversion channel mobility is the density of interface states (D_{it}) on p-type SiC since all n-channel devices are made on top of it. It was found that the density of interface staes rises exponentially towards the conduction band edge in upper half of the band gap reaching levels of 10^{13} eV^{-1}cm^{-2}. However, post oxidation annealing in nitric oxide (NO) can significantly reduce (D_{it}) yielding higher inversion layer mobilities [8-11]. Further reduction in R_{on-sp} has been made with the development of ACCUFET which has drastically increased the channel mobility from very low values [12] to 120 cm^2 per volt-sec [13]. This brought down the value of R_{on-sp} to 18mΩ-cm^2. Further improvements in channel mobility in 6H-SiC MOSFETs has also made using a buried channel with mobilities going upto 180 cm^2 per volt-sec [14].

The ultimate aim in reducing the magnitude of R_{on-sp} of vertical DIMOSFET is to reduce its power dissipation, P_D or its power loss which is given by $P_D \sim J_{on}^2 R_{on-sp} A$, where J_{on} is the on state current density and A is the device cross-sectional area. The reduction of power dissipation suggested in this paper has been made on the basis of using a linearly graded doping profile in the epitaxial layer of the DIMOSFET with a lightly doped region at the top to a gradually increasing doping level near the drain and at the bottom of the device. Such a profile has a linearly graded profile in the accumulation region (A), JFET region (B) and drift region (C) of the vertical DIMOSFET shown in Fig.1. The device should give a wide depletion region owing to low doping level in region B and a low parasitic series resistance in region C because of a higher doing level. This structure should significantly reduce the magnitude of R_{on-sp} because of an increase in magnitude of the effective doping level and a corresponding decrease in the depletion region width at a given value of V_{DS}. Such devices are likely to have a lower power dissipation, smaller device thickness and a lower blocking voltage than device with uniformly doped epitaxial layers.

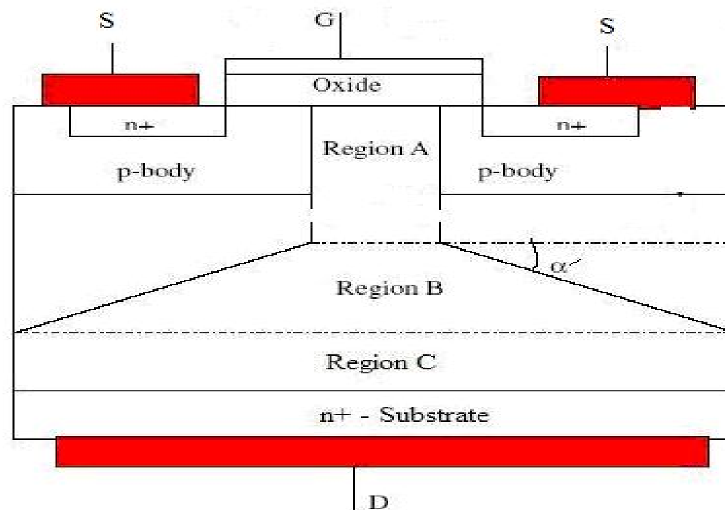

Fig.1

2.0 Theoretical Analysis:

The basic structure of the DIMOSFET as shown in Fig.1. It is redrawn labeled with the device dimensions using suitable symbols and is shown in Fig.2.

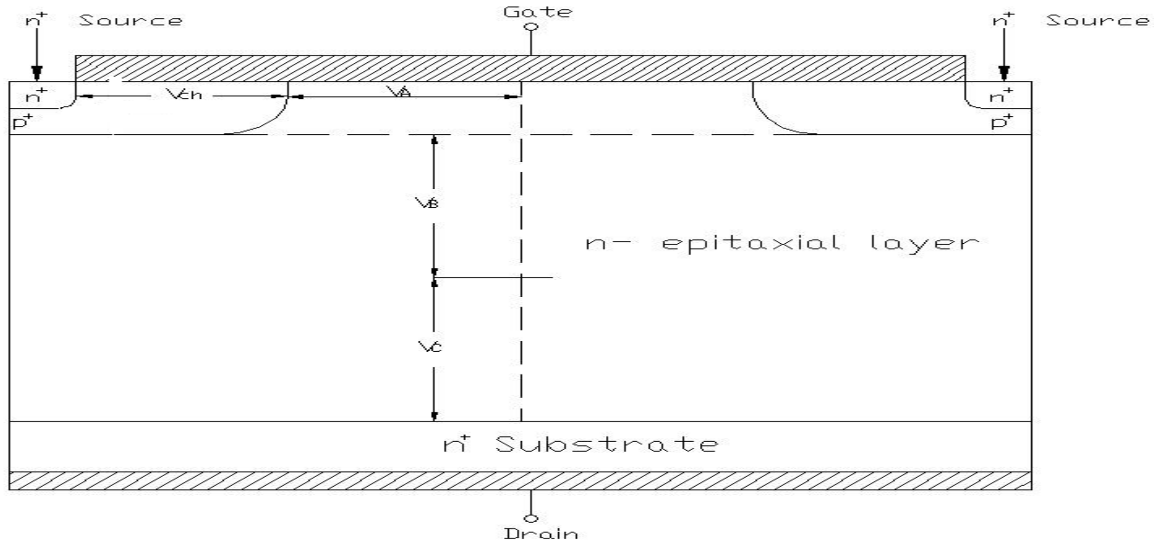

Fig.2

The power dissipation, P_D for a 50% duty cycle of these two devices for various current levels can then be calculated using the basic equations:

$$P_D = \frac{1}{2}\left(J_{on}^2 AR_{on-sp} + V_B A\right), \quad (2)$$

where, J_{on} is the on state current density, J_L is the reverse leakage current density of the p-body/n-drift region junction located in region B(Fig.1), V_B is the breakdown voltage of the DIMOSFET and A is the device area. Since J_L is negligible in SiC diode [15], eq(2) can be simplified

$$P_D = \frac{1}{2}\left(J_{on}^2 AR_{on-sp}\right). \quad (3)$$

Writing J_f as the forward current density considered to be the same as J_{on}, eq (3) gives,

$$P_D = \frac{1}{2}\left(J_f^2 AR_{on-sp}\right). \quad (3)$$

The channel current I_{ch} which equals the drain current I_{DS} in on-state can be expressed by [16]:

$$I_{DS} = \frac{W\mu_n}{2L[1+(\mu_n/2v_{sat}L)V_{ch}]} V_{ch}[2C_{ox}(V_{GS}-V_T)-(C_{ox}+C_{do})V_{ch}], \quad (4)$$

where W is the device width, L is the channel length, μ_n is the effective zero field doping dependent carrier mobility corresponding to doping level N_B of the drift region obtained from[15], V_{ch} is the voltage across the channel region, v_{sat} is the saturated drift velocity of the carrier taken to be $2x10^7$ cm per sec, C_{ox} is the oxide capacitance per unit area, V_{GS} is the gate to source voltage, C_{do} is the body depletion capacitance considered to be much less than C_{ox} and can be neglected.

The values of V_{ch} can be evaluated by using equation (4). For this equation, the value of C_{do} is much less than C_{ox} and can be neglected and the value of V_{GS}=40V and V_T=1V, the equation (4) now becomes

$$I_{DS} = \frac{W\mu_n C_{ox} V_{ch}[78 - V_{ch}]}{2L[1+(\mu_n/2v_{sat}L)V_{ch}]} \quad (5)$$

where μ_n is the mobility at the effective doping level, N_{eff}.

After solving eq. (5), we get

$$I_{DS} = \frac{W\mu_n C_{ox} V_{ch}[78 - V_{ch}]}{2v_{sat}L + \mu_n V_{ch}} \quad (6)$$

Eq.(6) can be written as

$$W\mu_n v_{sat} C_{ox} V_{ch}^2 + (\mu_n I_{DS} - 78W\mu_n v_{sat} C_{ox})V_{ch} + 2v_{sat} L I_{DS} = 0 \quad (7)$$

Eq.(7) is again a quadratic equation, the value of V_{ch} could be evaluated as:

$$V_{ch} = \frac{-(\mu_n I_{DS} - 78W\mu_n v_{sat} C_{ox}) \pm \sqrt{(\mu_n I_{DS} - 78W\mu_n v_{sat} C_{ox})^2 - 8LWI_{DS}\mu_n v_{sat}^2 C_{ox}}}{2W\mu_n v_{sat} C_{ox}} \quad (8)$$

The voltage drops across regions A, B and C have derived [16] and found to be of the form:

$$V_A = \frac{I_{DS}(W_j + W_d)}{W(L_{diff} eN_{eff})\mu_n - I_{DS}/E_c} \quad (9)$$

$$V_B = \frac{I_{DS}}{WeN_{eff}\mu_n \cot\alpha} \log\left[\frac{WeN_{eff}(\mu_n(L_{diff} + L_p) - I_{DS}/E_c}{WeN_{eff}\mu_n L_{diff} - I_{DS}/E_c}\right] \quad (10)$$

$$V_C = \frac{I_{DS}(W_t - W_j - W_d - L_p \tan\alpha)}{WeN_{eff}\mu_n(L_s + 2L_p) - I_{DS}/E_c} \quad (11)$$

where the symbols are the same as those shown in Fig.2 and L_{diff} is the separation of p-bodies with N_{eff} being doping level of drift region. Here W_t=h, the device height which has been set by using the maximum depletion region width i.e the punch through width at a pre designed breakdown voltage of 10kV. W_j is the p-body thickness and W_d is the depletion region width under on-state condition, the drain to source voltage V_{DS} is obtained by adding V_{ch}, V_A, V_B and V_C. The drift region voltage drop $V_{drift}=V_A+V_B+V_C$ and $V_{DS}=V_{drift}+V_{ch}$. The device height, h has been set by setting the punch through depletion region width equal to that at the avalanche breakdown voltage. The quantity 'E_c' in equations (9) to (11) is the critical field for avalanche breakdown.

For the case of DIMOSFET with a linearly graded drift region as shown in Fig.3 with a gradient α, the p-body/n-epitaxial layer junction, depletion region width has been evaluated using the equation of a one-sided linearly graded junction as the depletion region in the lightly doped p-body can be regarded as negligible. Fig.4 shows the cross section of 6H-SiC DIMOSFET with linearly graded profile and gradient α.

***Determination of* N_{eff} [17]:**

Consider the cross section of the epitaxial layer of Figure 3 as shown in Figure 4. The resistance dR of a thin element of thickness dx at a distance x from the top of this device can be expressed as

$$dR = \frac{1}{\mu_n eN(x)} \frac{dx}{A} \quad (12)$$

where A is the cross-sectional area in the direction perpendicular to the figure. The total resistance R of this layer can be evaluated by writing $N(x) = N_0 + \alpha x$ and integrating within limits of x from 0 to h, where h is the height of the device. This gives

$$R = \int_0^h \frac{1}{\mu_n eA} \frac{dx}{(N_0 + \alpha x)} \quad (13)$$

Gate

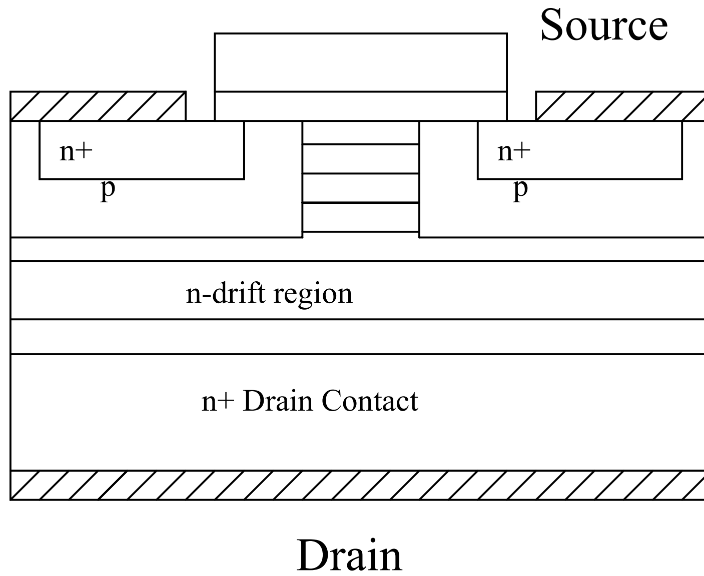

Fig.3

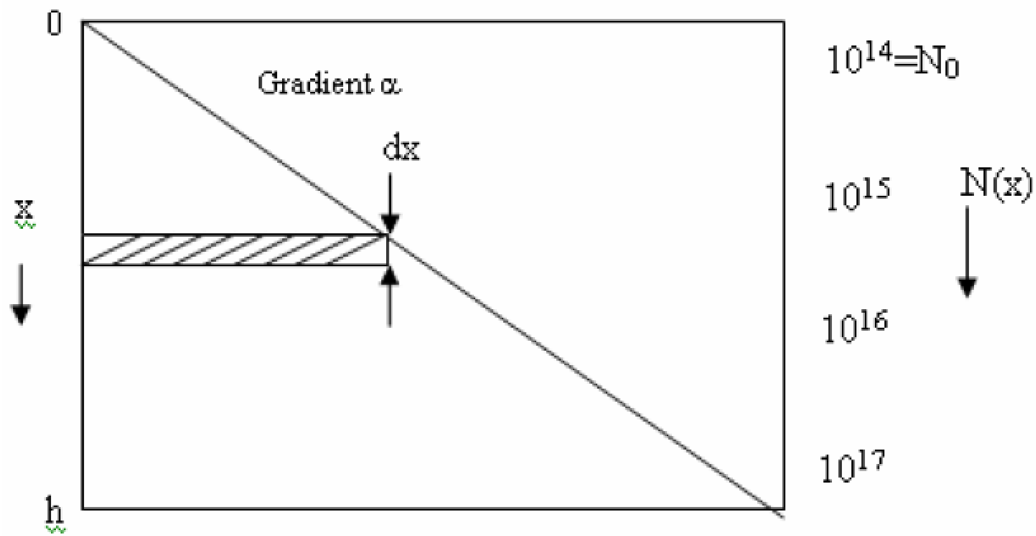

Fig.4

On solving eq.(12), the value of R can be determined as:

$$R = \frac{1}{\mu e A \alpha} \ln\left[1 + \frac{\alpha h}{N_0}\right] \qquad (14)$$

If the effective concentration of this layer is N_{eff}, then R may also be written as

$$R = \frac{1}{\mu e N_{eff}} \frac{h}{A} \qquad (15)$$

Comparing equations (14) and (15), N_{eff} may be written as

$$N_{eff} = \frac{h\alpha}{\ln\left(1 + \frac{\alpha h}{N_0}\right)} \tag{16}$$

where N_0 is the value of the n-drift region doping level at the p-base /n-drift region junction assumed to be 10^{14} or 10^{15} per cc in this paper.

Lastly, the specific on-resistance of the DIMOSFET can be expressed using Fig.2 as [16]:

$$R_{on-sp} = RA = \rho l = \frac{\left(W_t - W_j - W_d - L_p \tan\alpha'\right)}{\mu_{neff} eN(x)} \tag{17}$$

where α' is the angler of the slope of the drift region narrowing and μ_{neff} has been obtained from [15] corresponding to the effective concentration of N_{eff} of the linearly graded drift region. Thus N_{eff} and μ_{neff} give the overall average value of doping level and carrier mobility in the drift region respectively. A fixed value of device current $I_{DS}=I_{ch}$ was used and W_d was obtained by iteration from eq. (8). Finally Ron-sp was calculated using eq.(9).

The magnitude of power dissipation P_D was calculated by knowing R_{on-sp}, J_{on} and the device cross sectional area A. Values of P_D for different doping levels for uniformly doped drift regions and concentration gradients for different graded profiles were calculated for different current levels. The value of V_B and V_C were then calculated using eqs.(10) and (11). The magnitude of V_{ch} was obtained knowing a preset value of I_{DS} from eq.(4). The drain to source voltage V_{DS} is given by: $V_{DS}= V_{drift}+V_{ch}= V_{ch} + (V_A+V_B+V_C)$, where V_{drift} is the voltage drop across the drift region. Finally, the forward voltage drop can be calculated using the equation $V_f=J_{on} \cdot R_{on-sp}$.

The Critical Field, E_c and the Breakdown Voltage (V_{BPT} and V_{BAV})

The depletion region width at breakdown was estimated by first estimating the depletion region width for punch through breakdown voltage, V_{BPT} and was obtained using the equation

$$W' = \left[\frac{12\varepsilon_s (V_{BPT} + V_g)}{eN_B}\right]^{\frac{1}{3}} \approx \left[\frac{12\varepsilon_s V_{BPT}}{eN_B}\right]^{\frac{1}{3}} \tag{18}$$

as $V_g \ll V_{BPT}$, where V_g is the gradient voltage for the linearly graded drift region.

The depletion region width W' for a linearly graded drift region corresponding to punch through breakdown voltage, V_{BPT} was obtained from eq.(18). The corresponding critical field E_c for avalanche breakdown was obtained using the equation [18]:

$$E_c = \left(\frac{e\alpha W'^2}{8\varepsilon_s}\right), \tag{19}$$

where W' represents the depletion region width at breakdown.

The avalanche breakdown voltage V_{BAV} was then calculated using the equation

$$V_{BAV} = \frac{2}{3} E_C W' \tag{20}$$

where the depletion widths at the two breakdown voltages have again been set equal to each other for actual device design i.e. $W=W'$.

3.0 Calculations & Related Graphs:

The device dimensions of 6H DIMOSFET have been set so that the height $h \approx W_t$ equals the depletion region width, W_d under a reverse bias of 6.75kV applied on the p-body/n-epitaxial layer junction. The dimensions of other variables as shown in Fig.2 have been taken to be: W_j=1µm, L_p=25µm, $\alpha^{/}=64^0$, where $\alpha^{/}$ is the angle of slope of drift region narrowing and a smaller value of $\alpha^{/}$ corresponds to be wider spread of the current from the accumulation region A has been used here. The quantity W_j has been taken to be 1µm as implant depth in 6H-SiC is of this order [19].The device cross-sectional area is taken with width x length as300x80µm^2 =24000x10^{-8} cm^2. The device have been split into two by a vertical line bisecting the device of Fig.1, giving a single unit of calculations with a cross sectional area A=12000x10^{-8} cm^2.

Calculations of the 6H-SiC DIMOSFET with a linearly graded drift region has been made by using a doping profile with a doping level of 10^{14} per cc near the source to 10^{16}, 10^{17} and 10^{18} per cc near the drain and other with a 10^{15} to 10^{19} per cc gradient of the device height W_t=h. The device height 'h' had been set at 65µm instead of 73 µm for the uniformly doped profiles as graded profiles yield smaller depletion region width at a given voltage than uniformly doped profiles as graded profiles yield smaller depletion width at a given voltage than uniformly doped regions. The corresponding reverse voltage which is the punch through voltage, V_{BPT} obtained from eq.(19) is 6.75kV. The gradient α is obtained by taking the difference in carrier concentration from source to drain and dividing it by W_t=h=65µm.

The specific R_{on-sp} is obtained by calculating N_{eff} from eq.(16), finding the effective value of mobility, μ_{neff} from the µ versus field plot [15] and using eq.(17) with $\alpha^{/}=64^0$.

The values of power dissipation, P_D was then calculated using current densities, J_F ranging in magnitude from 1 to 1000 amperes per cm^2. This was repeated for other values of concentration gradient 'α'. The results are shown in Tables I to IV. The plot of power dissipation vs J_F, the forward current density is shown in Fig.5. The variation of the specific on resistance of the device for the various values of V_{DS} is shown in Fig.6.

Table I

For10^{16}-10^{14},h=.0065,N_{eff}=2.15x10^{15}/cc,μ_n=530cm^2/V-sec,α=1.58x10^{18}, A=12000x10^{-8} cm^2

J_f	I	V_{ch}	V_A	V_B	V_C	$V_{DS}=V_A+V_B+V_C+V_{ch}$	W_d	R_{on-sp}	V_f	P_D
1	12e-5	.0028	.0015	.0191	.0059	.0293	1.07e-4	.0119	.0119	7.13e-7
10	12e-4	.028	.024	.191	.0561	.299	2.33e-4	.0099	.099	6.72e-5
100	12e-3	.283	.4383	1.91	.487	3.116	5.1e-4	.00883	.883	.0058
1000	12e-2	3.16	8.80	19.20	3.23	34.32	.0011	.00847	8.46	.3761

Table II

For10^{17}-10^{14},h=.0065, N_{eff}=1.45x10^{16}/cc, μ_n=500cm^2/V-sec,α=1.54x10^{19},

$A=12000x10^{-8}cm^2$

J_f	I	V_{ch}	V_A	V_B	V_C	$V_{DS}=V_A+V_B+V_C+V_{ch}$	W_d	R_{on-sp}	V_f	P_D
1	12e-5	.003	1.52e-4	.0030	9.6e-4	.0071	3.1e-5	.0019	.0019	1.16e-7
10	12e-4	.029	.0019	.030	.0095	.071	6.66e-5	.0016	.0163	1.15e-5
100	12e-3	.3	.0281	.301	.0921	.721	1.4e-4	.0014	.1428	.0011
1000	12e-2	3.37	.480	3.01	.847	7.70	3.18e-4	.0011	1.1429	.1015

Table III

For10^{18} -10^{14}, h=.0065, N_{eff}==$1.09x10^{17}$/cc,μ=$300cm^2$/V-sec,α=$1.54x10^{20}$,
$A=12000x10^{-8}$ cm^2

J_f	I	V_{ch}	V_A	V_B	V_C	$V_{DS}=V_A+V_B+V_C+V_{ch}$	W_d	R_{on-sp}	V_f	P_D
1	12e-5	.0050	2.91e-5	6.67e-4	.00022	.0059	1.35e-5	.00042	.00042	2.61e-8
10	12e-4	.050	3.31e-4	6.67e-3	.0022	.059	2.92e-5	.00040	.0040	2.59e-6
100	12e-3	.50	.0042	.0667	.021	.592	6.28e-5	.00037	.03658	2.55e-4
1000	12e-2	5.82	.0617	.667	.205	6.754	1.41e-4	.00034	.3387	.025

Table IV

For 10^{19}-10^{15},h=.0065, N_{eff}=$1.09x10^{18}$/cc,μ=$140cm^2$/V-sec,α=$1.54x10^{21}$,
$A=12000x10^{-8}cm^2$

J_f	I	V_{ch}	V_A	V_B	V_C	$V_{DS}=V_A+V_B+V_C+V_{ch}$	W_d	R_{on-sp}	V_f	P_D
1	12e-5	.011	5.91e-6	1.42e-3	4.66e-5	.0112	7.77e-6	9.32e-5	9.32e-5	5.59e-9
10	12e-4	.11	6.51e-5	1.43e-3	4.64e-4	.112	1.67e-5	8.68e-5	8.68e-4	5.57e-7
100	12e-3	1.08	7.45e-4	1.429e-2	4.61e-3	1.103	3.58e-5	7.65e-5	7.65e-3	5.53e-5
1000	12e-2	14.28	.0101	.143	.0453	14.48	8.46e-5	6.79e-5	6.79e-2	.0054

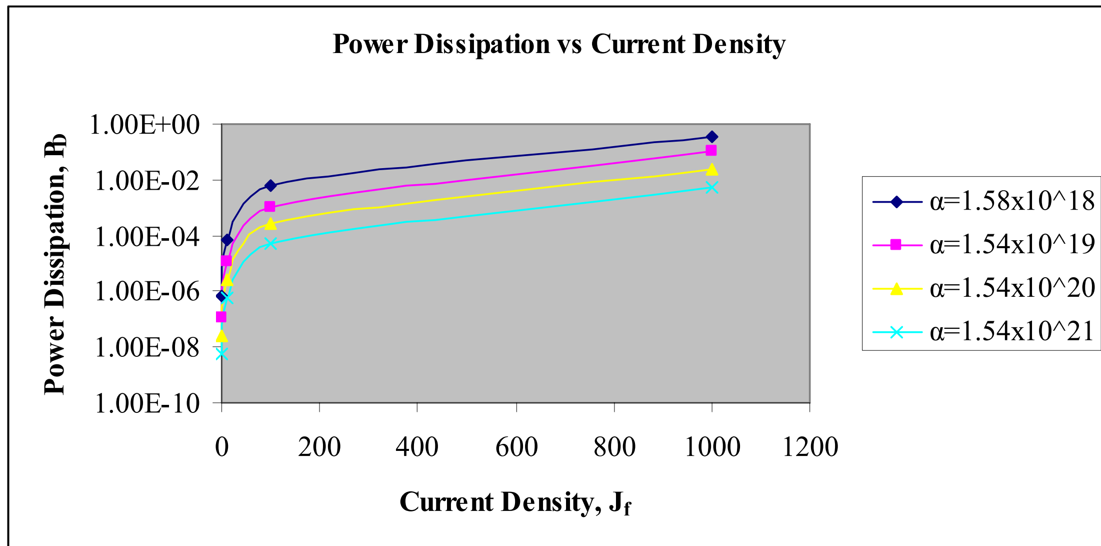

Fig.5

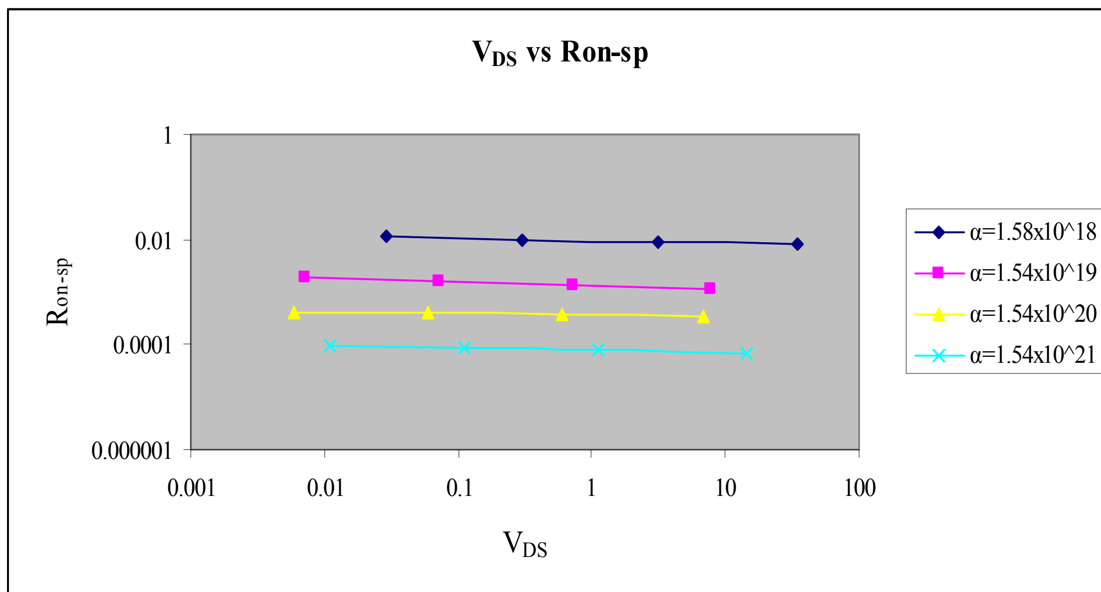

Fig.6

Calculation of Breakdown Voltages (V_{BPT} and V_{BAV}):

The breakdown voltage considered here are the punch-through breakdown voltage, V_{BPT} and the avalanche breakdown voltage, V_{BAV}. For a given voltage, device design requires that the two voltages be made equal to each other. In this work, the lower breakdown voltage has been considered for use as the device breakdown voltage.

In case of linearly graded profile, the punch through breakdown voltage V_{BPT} was set at 6.75kV for a depletion region width W of 65 µm considered equal to device height W_t=h with a gradient of 1.58×10^{18} cm^{-4}. The value of critical field, E_c was calculated using equation (19) and avalanche breakdown voltage V_{BAV} from equation (20). The depletion region width $W^{/}$ for the values of α were calculated by using equation (18). The results are shown in Table V.

Table V

6H-SiC DIMOSFET linearly graded drift region V_{BPT}=6.75kV, $\alpha=1.58*10^{18}cm^{-4}$, W_t=h=65μm

Grad 'α' cm^{-4}	$W^{/}$(μm)	$E_c = \left(\frac{e\alpha W'^2}{8\varepsilon_s}\right)$ (V/cm)	$V_{BAV}=(2/3)(E_cW^{/})$ (volts)	V_{BPT} (volts)
$1.32x10^{18}$	75	$1.73x10^{6}$	8.75 kV	10 kV
$1.58x10^{18}$	65	$1.55x10^{6}$	6.74 kV	6.75kV
$1.54x10^{19}$	26	$2.42x10^{6}$	4.20 kV	4kV
$1.54x10^{20}$	8.56	$2.63x10^{6}$	1.49 kV	1.5kV
$1.54x10^{21}$	3.42	$4.20x10^{6}$	956.37V	1kV

Conclusions & Discussion:

An analysis of calculated data of uniformly doped drift regions of the 6H-DIMOSFET presented in Tables I to IV shows that increasing current levels for a given drift region doping level cause an increase in the magnitudes of V_{ch}, V_A, V_B, V_C and consequently V_{DS}. An increase in V_{DS} causes an increase in magnitude of the depletion region width, W_d, the forward drop, V_f and the power dissipation, P_D. However, the magnitude of R_{on-sp} decreases with an increase in the value of W_d and can be verified from eq.(17). This is shown in Fig.5 which shows the non-linear increase in power dissipation, P_D with forward current density, J_f. The variation of R_{on-sp} with V_{DS} is shown in Fig.6. As the doping level of the drift region increases, the drop over the channel, V_{ch} but all other values including V_{DS}, V_f, W_d, R_{on-sp} and P_D are found to be decreased. The decrease in power dissipation, P_D at higher doping levels of the drift region is primarily to a decrease in the magnitude of R_{on-sp}. At a current density, J_f of 1000 A/cm^2, the power dissipation, P_D is estimated to fall by about 0.3761 to .0054 as the drift region doping levels changes from 10^{15} per cc to 10^{18} per cc. However, high doping levels limit the value of breakdown voltage, V_B and so an optimum value of drift region doping level will have to be selected which can give a low value of P_D and a high value of V_B.

Estimation of breakdown voltages, i.e punch through (V_{BPT}) and avalanche (V_{BAV}) breakdown voltage, can be made on the basis of the calculated data presented in Table V for linearly graded drift region devices. Table V gives the calculated values of V_{BAV} and V_{BPT} for various values of α, the concentration gradients of the drift region of the 6H-SiC DIMOSFET. From a tally of breakdown voltages shown in Table V, it can be found that a linearly graded drift region with the value of α of $1.58x10^{18}$ cm^{-4} with a device height of 65 μm would give the V_{BAV} of 6.74kV and V_{BPT} of 6.75kV. As shown in Table V, it can also be found that a linearly graded drift region with the value of α of $1.32x10^{18}$ cm^{-4} with a device height of 75 μm would give the V_{BAV} of 8.75kV and V_{BPT} of 10 kV.

In conclusion, it may be stated that 6H-SiC DIMOSFET's having linearly graded drift regions have significantly low values of power dissipation, P_D at any current level than uniformly doped drift region devices. Thus, it is useful to obtain 6H-SiC DIMOSFET's with linearly graded drift regions as these devices could be fabricated with lesser device height and give low power dissipation but a slightly more breakdown voltage than uniformly doped drift region.

References:

1. J.A.Cooper, S.H.Ryu, M.Matin, J.Spitz, D.T.Morisette, H.M.Meglothlin, M.K.Das, M.R.Melloch, M.A.Capano and J.M. Woodall, " SiC power electronic devices, MOSFETs and Rectifiers," Int. Mat. Res. Soc. Symp. Proc., vol. 572, 1999, pp. 3-12.
2. H. Morkoe, S. Strite, G.B.Gao, M.E.Lin, B.Sverdlov, and M.Burns, " Large bandgap SiC, III-V nitride and II-VI ZnSe-based semiconductor device technologies," J.Appl.Phys., vol.76, pp.1363-1398, Aug.1994.
3. D. M. Brown, E.Downey, M. Ghezzo, J. Kretchmer, V.Krishnamurthy, W.Hennessy and G.Michon, " Silicon carbide MOSFET Technology", Solid-State Electron, vol.39, pp.1531-1542, 1996.
4. R.Schorner, P.Friedrichs, D.Peters and D.Stephani, "Significantly improved performance of MOSFETs on silicon Carbide using the 15R-SiC polytype," IEEE Electron Device Lett., vol.20, pp.241-244, July 1999.
5. J. A. Cooper, M. R. Melloch, R. Singh, A. Aggarwal, and J. W. Palmour, "Status and prospect for SiC MOSFET", IEEE Trans. Electron Devices, vol. 49, pp. 658-664, April, 2002.
6. P. M. Shenoy and B. J. Baliga, "High voltage planar 6H-SiC ACCFET," in silicon carbide, III-Nitrides and Related Materials, Zurich, Switzerland: Trans Tech, 1998, p.993.
7. V.V.Afanasev, M.Bassler, G.G.Pensl and M.Scultz, "Intrinsic SiC/SiO_2 interface states," Phys. Stat. Sol., vol. 162, p.321, 1997.
8. C.Y.Chung, C.C.Tin, J.R.Williams, K.McDonald, M.Di Ventra, S.T.Pantelides, L.C.Feldman and R.A.Weller, "Effect of nitric oxide annealing on the interface trap densities near the band edges in the 4H polytype of silicon carbide," Appl. Phys. Lett., vol.76, p.1713, 2000.
9. C.Y.Chung, C.C.Tin, T.Issacs-Smith, J.R.Williams, K.McDonald, M.Di Ventra, S.T.Pantelides, L.C.Feldman, R.A.Weller and O.W.Holland, "Nitrogen passivation of interface states near the conduction band in silicon carbide," Mat. Res. Soc. Symp., Boston, MA, Nov. 27-Dec.1,2000.
10. M.K.Das, L.A.Lipkin, J.W.Palmour, G.Y.Chung, J.R.Williams, K.McDonald and L.C.Feldman, "High mobility 4H-SiC inversion mode MOSFETs using thermally grown, NO annealed SiO_2," IEEE Trans. Device Research Conf., Denver, CO, June 19-21,2000.
11. M.G.Spencer, J.W.Palmour, and C.H.Carter, "Substrate and Epitaxial Issues for SiC Power Devices," IEEE Trans. Electron Devices, vol.49, Apr.2002.
12. P. M. Shenoy and B. J. Baliga, "The planar 6H-SiC ACCFET: A new high-voltage power MOSFET structure," IEEE Trans. Electron Device Lett., vol.18, pp. 589-591, Dec.,1997.
13. Ravi K.Chilukuri, P. M. Shenoy and B. J. Baliga, "Comparison of 6H-SiC and 4H-SiC high voltage planar ACCUFETs," Int. Symp. On Power Semiconductor Devices & ICs, Kyoto, pp.115-118, 1998.
14. Scott T.Sheppard, Michael R.Melloch and James A.Cooper, "Characteristics of inversion channel and buried channel MOS Devices in 6H-SiC," IEEE Trans. Electron Devices, vol.41, pp. 1257-1264, July,1994.
15. M. Bhatnagar and B. J. Baliga, "Comparison of 6H-SiC, 3C-SiC and Si for power devices", IEEE Trans. Electron Devices, vol. 40, pp. 645-655, March, 1993.
16. M. Hasanuzzaman, S. K. Islam, L. M. Tolbert and Burak Ozpineci, "Model simulation and verification of vertical double implanted (DIMOSFET) transistor in 6H-SIC", Int. J. Modeling and Simulation, vol.4, pp. 1-4, 2003.
17. Rajneesh Talwar and A.K.Chatterjee, "Estimation of power dissipation of a 4H-SiC Schottky barrier diode with a linearly graded doping profile in the drift region", Maejo International Journal of Science and Technology, vol.03, issue 02, pp. 352-36, 2009
18. S.M.Sze, Physics of Semiconductor Devices, John Wiely & Sons, New York, 1999 edition, p.81.
19. Vikram R. Vathulya, Huiling Shang and Marvin H. White, "A novel 6H-SiC power DMOSFET with implanted p-well spacer, IEEE Trans. Electron Device Letters, vol. 20, pp. 354-356, July, 1999.