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AREA-CONSTRAINED DESIGN OF DIFFERENTIAL INPUT STAGE FOR A TWO-STAGE COMPENSATED OPERATIONAL AMPLIFIER

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ABSTRACT

A new figure of merit under area constraints is proposed for designing optimum performance differential input stage of a two-stage compensated operational amplifier. Figure of Merit, FoM2 is defined that includes the three small signal performance parameters, namely input-referred noise, unity-gain bandwidth and differential dc gain. Expressions for these parameters in terms of area assigned, have been derived analytically and finally the expression for FoM2. It is shown how these performance parameters vary with the relative allocation of the total available area between the input and load transistors. The FoM2 is a peaking function of relative area allocation to the input transistors in the range of 64 % to 84 % of the total available area. The peak value of FoM2 and the minimum noise platform are functions of total available area. The total band noise for a given area is almost constant. These analyses are useful in developing CAD tool for the automatic synthesis of optimal differential input stage circuit design of an operational amplifier under area constraints.

Keywords

Area-Constraint Design; Thermal noise; Figure of Merit; Differential Input stage.

1. INTRODUCTION

The concept of Figure of Merit and one such Figure of Merit was proposed by the authors for the low frequency applications where flicker noise is the dominant noise [1]. This figure of merit is not suitable for the first stage of a two-stage compensated operational amplifier operating in mid frequency ranges for two reasons. One, at these frequencies, thermal noise dominates the flicker noise and secondly, the pole of the first stage has to be shifted towards left in order to provide proper splitting of poles.

Here, another figure of merit has been proposed for differential input stage of a two stage compensated operational amplifier operating at mid frequency that takes into account the maximization of differential gain with minimization of mean square noise with pole being shifted to as left as possible and is proposed to be given by:

$$FoM2 = \frac{Ad}{UGB * (IRN)^2} \quad (1)$$

where UGB is the unity-gain bandwidth, Ad is the differential dc gain and $(IRN)^2$ is the mean square Input-Referred thermal noise spectral density.

2. THERMAL NOISE MODEL FOR MOS TRANSISTOR

Each semiconductor device in the circuit introduces noise. Out of the various types of noises that could be possible in a device, thermal noise starts dominating at mid frequencies.

There exist numerous models for thermal noise in the MOS transistor [2,3,4,5,6,7,8,9,10]. According to the most popular model [8], the thermal noise due to a MOS transistor can be lumped as a voltage source at its gate and is given by

$$\overline{V_{eq}^2} = 4kT \cdot \left(\frac{2}{3g_m}\right) \cdot \Delta f \quad (2)$$

in the noise bandwidth of Δf and g_m is the device transconductance at the operating point.

However, the overall circuit noise depends on the circuit configuration.

2.1. Input-Referred Noise

The differential input stage amplifier is shown in Fig. 1.

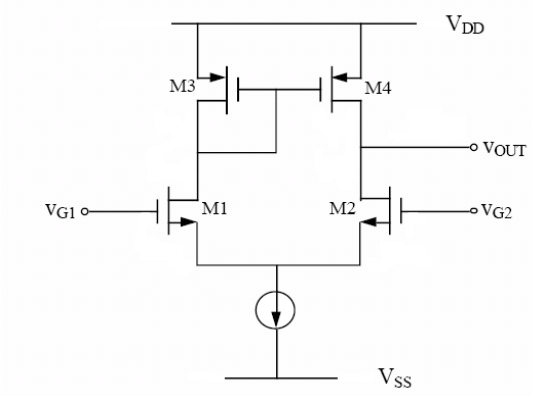

Fig. 1 Differential Amplifier.

If the noise in each MOSFET is represented by its equivalent input noise voltage generator as shown, the equivalent input thermal noise voltage of the circuit, $\overline{V_{eqT}^2}$ at input (gate of M1) can be given by the following equation [9]:

$$\overline{V_{eqT}^2} = \overline{V_{eq1}^2} + \overline{V_{eq2}^2} + \left(\frac{g_{ml}}{g_{mi}}\right)^2 \cdot \left(\overline{V_{eq3}^2} + \overline{V_{eq4}^2}\right) \qquad (3)$$

where $\overline{V_{eq1}^2}$, $\overline{V_{eq2}^2}$, $\overline{V_{eq3}^2}$, $\overline{V_{eq4}^2}$ are the noise sources at the gates of transistors M1, M2, M3 and M4. g_{mi} and g_{ml} are the transconductance of the input (M1 and M2) and load (M3 and M4) transistors, respectively, and are given by

$$g_{mi} = \sqrt{2 \cdot k_n \cdot \left(\frac{W_i}{L_i}\right) \cdot \left(\frac{I_o}{2}\right)}, \text{ and}$$

$$g_{ml} = \sqrt{2 \cdot k_p \cdot \left(\frac{W_l}{L_l}\right) \cdot \left(\frac{I_o}{2}\right)}. \qquad (4)$$

where W_i, W_l, L_i, and L_l are the widths and lengths of input and load transistors respectively, k_n and k_p are the process transconductance parameters for n-channel and p-channel MOS transistors, and I_o is the tail current of the differential amplifier.

Using equations (2), (3) and (4), the Power Spectral Density of noise at the gate of M1 is written as

$$S_{VG}^2 = \frac{\overline{V_{eqT}^2}}{\Delta f} = 4kT \frac{4}{3\sqrt{2 \cdot k_n \cdot (W_i/L_i) \cdot (I_o/2)}} \cdot \left[1 + \sqrt{\frac{k_p \cdot (W_l/L_l)}{k_n \cdot (W_i/L_i)}}\right] \quad \ldots (5)$$

Therefore, root mean square value of spectral power density better known as input-referred noise is written as

$$IRN = \sqrt{4kT \frac{4}{3\sqrt{2 \cdot k_n \cdot (W_i/L_i) \cdot (I_o/2)}} \cdot \left[1 + \sqrt{\frac{k_p \cdot (W_l/L_l)}{k_n \cdot (W_i/L_i)}}\right]} \qquad (6)$$

3. FORMULATION OF FIGURE OF MERIT, FOM2

Unity-gain bandwidth of the circuit, UGB is given by

$$UGB = \frac{g_{mi}}{2 \cdot \pi \cdot C_L} = \frac{1}{2 \cdot \pi \cdot C_L} \sqrt{\frac{k_n \cdot W_i \cdot I_o}{L_i}} \qquad (7)$$

where C_L is the total load capacitance at the output node. And the differential dc gain, Ad of the differential input amplifier given by

$$Ad = \frac{g_{mi}}{g_{di} + g_{dl}} = 2 \cdot \sqrt{\frac{k_n}{I_o}} \cdot \left(\frac{W_i}{L_i}\right) \cdot \left(\frac{1}{L_i}\left(\frac{dx_d}{dV_{DS}}\right)_n + \frac{1}{L_l}\left(\frac{dx_d}{dV_{DS}}\right)_n\right)^{-1} \quad \ldots (8)$$

where g_{di} and g_{dl} are the drain to source conductance of input and load transistors, respectively. The drain to source conductance g_d is approximated as

$$g_d = \frac{I_o}{2.L} \cdot \left(\frac{dx_d}{dV_{DS}}\right) \qquad (9)$$

where $\left(\frac{dx_d}{dV_{DS}}\right)$ (known as channel-length modulation parameter) is a process parameter [12] and its value has been taken as 0.1 μm/V for nMOS and 0.05 μm/V for pMOS transistors.

Substituting the values of UGB, Ad and IRN from Eqns. (6), (7) and (8) in (1), we get

$$FoM\ 2 = \frac{3.\pi.C_L \cdot k_n \cdot (W_i \cdot L_i)}{4.k.T.\sqrt{I_o}} \cdot \left[\left(\frac{dx_d}{dV_{DS}}\right)_n + \frac{L_i}{L_l}\left(\frac{dx_d}{dV_{DS}}\right)_p\right]^{-1} \cdot \left(\sqrt{k_n.W_i.L_i} + \frac{L_i}{L_l} \cdot \sqrt{k_p.W_l.L_l}\right)^{-1} \qquad (10)$$

4. MAXIMIZATION OF FIGURE OF MERIT UNDER AREA CONSTRAINTS

If A is the total area available for the devices in the differential amplifier, let us assign fraction x of A i.e. $x \cdot A$ to the input transistors and $(1-x)\cdot A$ to load transistors. Then, writing the expressions for UGB, Ad and IRN in terms of x, area (A), bias current (I_o) and technology parameters, we get

$$A_d = 2.\sqrt{\frac{2\cdot k_n \cdot (x\cdot A)}{I_o}} \cdot \left(\left(\frac{dx_d}{dV_{DS}}\right)_n + \frac{L_i}{L_l} \cdot \left(\frac{dx_d}{dV_{DS}}\right)_p \right)^{-1} \tag{11}$$

$$UGB = \frac{\sqrt{k_n . I_o \cdot (x\cdot A)}}{2\sqrt{2}.\pi \cdot C_L} \cdot \frac{1}{L_i} \tag{12}$$

$$IRN^2 = \frac{16.k.T}{3.\sqrt{k_n.(x.A).I_o}} . \frac{1}{L_i} . \left(1 + \frac{L_i}{L_l} . \sqrt{\frac{k_p.(1-x)A}{k_n.(xA)}}\right) \tag{13}$$

Hence, from Eqns. (1), (11), (12) and (13) figure of merit $FoM\,2$, in terms of x, area (A), bias current (I_o) and technology parameters is written as

$$FoM\,2 = \frac{3\pi.C_L \cdot k_n \cdot (xA)}{4kT \cdot \sqrt{I_o}} . \left(\sqrt{k_n.(xA)} + \frac{L_i}{L_l} . \sqrt{k_p.(1-x)A} \right)^{-1} \cdot \left[\left(\frac{dx_d}{dV_{DS}}\right)_n + \frac{L_i}{L_l}\left(\frac{dx_d}{dV_{DS}}\right)_p \right]^{-1} \tag{14}$$

From (14), following conclusions can be drawn

- Figure of Merit, $FoM\,2$ is dependent on technology parameters *i.e.* process transconductance parameters, k_n for n-channel transistor k_p for p-channel transistor and device channel length modulation parameters, $\left(\frac{dx_d}{dV_{DS}}\right)_n$ for n-channel transistor, and $\left(\frac{dx_d}{dV_{DS}}\right)_p$ for p-channel transistor.
- To maximize $FoM\,2$ for a given load C_L, length of input transistor L_i should be kept minimum for a given area A, as it maximizes all the three product terms wherever it appears.
- Length of load transistor L_l should be as large as possible under the constraints of area since it maximizes the last two product terms and hence maximizes Figure of Merit $FoM\,2$.
- Figure of Merit is independent of the width of load transistor, W_l hence should be kept as minimum.

5. ANALYTICAL RESULTS

The variation of differential dc gain as a function of relative area allocated to input transistors at different values of total area is shown in figure 2. It is clear that it increases with increasing area allocation to input transistor and peaks at a certain value of x. Also, as the total area increases, the peak value of differential dc gain increases. The peak value of dc gain is obtained for x in the range of 0.6 to 0.8. Fig. 3 shows that the unity-gain bandwidth is a monotonically increasing function of x.

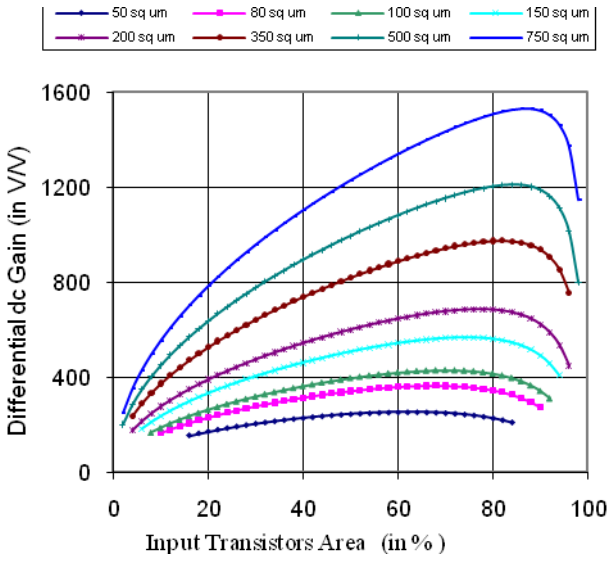

Fig. 2 The Differential dc Gain as a function of input transistor area.

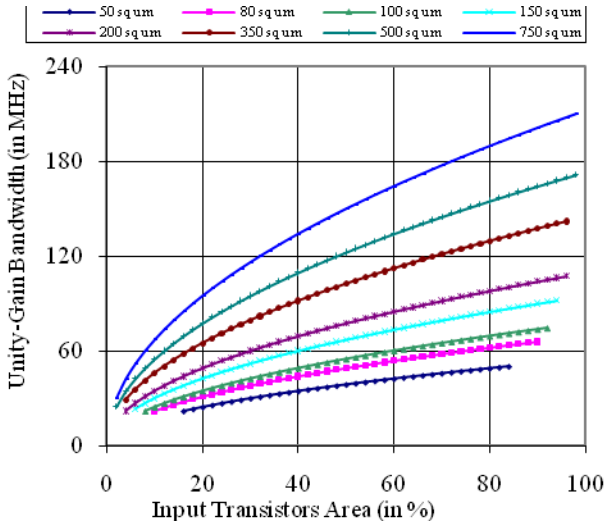

Fig. 3 Unity-Gain Bandwidth (in MHz) as a function of input transistor area.

The variation of input-referred noise as a function of X is shown in Fig. 4. For larger values of X, the noise is reducing because with increasing X the gate area of input transistors is increasing and their noise contribution is decreasing.

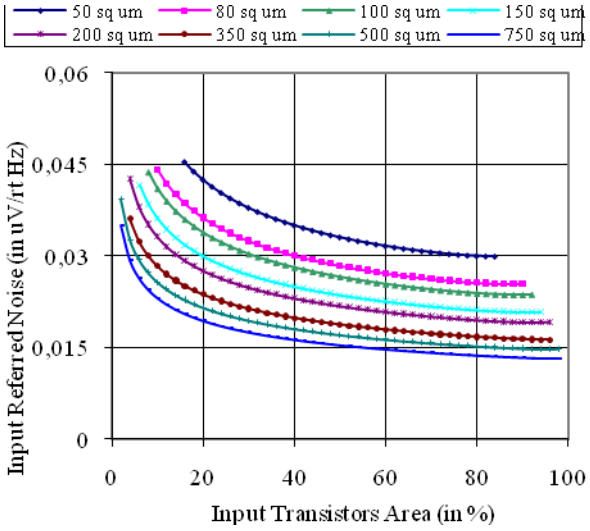

Fig. 4 Input-Referred Noise (in nV/rt(Hz)) as a function of input transistor area.

Fig. 5 shows the total band noise as a function of X for different values of A. It is interesting to note that the total band noise remains almost constant for all the values of A. It implies that by allocating more area to the input transistors, the unity-gain gain bandwidth of the circuit can be increased with reduced input referred noise such that the total band noise is almost the same.

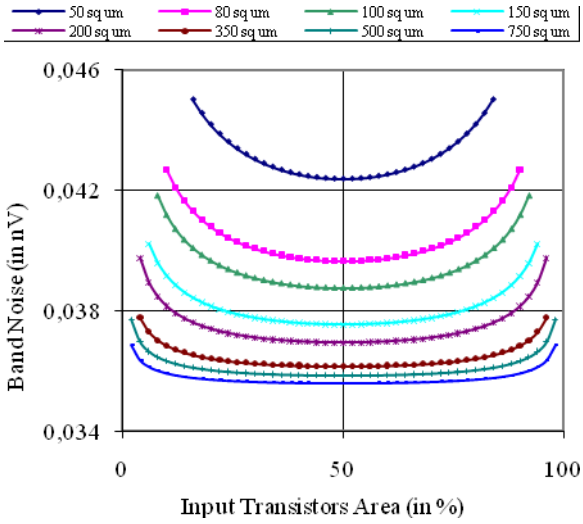

Fig. 5 Total Band noise (in nV) as a function of input transistor area.

Next the figure of merit, FoM2 is plotted as a function of percent area allocated to input transistors. Figure of Merit is a peaking function of X in the range 64% to 84% as shown in Fig. 6. It is clear that figure of merit increases with total area A. It also indicates that for a fixed value of total area, about how much percent of total area should be assigned to input transistors to obtain a maximum value of Figure of Merit. Peak value of figure of merit, FoM2 as a function of total area is plotted in Fig. 7.

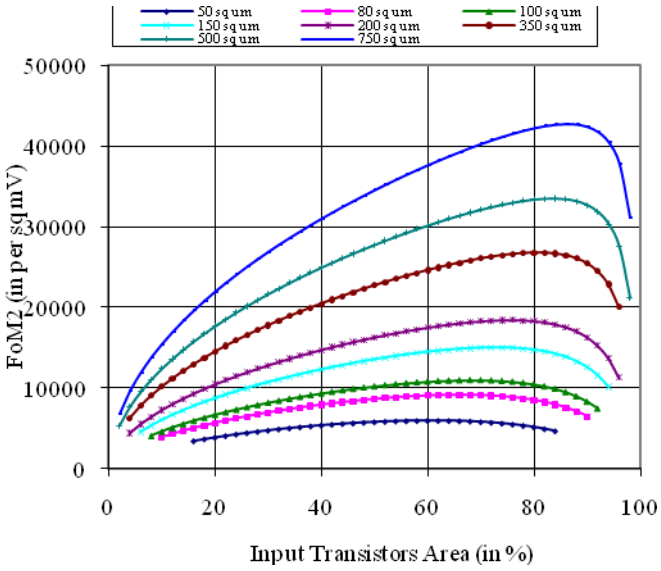

Fig. 6 The FoM2 as a function of input transistor area.

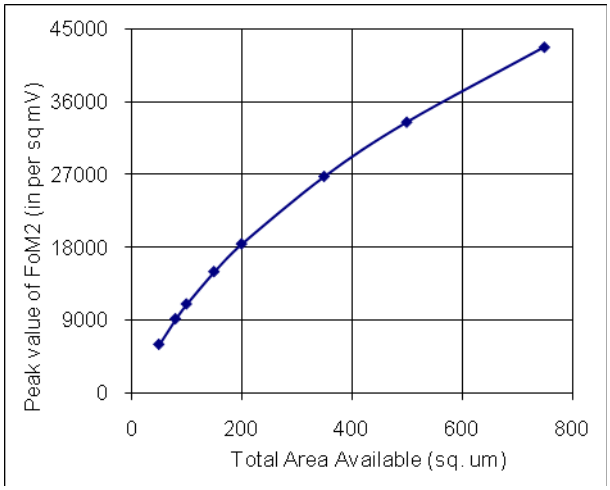

Fig.7 Peak value of FoM2 as a function of total area.

Fig. 8 indicates that for a fixed value of total area, there is a minimum value of band noise present in the circuit. It implies that if the total area of the circuit is reduced the noise platform may increase exponentially beyond a point. It is also clear that one cannot lower the noise platform beyond a limit, whatever large area is assigned to the circuit.

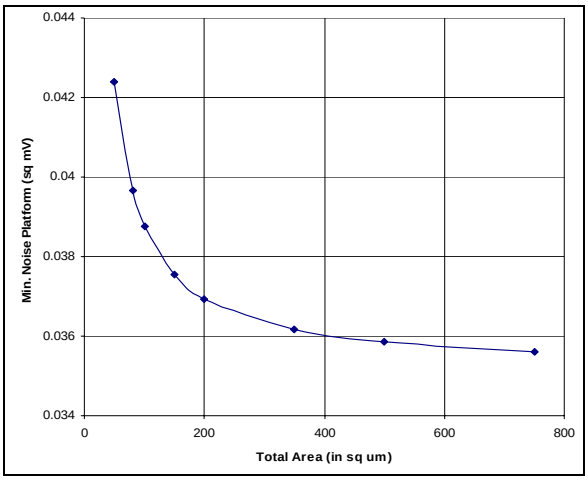

Fig.8 Minimum Noise platform as a function of total area.

6. SIMULATION RESULTS

Circuit simulations using TSpice, also validated the analytical results. To perform this task, a value of total area was chosen. The total area was divided between input and load transistors in a predefined ratio. Then for this distribution of areas all combinations of aspect ratio of input and load transistors were simulated to obtain the differential dc gain, unity-gain bandwidth and input-referred noise.

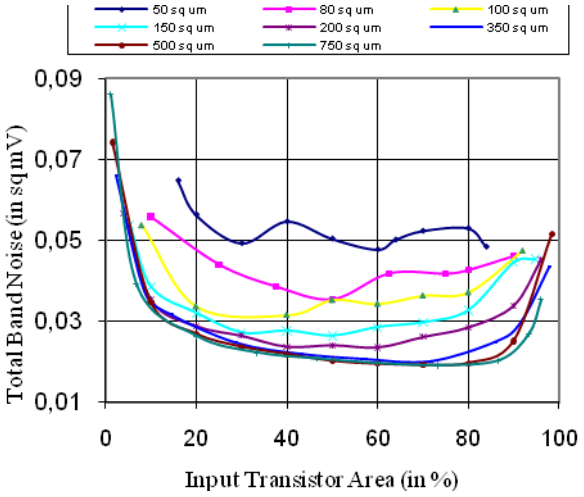

Fig.9 Simulated plot of total band noise as a function of area.

The total band noise and the figure of merit were computed from these parameters. The total band noise and peak figure of merit as a function of input transistor area in percent (ratio of area allocated to input transistors to the total available area, A) for various values of total area are plotted as shown in figs. 9 & 10, respectively. These plots match well with the analytical results shown in previous section.

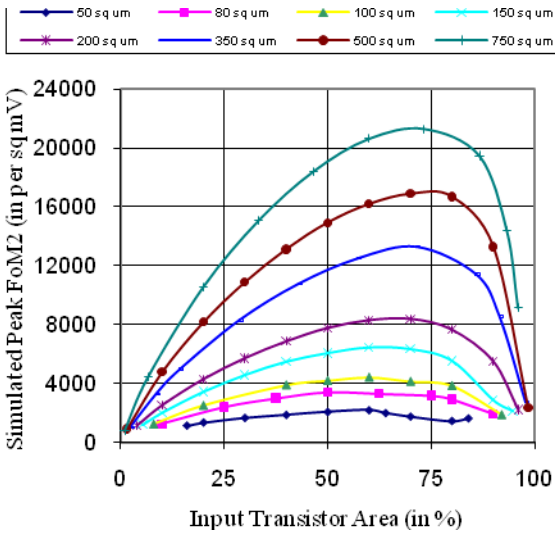

Fig.10 Simulated plot of figure of merit as a function of area.

In order to demonstrate the utility of figure of merit as a tool to optimize the design, we define three new parameters as follows:

Ad% -- Differential dc gain at peak figure of merit as a percentage of maximum differential dc gain achievable for a given area.

BN% -- Band Noise at peak figure of merit as a percentage of minimum Band Noise achievable for a given area.

Table I compares the analytical and simulated values of peak figure of merit FoM2, Ad%, BN% for constant area.

7. CONCLUSION

The proposed concept is a suitable tool for synthesizing optimal design of differential input stage of a two-stage compensated operational amplifiers under area constraints and leads to the realization of differential dc gain, unity-gain bandwidth and input-referred noise values that are also very close to their individually achievable best values under the same area constraints. The above analyses validate that idea of FoM may be deployed in a CAD tool for automatically synthesizing the differential input stage amplifiers and can be extended for many other building blocks. The paper also highlights that the total band noise for a given area is almost constant.

Table I. Comparison Between Analytical and Simulated Performance at Peak Figure of Merit

Area (μm^2)	Peak Figure of Merit, FoM2 (per sq mV)		Ad%		BN%	
	Analytical	Simulated	Analytical	Simulated	Analytical	Simulated
50	5973.92	2202	99.84	95.69	100.31	100
80	9136.22	3438.2	99.92	77.93	100.63	100
100	10981.2	4397.7	99.88	83.5	100.67	100
150	14990.2	6454.6	99.85	79.97	100.71	100
200	18423.9	8385.4	99.99	82.72	100.84	100
350	26776.3	13279	99.9	83.51	100.72	115.3
500	33501.5	16885	100	87.45	100.74	120.7
750	42781.4	21303	100	87.0	100.6	116.7

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REFERENCES

1. Alpana Agarwal & Chandra Shekhar, "Figure-of-Merit-Based Area Constrained Design of Differential Amplifiers," VLSI Design, vol. 2008, Article ID 847932, 5 pages, 2008. doi:10.1155/2008/847932.
2. A. van der Ziel, "Thermal noise in field-effect transistors", *Proc. IEEE*, vol. 50, pp. 1808–12, August 1962.
3. A. van der Ziel, "Gate noise in field-effect transistors at moderately high frequencies", *Proc. IEEE*, vol. 51, pp. 461–465, Mar. 1963.
4. G. Nicollini, D. Pancini, and S. Pernici, "Simulation-Oriented Noise model for MOS Devices", *IEEE Journal of Solid-State Circuits*, vol. SC-22, no. 6, pp. 1209-12, Dec. 1987.
5. Y. Tsividis and G. Masetti, "Problems in *IEEE* precision modeling of the MOS transistor for Analog Applications," *IEEE Trans. Computer-Aided Design*, vol. CAD-3, pp. 72–79, Oct. 1984.
6. R. M. Fox, "Comments on Circuit Models for MOSFET Thermal Noise", *IEEE Journal of Solid-State Circuits*, vol. 28, no. 2, Feb. 1993.
7. B. Wang, J. R. Hellums, and C. G. Sodini, "MOSFET Thermal Noise Modeling for Analog Integrated Circuits", *IEEE Journal of Solid-State Circuits*, vol. 29, no. 7, July 1994.
8. P. R. Gray and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, Third Edition, Wiley, 1993, pp 765 - 767.
9. B. J. Sheu, D. L. Scharfetter, P. K. Ko, and M. C. Jeng, "BSIM: Berkeley short-channel IGFET model for MOS transistors," *IEEE Journal of Solid-State Circuits*, vol. 22, no. 4, pp. 558-566, Aug. 1987.
10. K. K. Hung, P. K. Ko, C. Hu, and Y. C. Cheng, "A physics-based MOSFET noise model for circuit simulators," *IEEE*

Trans. Electron Devices, vol. 37, no. 5, pp. 1323 – 1333, May 1990.

11. P. R. Gray and R. G. Meyer, *Analysis and Design of Analog Integrated Circuit*, Third Edition, John Wiley & Sons, 1992, pp. 68, 156-158.
12. K. L. Clark, *Negations as failure*, *Logic and Data Bases*, eds. H. Gallaire and J. Winker (Plenum Press, New York, 1973), pp. 293–306.