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Minimal Fractional Design in a Semiconductor Manufacturing Line

Jean-Yves Rosaye Ph.D
Spansion Inc.
5204 East Ben White Boulevard, MS 613, Austin, TX 78741 USA
jysros@gmail.com

Mot clefs: Robust engineering, process optimization, capacity index C_p/C_{pk}, DOE L8/L18 arrays

Abstract: Processes need to be optimized and product variations reduced. However, experiment or parameters are scarce, design rules not followed and if variability is evaluated, this is nothing more than with C_p/C_{pk} or standard deviation Furthermore, because of the scaling reduction, optimization and design become of first concerns even in restricted conditions such as minimal "fast" experiments. With Excel and only simulation is proposed a method used for process control to deal with charge loss, improve C_p/C_{pk}, study wafer position dependency and etching uniformity in margin evaluations. DOE is modified to fit for minimal "fast" experimentation. JMP, APC, six sigma or other methods exist but they are for larger projects and costly methods. In the case of minimal fractional design, a simple DOE combination, S/N comparison with Excel is by far easier and enough precise. A new approach is proposed from simulation of experiment to statistical planning to lead to better process optimization against overall source of variation, especially charge loss correlated with dangling bonds Si-H at the Si/SiO_2 interface.!

I) Introduction

Charge loss in memory products is directly related to leakage current from defects near or at the Si/SiO_2 interface in silicon dioxide for TNOX, GOX and ONO structures [1, 4]. Statistical evaluations by reducing variations are addressing the source of failure depending on noise, not always a defect current, and temperature is the most influent parameter [3, 5, 6]. Structures concerned are NOR and NAND memories and several experiments were performed:

Technology	Objective	Data	Solutions
NOR memory with floating gate	Charge Loss reduction	ECN (Engineering Change Notice)	Combination of DOE and S/N ratios.
NOR memory shrink with floating gate	Root cause of C_p/C_{pk} > 1.33	Online data and index C_p/C_{pk}	Online simulation of experiments
NAND and ONO NOR memory	Optimum parameter setting	Wafer position uniformity evaluation	Corrective action confirmation of effectiveness

Tab 1: Three experiments were performed, one simulation, one online Taguchi design and one case study.

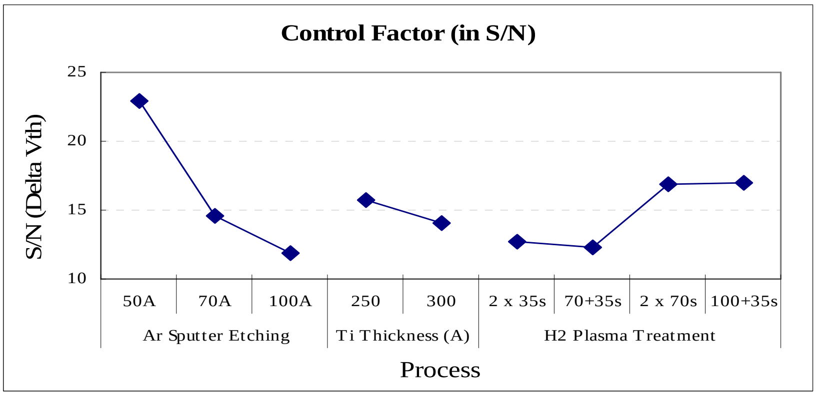
II) Simulation of experiment

Charge loss improvement comes from process optimization. Wafer position is the noise factor, S/N ratio comes from SORT Yield [S/N③= -10log1/y, y= yield (%)] and zero charge loss target S/N②. With a few data or parameters, analysis is easy to perform from traditional DOE [7, 8] to combinations of L8 and L18 orthogonal arrays by using already known data [9].

Experiment	A	B	C	*N1*	*N2*	*N3*	*N4*	*N5*	*N6*	*N7*	*N8*	*N9*	S/N①	S/N②	S/N③	*Average*
1	*3*	*1*	*1*	277	300	294	263	244	225	253	272	263	12.8	-48	-2.04	400
	second wafer			100	150	253	269	159	38	97	363	325				
2	*3*	*2*	*3*	192	325	288	369	213	250	294	425	291	11	-51.5	-1.59	600
	sd wf			544	288	232	356	338	300	566	513	497				
4	*1*	*2*	*3*	285	263	297	306	291	281	344	288	307	22.9	-50	-1.37	300
5	*2*	*1*	*2*	244	244	266	306	291	344	272	288	294	16.5	-49.5	-1.33	300
	sd wf			202	188	369	263	234	306	251	269	275				
7	*2*	*2*	*2*	314	281	201	281	256	244	363	656	341	8.2	-50	-1.41	300
	sd wf			160	325	316	281	225	113	106	231	229				
8	*2*	*1*	*3*	225	306	188	263	235	306	219	269	275	16.7	-50	-1.52	300
	sd wf			250	306	356	263	254	263	303	244	247				

Tab 2: Noise factor is charge loss (ΔV_{cl}, mV) from N1 to N9 wafer position.

Process optimization was investigated for three parameters because of charge loss from overall noise analysis. Standard deviation, average (S/N ①) and yield S/N ratios are obtained: charge loss is reduced to zero, conformed to average or lead to best yield as three quality targets. Two partial DOE evaluated parameter weights by Excel. Only six experiments were performed, but if several simulations lead to same relative weights and if the merit of optimization is proved, that is enough. Experiment No. 5 and 8 are judged as best. S/N ① calculation confirms No. 5 is good but the best solution remains split No. 4 (highest S/N). From charge loss wafer average data and other S/N ②, or S/N ③ evaluations, there is no contradistinction for best split No. 4. If S/N ② for split No. 1 is good, wafer average value is not: average real value based on noise data is the lowest value. Judgment needs to be independent of wafer average for charge loss evaluation or it leads to wrong evaluation by S/N ② formulae. Then, S/N ① and S/N ③ are more relevant ratios and confirm experiment 5 is good. Two DOE must be combined in a simulation of experiment without complete DOE orthogonal array.



Graph 1: S/N (optimized) – S/N (normal) = 25.7 db – 10.6 db = 15.1 db

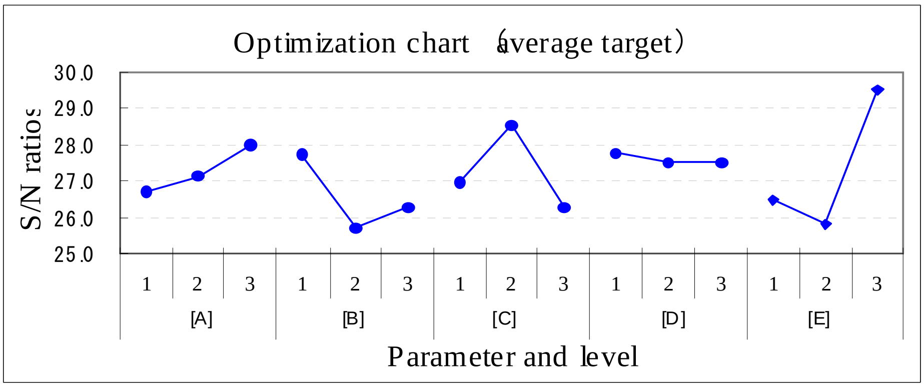
Precision is about 1 db and compensated by a large 15db gain. It shows optimization was important to achieve concerning charge loss, which justifies process statistical re-evaluation.

III) Online design of experiments

In NOR memory shrink, process FICD measures have often C_{pk} inferior to 1.33. However, goal is to reduce variations and identify their sources: SPC assignment is C_{pk} >1.33 and sources of variation are critical for failure. Average target S/N ① is examined as FICD target is 100 nm, authorized disposition limits are ±20 nm and parameter level set-up to $X_0 \pm \sqrt{3/2}\,\sigma$ [10].

Process	Level 1	Level 2	Level 3	$\sqrt{3/2}\,\sigma$ (%)
[A]	135 nm	140 nm	145 nm	3.5
[B]	139 nm	145 nm	151 nm	3.5
[C]	465 Å	475 Å	485 Å	2
[D]	510 Å	520 Å	530 Å	2
[E]	65 nm	70 nm	75 nm	7

Tab 3: Level parameter setting, this is genuine setup not simulation of experiments, using online data



Graph 2: S/N (L18 optimized) – S/N (normal) = 25.6 db – 33.1 db = 7.5 db

Parameters C and D are already optimized, but not A and B. Normal conditions are seen as not very good conditions but optimization is not so severe critical here (less than 8 dB). Trends in A, B, and E parameters can be seen as not optimized. Correlation between parameters is examined to identify root cause of variation due to none optimized conditions. Information gained by this investigation of online data was effective for the exact root failure determination even if a statistical evaluation is only studying parameter correlation to find most influent parameters and their relationships [11]. Other tools can be efficient than only Excel, especially R tool for confirmation of results in robust engineering [12].

IV) Optimum parameter setting

In Manufacturing, parameters with only two levels are not enough because interactions between parameters are not examined. On the contrary, Taguchi array is using three parameter levels, a better design but more experiments are necessary. However, using partial DOE together with complete two levels DOE i.e. combine relative information given by three levels and information given by two is the idea. This is confirmed by factorial DOE analysis, which recommends not satisfying with only 2 level parameters even if this is easier [13]. A failure in wafer edge (case study) asked for a corrective action as same as optimization of parameters and equipment set-up: thickness uniformities in four cases were compared.

	Signal on Noise definitions
S/N (1)	Over Etch Step Al E/R (N1 to N9 wafer sites)
S/N (2)	TiN rate/uniformity (etching quantity in nm/min)
S/N (3)	FICD/CD Bias (CD bias = FICD – DICD lentghs)
S/N (4)	Al top notch/Bottom notch (in nm)

Tab 4: Uniformity issues (margin insufficiency) leading to over etch process optimization.

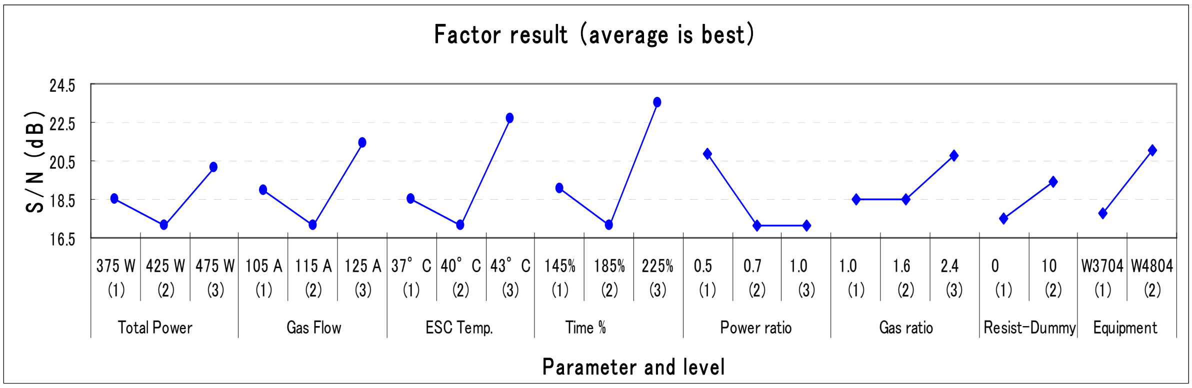
Without Taguchi design, S/N ratios were close, 19.5 until 21.9 dB: traditional ANOVA "fast" variation analysis could not be effective. It was observed conditions 2 and 3 were not optimized:

S/N1 (optimization) – S/N (currently) = 26 db – 24 db = 2.0 db

S/N2 (optimization) – S/N (currently) = 30 db – (–1) db = 31 db

S/N3 (optimization) – S/N (currently) = 14 db – 4 db = 10 db

S/N4 (optimization) – S/N (currently) = 35 db –35 db = 0 db



Graph 3: Result from TiN over-etching show optimization is far from being achieved (SN2 = 31db).

Another method is to uses JMP, which with factorial DOE govern traditional DOE in the US. It was an alternate method for this third experiment because there were as many as eight parameters, which leads to complex combination: eight parameters is the limit of L8/L18 arrays.

Conclusion

This is necessary to find an adequate design even in the case of minimal experiments. If simulation depends on already introduced data, DOE plan is however previous to experiments.

Fractional DOE can be viewed as suitable if there are at least two fractional DOE to reinforce precision, which might be questionable from a more formal statistical viewpoint, but is most an empirical approach: seven experiments have shown it is working and justified by S/N differences between optimized and normal conditions. For example, new experiments were necessary for experiment 1 as it was far from, being optimized from charge loss, as it is quoted "If your experiment needs statistics, you ought to have done a better experiment …" Lord Rutherford. Nowadays, Six Sigma (DMAIC) is also proposing global DOE solutions [14].

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