Journal of Electron Devices, Vol. 2, 2003, pp. 62-64
ã JED [ISSN: 1682 -3427]

Journal of Electron Devices
www.j-elec-dev.org

PARAMETERS DEGRADATION OF VDMOSFET DURING OPERATION UNDER NATUREL STRESS

Wahiba TAZIBT [1], Roland HABCHI[2], C. SALAME[2], B. NSOULI[3], A. Khoury [2], P. MIALHE[1]

[1]LP2A, 52 av de Paul Alduy, 66860 Peprignan cedex, France

[2] CEA -LPSE, Faculty of SciencesII, Lebanes e University, 90656 Jdeidet El Mten, Lebanon

[3]Lebanese Atomic Energy Commission, CNRS, Beirut Lebanon

Abstract

In this work, we have studied the evolution of the electrical properties of the Body-Drain N-channel VDMOSFET submitted to gate oxide electrical stresses.
Constant voltage stresses at V_G =68V led to an important variations of transistor parameters as well as for the integrated pn junction.

A reduction in the transconductance and drain current correlated to an increase of the stress time was detected and associated to an increase in the interface state density. The junction diffusion voltage reduction was explained by the positive charge trapped in the gate oxide.

I. INTRODUCTION

Electrical stress technique can be used to simulate and evaluate natural ageing and its resulting parameters degradation of the device when the later found to operate under normal conditions.

Two categories of electrical stress can be used to study the progressive build-up of defects responsible for the deterioration of the MOSFET structure: uniform carrier injections by imposing a constant current or a constant voltage through the oxide, or hot carrier injections generated either in the channel or in the substrate of a MOSFET[1–2]. It is believed that, in both cases, the degradation results from one mechanism linked to energetic electrons and not oxide electric field [3-4]. Theories and mechanisms of defect generation are discussed elsewhere [5],[6]. In [7], microscopic aspects of oxide degradation were treated and modelled. In this paper, we will show some experimental data revealing the effects of degradation over the standard VDMOS characteristics, such as I-V curve and junction current.

II. EXPERIMENTAL SET UP

The devices used in this study were BUK556 commercial n-channel power VDMOSFETs built in a standard Si gate technology and capsulated in standard TO-220 plastic cases. The manufacturer's data sheet indicates a drain-source breakdown voltage up to 60V and a gate-source maximum voltage of 20V. Devices were electrically characterised before stress and then each one was subjected to constant voltage stressing by applying positive DC bias to the gate electrode with drain and source terminals grounded. To prevent oxide sudden breakdown, gate voltage was gradually increased by steps of

1V/s up to the desired value. All experiments were done at room temperature.

II I. EXPERIMENTAL RESUL TS

The evolution of electronic properties of the investigated power MOSFETs structure was sensed after each dose of stress by recording both the standard I-V curve set of the transistor, and the direct junction current.

In Fig. 1 we present the typical change of the I_{DS}-V_{DS} curve for N-VDMOSFET in saturation regimes, after a constant voltage stress (CVS) and we have obtained relatively, an important decrease of the drain saturation current.

This degradation indicates interface state creation influencing channel carrier mobility.

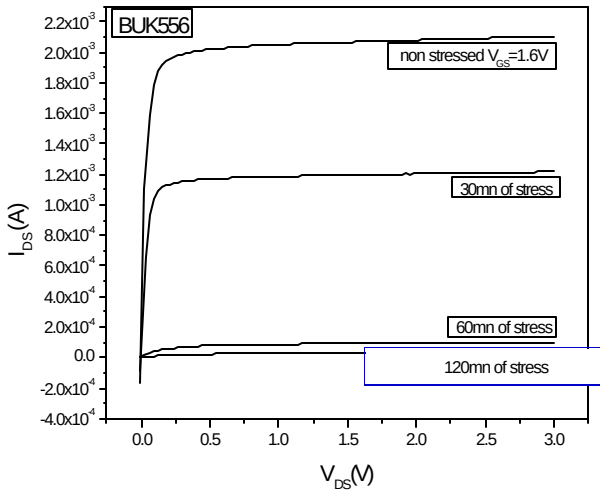

Figure 1. I_{DS}-V_{DS} curve before and after different doses of stress.

Results obtained with direct junction current (Fig2) indicate a positive trapped charges in the gate oxide that modifies the surface potential by creating an inversion layer at the interface Si/SiO2. These inversion layers (electrons for n-MOSFET) have a similar effect on the body drain junction as the channel effect.

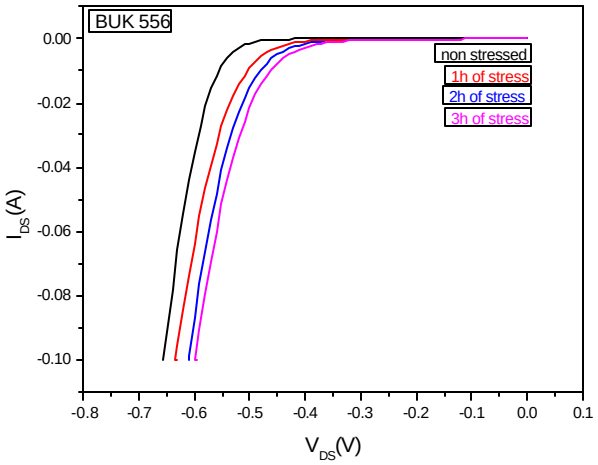

Figure 2. Direct junction current variation.

As can be seen, the use of electrical stress leads to a remarquable increase of both oxide traps, and interface state densities.

IV. CONCLUSION

The gate oxide DC electrical stresses effects on the electrical characteristics of the n-channel of power MOSFET were studied.

The transconductance and the drain current show a decrease correlated to an increase with the stress time and the phenomenon was associated to an increase in the interface state density.

The built in voltage of the pn junction reduction was explained by the positive charge trapped in the gate oxide.

The integrated Body –Drain pn junction, was shown to be affected the interface potential variation due the gate electrical stress.

V. REFERENCES

[1]E.M. Vogel et al. Ultrathin silicon dioxide under combined substrate hot-electron and constant voltage tunneling. IEEE Trans. Electron Dev. ED-47 (2000) 1183.

[2]D. Zander et al. Creation and thermal annealing of interface states induced by

uniform or localized injection in 2.3 nm thick oxides. Microelectronics Reliability 41 (2001) 1355-1360.

[3] D.J. DiMaria, Defect generation under substrate-hot-electron injection into ultrathin silicon dioxide layers. Journal of Applied Physics 86 (1999) 2100.

[4] F. Lime, Stress induced leakage current at low field in ultra thin oxides. Microelectronics Reliability 41 (2001) 1421-1425.

[5] K.Hess et al.Theory of channel hot-carrier degradation in MOSFETs. Physica B 272 (1999) 527-531.

[6] J.H.Chen et al. Breakdown and stress-induced oxide degradation mechanisms in MOSFETs. Solid –StateElectronics 46 (2002) 1965-1974.

[7] R. Ferruglio et al. Microscopic aspects of defect generation in SiO_2. Microelectronics Reliability 42(2002) 1427-1432