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ANALYSIS AND MODELING OF THE EFFECT OF STATISTICAL FLUCTUATIONS ON (6T) NANO-CMOS SRAM CELL STABILITY

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ABSTRACT

Static RAM cells are among the most important fundamental blocks of digital circuits. These cells go through considerable statistical fluctuations as a result of scale change of the bulk-CMOS technology to nanometer scales. Thisscale change is aimed to increase data storage density. It also influences static RAM stability significantly. In this research, the statistical sensitivity of static noise margin was analyzed in non-ideal conditions and the statistical stability of SRAM cells was examined to recognize weak cells.

Keywords: Static Noise Margin (SNM) , Random Dopant Fluctuations (RDF) , Line Edge Roughness (LER) , Polysilicon Gate Granularity (PGG).

I. INTRODUCTION

As the size of bulk-CMOS transistors reaches nanometer scales, statistical variations [1, 2] of devices are turned into a significant problem in the design of next generation circuits. In most circuits made of a large number of identical nominal transistor pairs, a lack of conformity between parameters of transistor pairs leads to a reduction in the constructability and reliability of the designed circuit. Analysis of statistical fluctuations is vital to the functionality of circuits used in pioneer technologies [3]. The effect of these variations on SRAM cell transistors causes destructive and stable defects, which do not completely damage cells. The rotatory mode is also a result of some specific operational conditions. Cells with such defects are known as weak cells with inadequate noise margins [4, 5]. Six-transistor (6T) CMOS SRAM cell(Fig. 1) is composed of two mutual connected inverters and two access transistors. Q1 and Q2 are the driver transistors with the largest role in maintenance of cells. Q3 and Q4 are also load transistors and are used as loads for Q1 and Q2. Finally, Q5 and Q6 are access transistors responsible for reading and writing in cells.

In this study, a new method based on cell static noise margin (SNM) was used to deal with the statistical fluctuations of random, systematic and environmental parameters. In this method, 1000 sample transistors of N and P types from the closed BSIM4 model with a gate length of 35nm and unique structures composed of statistical variation sources (RDF, LER, and PGG) were substituted for SRAM cell transistors. In fact, 1000 random netlist files were created for the HSPICE simulator. Each file was

an SRAM cell with a unique structure made of intrinsic parameters. One SNM was extracted for each file which enabled the authors to perform mean analyses of SNMs of the first moment (i.e. Normalized Standard Deviation) and the second moment (Skew). It also enabled them to examine SNM values.
This Monte Carlo simulation method produces highly precise results because the closed BSIM4 models used in this method are derived from the numerical simulation of the device by considering quantum physics limitations. Note that the more the number of randomly generated netlists, the higher is the precision of this method. Fluctuations are basically divided into the following categories: random, systematic, and environmental. In the following, the effect of each type of fluctuation on SRAM 6T cell stability is studied. Note that all measurements were conducted with read access permission.

II. RANDOM FLUCTUATIONS

These fluctuations are highly dependent on transistor size and become extremely unpredictable at Nano scale. These fluctuations are also among the main limitations imposed on the precision of functionality of circuits in the design of integrated circuits [6,7]. The main sources of these fluctuations include RDF, LER and PGG. As seen in Figure 2, these sources form the main source of variations of the transistor threshold voltage [8].

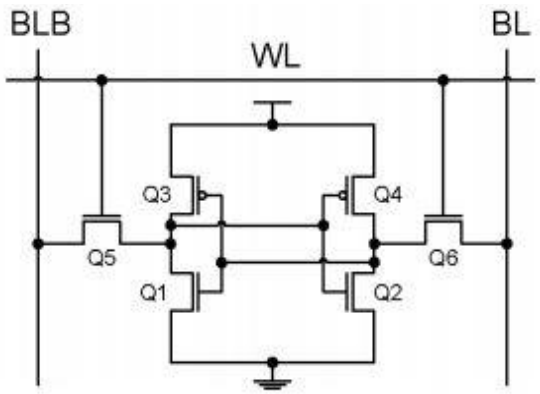

Fig.1: Six-transistor(6T) CMOS SRAM cell.

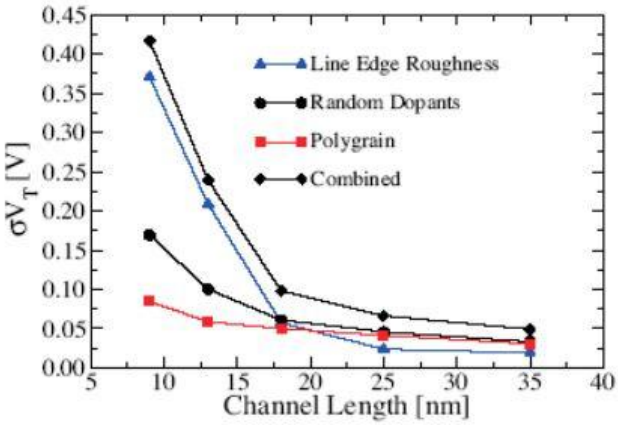

Fig.2: Standard deviation of threshold voltage variation vs.channel length, for square planar bulk MOSFETs. Constant gate line edge roughness (4 nm) is assumed [3].

Figure(3-a) shows the SNM mean deviation for changes of the threshold voltage of SRAM cell transistors. As seen in this figure, fluctuations of VTH of driver transistors have the highest effect on cell stability. These fluctuations are the result of a higher $\frac{W}{L}$ ratio as compared to that of other cell transistors.

A reduction in the access transistor VTH also facilitates access to the cell and leaves a negative significant effect on SNM. The reason is that in the cell accessed for reading/writing data, access and load transistors are strongly shunted and thus adversely affect the low mode of the cell. Figure (3-b) shows the normalized mean standard deviation. Considering the aforementioned reasons and Figure (3-b), fluctuations of VTH of driver transistors lead to a considerable change in SNM variations. Figure (3-c) shows SNM skew. In this figure, driver transistors demonstrate the highest (67%) deviations in the second SNM moment, respectively. Figure (3-d) shows SNM distribution with 100% of deviation from the typical value of driver transistors threshold voltage. Accordingly, the highest SNM distribution occurs at 0.116.

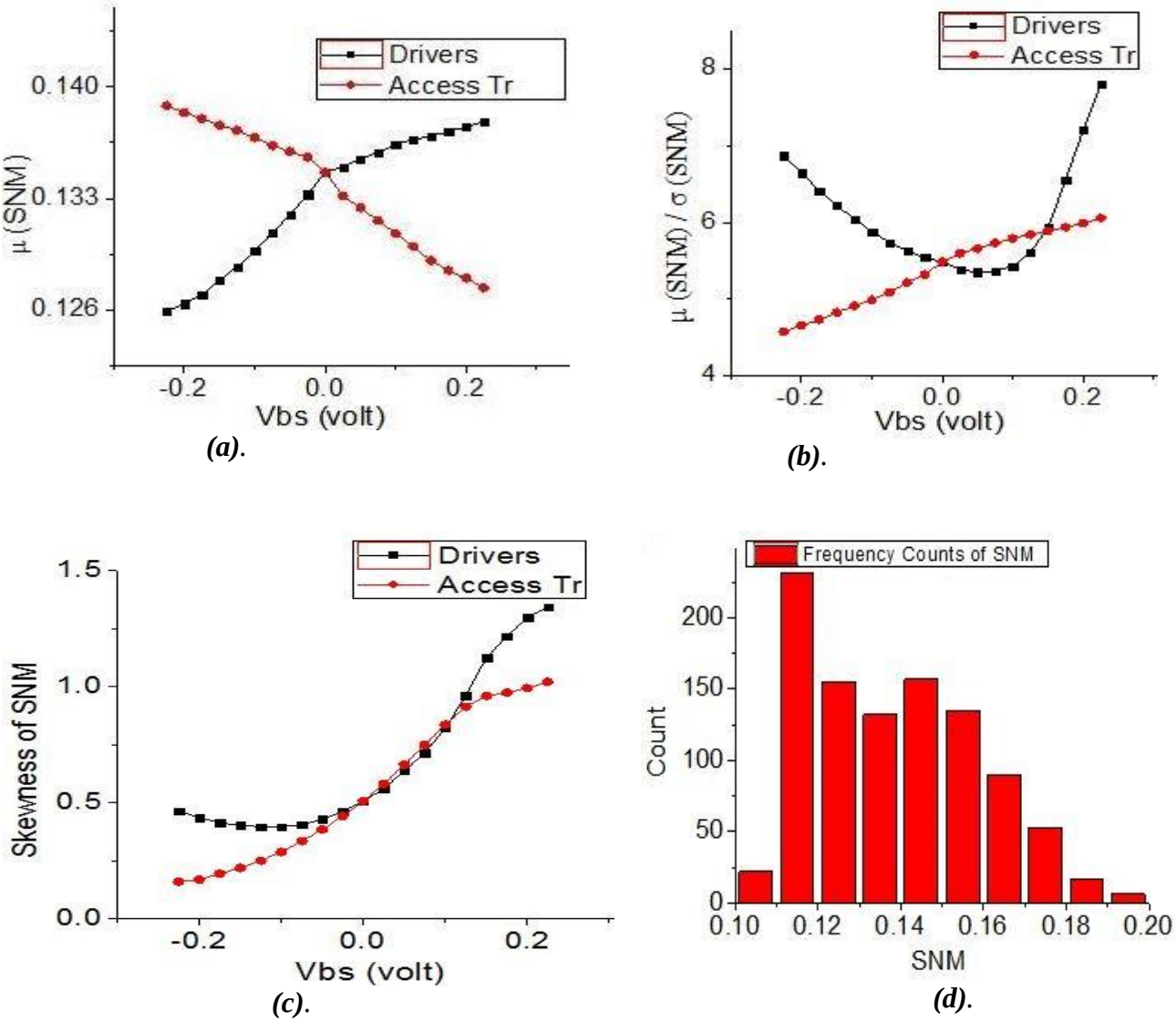

Fig. 3: Impact of VTH (Vbs) deviations on SNM **(a)**:SNM mean deviation - **(b)**:normalized standard deviation of SNM - **(c)**:SNM skew - **(d)**:SNM distribution.

III. SYSTEMATIC FLUCTUATIONS

This group of fluctuations is strongly related to the construction process, layout position and layout typology. This relationship results from lithography, mask errors and lens distortion. In order to study the SRAM cell SNM destruction caused by these errors, Carafe is used as an inductive fault analysis tool [9]. Carafe works by widening and constricting paging geometries. Faults identified for the SRAM cell were modeled for failures in the form of series and parallel resistance. A list of faults was also modeled using the HSPICE circuit simulation tool. There is a high possibility of failure with the absence of connection as well as in weak connections, VIAs and silicides [10, 11].

SNM deviation is a function of resistance of the most probable failures. As seen in Figure (4-a), increased resistance has an adverse effect on the SNM cell. That is to say, with increased resistance, SNM is destructed and data storage becomes defective. As seen, failure in the connection between SRAM cell and the ground has the highest adverse effect on SNM while failure in the drain of load transistors and the driver has a considerable effect on data storage. However, failure in driver transistor gates does not considerably destruct SNM due to the high resistance of the gates. Figure (4-b) shows the

relevant normalized standard deviation. According to this figure, as a result of a failure of 10MΩ in the cell ground, SNM variations are reduced to zero while failures below 10MΩin the driver transistor gates do not cause any change to the SRAM cell SNM due to the high resistance of gates. Failures higher than 10MΩ lead to changes in SNM. Figure (4-c) shows SNM skew. According to this figure, the highest deviation is associated with the failure in the cell ground while the lowest deviation is caused by the failure in driver transistor gates. Figure (4-d) shows the SNM distribution for the 40MΩ failure of driver transistors gates. In this figure, the highest SNM distribution occurs at 0.106.

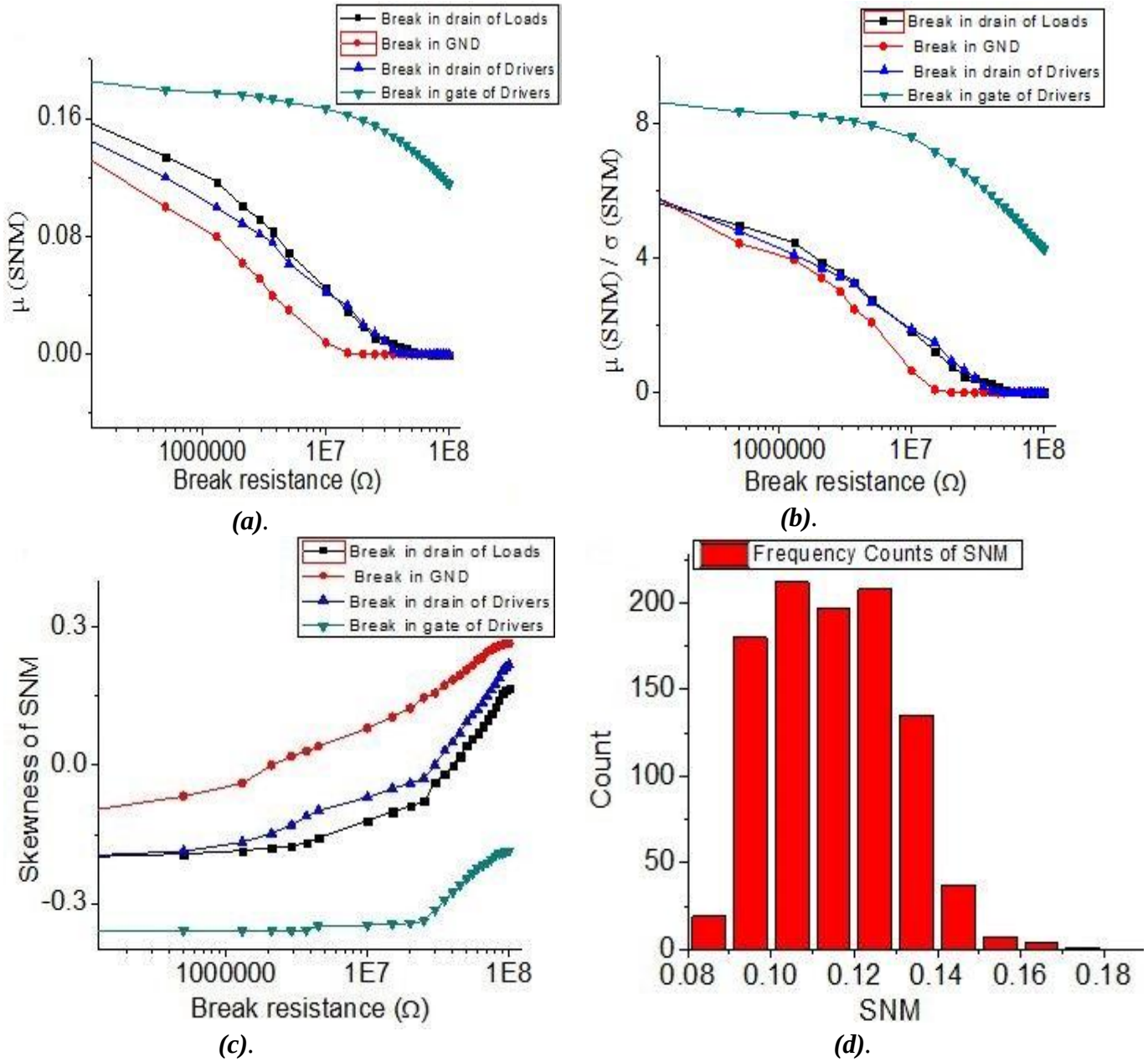

Fig. 4 Impact of break resistance on SNM: **(a)**:SNM mean deviation - **(b)**:normalized standard deviation of SNM - **(c)**:SNM skew - **(d)**:SNM distribution.

Figure (5-a) depicts the dependence of the SRAM cell SNM on variations in the W_{eff} and L_{eff} parameters of cell transistors. SNM changes break out when variations of the effective width and length reach 20%. In order to maintain a reasonable level of SNM as well as the effectiveness of future large-scale CMOS

SRAMs, cell ratios are to be increased from the typical ratio of r $=\frac{\frac{W}{L}_{Driver}}{\frac{W}{L}_{Access\ Tr}}=2$. The increase disturbs the balance of the scaling of the advantages of tens-of-nanometers technologies in relation to areas of SRAM cores [12].

Analysis of Figure (5-a) reveals that in weaker driver transistors SNM is reduced while in a transistor with weaker access SNM is enhanced. The reason is that deviation of the load transistor size only causes a slight destruction to SNM. The normalized standard deviation shown in Figure (5-b) indicates that changes of the load transistors size leads to a slight change in SNM, but changes in the size of access and driver transistors leave a considerable effect on SNM fluctuations. Figure (5-c) depicts SNM skew. As seen in this figure, variations of driver transistors W (70% deviation) and variations of load transistors L (10% deviation) have the highest and lowest effect on the SNM second moment deviation, respectively. Figure (5-d) shows distribution of SNM with a 15% deviation in the access transistors width. The highest SNM distribution occurs at 0.125.

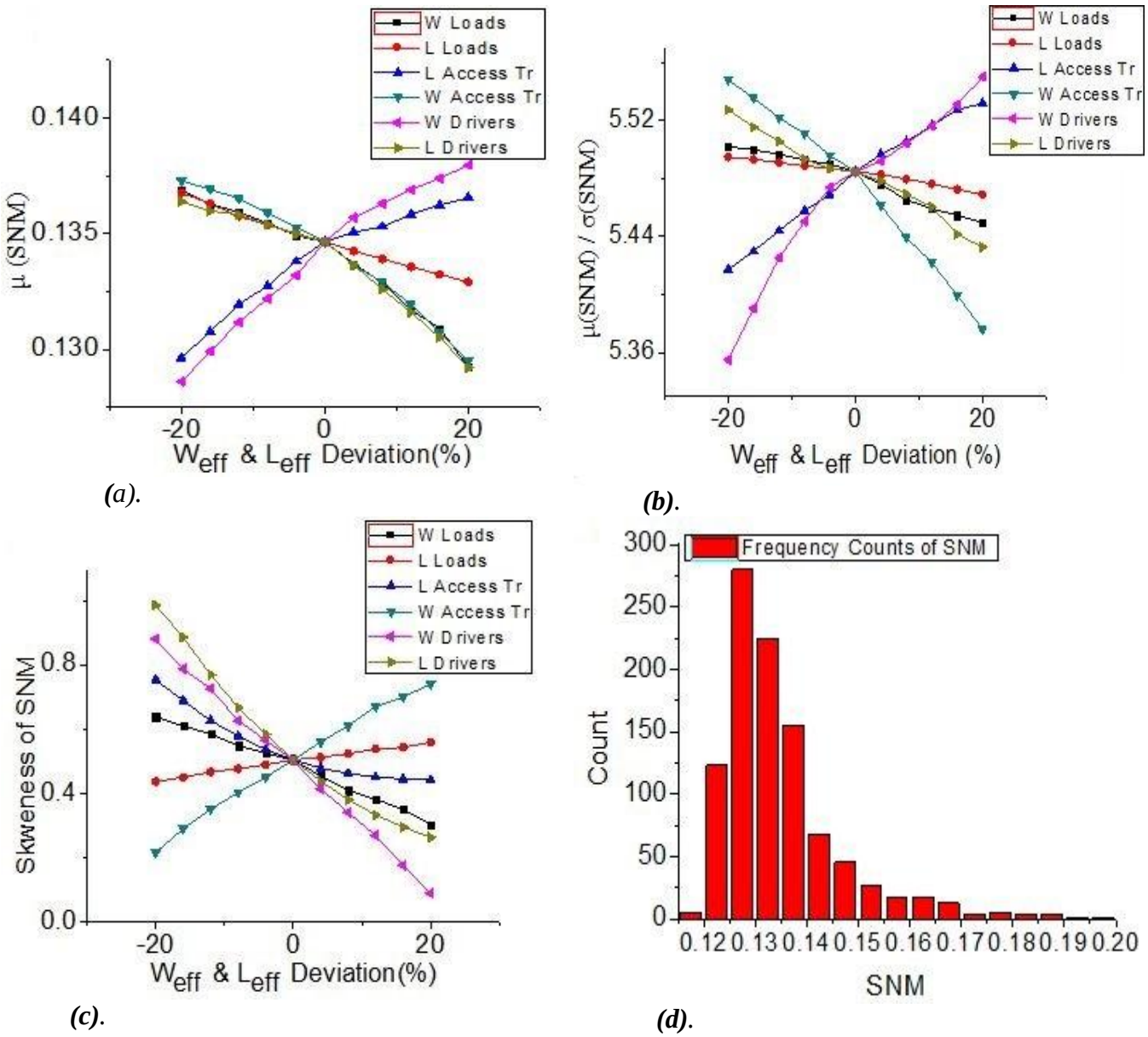

Fig. 5: Impact ofWeff and Leff deviations on SNM: **(a)**:SNM mean deviation - **(b)**:normalized standard deviation of SNM - (**c**):SNM skew - **(d)**:SNM distribution.

IV. ENVIRONMENTAL FLUCTUATIONS:

These fluctuations originally result from supply networks and surrounding noises [13]. Changes in working voltages (such as supply and word line voltages) are shown in Figure (6-a). As seen in this figure, SNM drastically influences the SRAM cell. SNM is highly dependent on VDD fluctuations as other voltages remain at their typical levels. These fluctuations lead to the strong shunting of access and load transistors, which in turn leave an adverse effect on the low mode of the cell. SNM is also enhanced with an increase in VDD, because the driver of the access transistors of the cell accessed for reading is weakened and the supply of mutually coupled inverters escalates.
The dependence of SNM on the variations word line voltage (VWL) shows that VWL < VTH in the access transistor does not influence SNM and the cell remains isolated from the read and write drivers. However, immediately with the change of VWL<VTH to VWL ≥ VTH in the access transistor, the cell is accessed for data read and write. Meanwhile, the access transistor starts shunting the load transistor

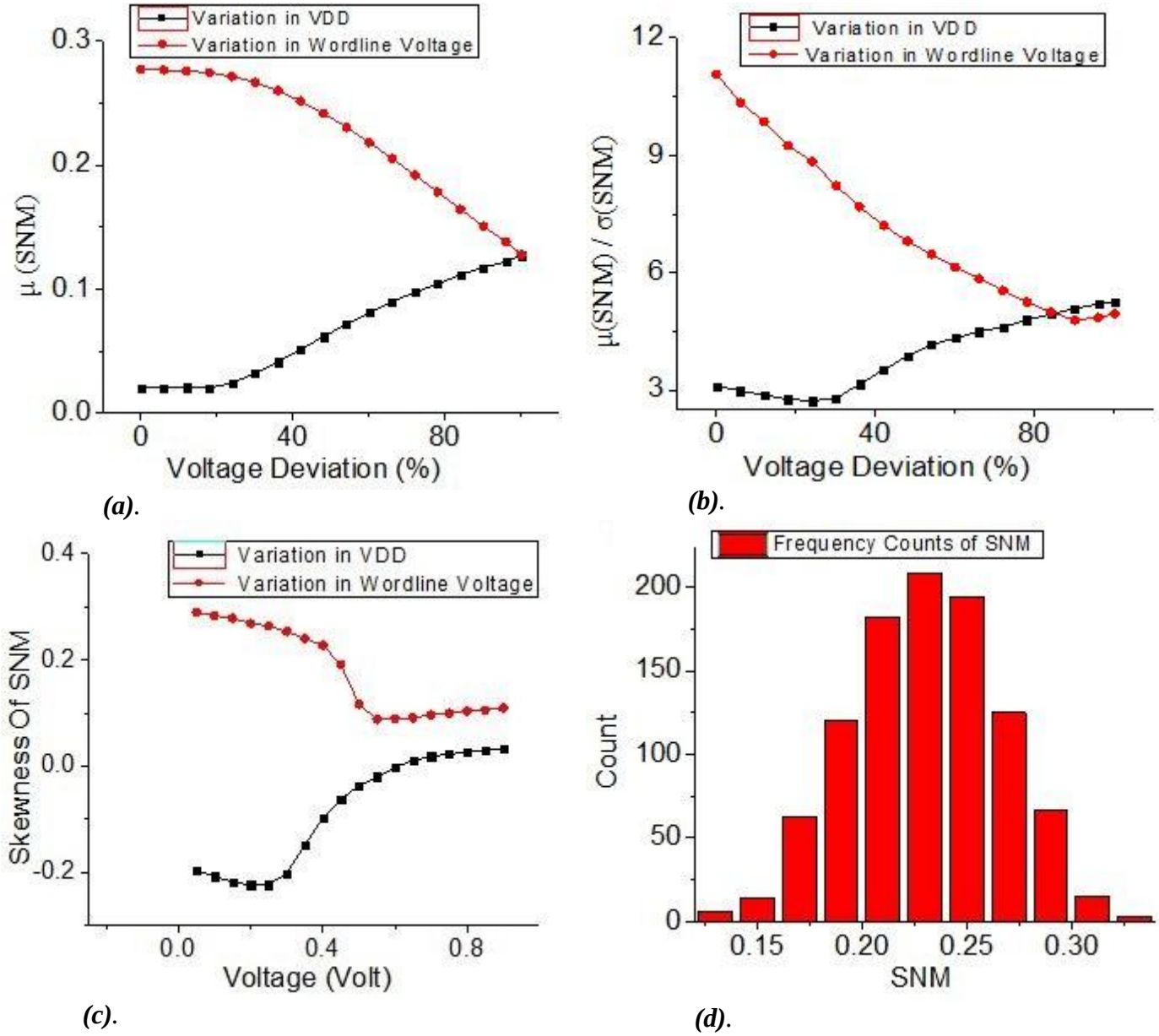

Fig. 6: Impact of voltage deviations on SNM: **(a)**:SNM mean deviation - **(b)**:normalized standard deviation of SNM - **(c)**:SNM skew - **(d)**:SNM distribution.

and elevates the node that stores the low mode. Consequently, a rotation occurs in the cell and the corresponding SNM is drastically destructed. Figure (6-b) shows the relevant normalized standard deviation. According to this figure, before VDD reaches a nominal value of 30%, variations of VDD have little contribution to SNM variations because the cell voltage has not reached the transistors threshold voltage yet. However, with a VDD between 30 and 60%, the nominal value of the effect of these changes on SNM mildly increases. Finally, when VDD reaches a value between 70% and 100%, the contribution of these changes to SNM variations declines since VDD approaches the nominal voltage. The effect of word line voltage variations on SNM changes declines drastically because the cell mode changes from storage to the read and write mode. When the voltage reaches a nominal value of 80%, the effect of these changes on SNM variations declines as the cell access completes. Figure (6-c) shows the relevant SNM skew. As seen in this figure, the slope of SNM changes resulting from fluctuations of word line and supply voltages is normalized in accordance with the slope of fluctuations of the normalized standard deviation. The normalization takes place based on the aforementioned reasons. Figure (6-d) shows SNM distribution in a VWL of 0.4v, which is the conduction threshold of access transistors. According to this figure, the highest SNM distribution occurs at 0.23 because the cell is in its storage mode and is not yet accessed for reading and writing.

V. CONCLUSION

SRAM cell stability is a determining factor in design, construction and test phases. Hence, broad analysis of SNM sensitivity is an important parameter for the identification of weak cells with inadequate noise margins. In this study, only one example for each of random, systematic and environmental fluctuations were studied. These fluctuations influence circuit function in the normal operation of the circuit. Moreover, building integrated circuits regardless of statistical fluctuations leads to a waste of time and money. Hence, study of the results of these changes can contribute to the development of more informed designs based on statistical fluctuations.

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