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3-D CHANNEL POTENTIAL MODEL FOR DOPED SYMMETRICAL ULTRA-THIN QUADRUPLE GATE-ALL-AROUND MOSFET

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ABSTRACT
The 3-D channel potential for Gate-all-around MOSFETs is based on two-dimensional solution of Poisson equation and perimeter weighted sum approach. The channel potential model of doped symmetrical GAA MOSFET is verified with simulation results for variation of channel length, silicon thickness and oxide thickness. The model of quadruple GAA MOSFET for channel potential is useful in analog and RF applications.
Keywords: Channel potential, subthreshold slope, quadruple gate MOSFET and short channel effect etc.

I. INTRODUCTION

The ultra-thin body SOI MOSFETs can be fabricated in different forms it may be a single or double gate (DG), quadruple gate MOSFET or Gate-all-around MOSFET[1]. One kind of Gate-all-around MOSFET is similar to the ultra-thin body SOI single-gate transistor, with the addition of bottom, front and back gate fully self-aligned to the top gate electrode in the opposite side of the buried oxide (BOX) [2]. On the basis of application of gate voltages, Gate-all-around MOSFETs may be grouped as symmetric, asymmetric MOSFETs[3]. The Gate-all-around MOSFET has higher scalability (i.e., better control of SCE) than the double-gate MOSFETs. The reason behind that the surrounding gate creates an electrical sheltering action of for electric fields creating from charges in the source and drain. An ideal Subthreshold slope of ~60mV/decade could be expected in a Gate-all-around MOSFET. Quadruple gate MOS devices have been presented with Undoped and doped channel for different applications. Undoped channel Quadruple MOSFET is suitable for digital applications. Doped channel Quadruple MOSFETs have found places in varieties of applications like base-band analog applications, memory applications [4-8] etc.

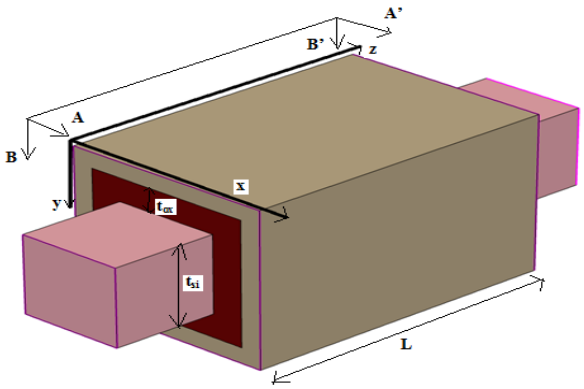

Figure 1: Schematic diagram of cubical channel Quadruple Gate-all-around MOSFET

A 3-D model of surface potential is modelled to get threshold voltage which is very important for the designing of VLSI circuits and systems targeting low-voltage, low-power and high-speed application [9-10]. We can also compare our results with the center potential of the CGAA MOSFET[11] which shows an extensive analysis carried out to find the impact of numerous device parameters.

II. DEVICE STRUCTURE AND DIMENSION

Figure 1 shows a cubical channel quadruple Gate-all-around MOSFET results when all surrounded gates have the same metal work function, same thickness of oxide and a single input voltage is applied

to all side of the gates. The device parameters and its values used for simulations are listed in Table 1. All the simulations are performed on Sentaurous device simulator [12]. The analytical model for channel potential is simulated with MATLAB and the results are compared with the results of 3-D device simulator.

Table 1: Device parameters and its values used in simulation

Parameters	Values
t_{ox}	*1nm-5nm*
t_{si}	*5nm-15nm*
L	*20nm-100nm*
W	*5nm-15nm*
N_d	$10^{20} cm^{-3}$
N_a	$10^{17} cm^{-3}$
μ_n	$1076 cm^2 / \ cm-s$
V_{gs}	$0-1\ V$
V_{ds}	$0.05-3\ V$

III. 3-D CHANNEL POTENTIAL MODEL

This paper deals with the 2-D modeling and simulation of the potential distribution and threshold voltage of ion-implemented Gate-all-around MOSFETs. Here the Gate-all-around MOSFET considered as cubical-channel Quadruple gate MOSFET for model derivation of 3-D channel potential. The doping profile of the channel is assumed to be constant. To simplify the mathematics the 3-D Quadruple gate device, device can be replaced with the 2-D equivalent symmetric double gate structure. For ignoring the coupling effects we take the channel length/channel width and channel length /channel thickness is larger than 2 which falls within the restriction required to obtain realistic and operational MOSFET. We use a method known as weighted parametric sum method in which a 3-D device Structure is divided into two 2-D symmetric structure. For individual 2-D structure we find the threshold voltage individually and by using the above method we can get the threshold Voltage of 3-D structure device.

III. 1 Channel Potential Derivation of the double gate MOSFET across cutline (AA')

The schematic structure of Undoped Quadruple gate MOSFET device used for the modeling and Sentaurus simulation is shown in Fig. (1.1). where, the notation L , t_{si} , t_h , t_{oxt} , t_{oxb} , t_{oxf} and t_{oxb} are the gate-length, channel thickness, channel width, top gate-oxide thickness, bottom gate-oxide thickness, front gate oxide thickness and back gate oxide thickness respectively. It should be noted that subscripts f and b are used for the front and back surface related parameters, respectively. The x-axes of the 2D structure are considered to be along the channel thickness and z-axes along the channel length which is shown in the Figure 2. For the distinction of the two gates, we use the nomenclatures of the gates as top-gate and bottom-gate of the device.

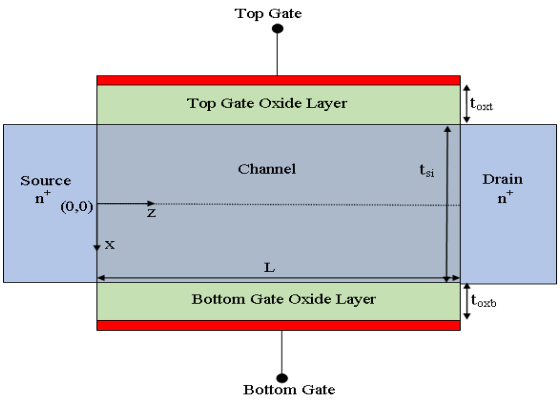

Figure 2: Schematic structure of the double gate MOSFET used in modeling and simulation

Let $\phi(x,z)$ be the potential distribution function in the channel, According to the Poisson equation, the channel potential is expressed by eq. (1)

$$\frac{\partial^2\varphi(x,z)}{\partial x^2}+\frac{\partial^2\varphi(x,z)}{\partial z^2}=\frac{qN_a}{\varepsilon_{si}} \quad (1)$$

The Poisson equation expressed by eq. (1) can be solved by using the following boundary conditions:

$$\phi\ x,z\ \big|_{x=0}=\phi_0\ \ x \quad (2)$$

$$\left.\frac{\partial\phi\ x,z}{\partial x}\right|_{x=0}=0 \quad (3)$$

$$\frac{\varepsilon_{ox}}{t_{ox}}\left(V_{gs}-V_{fb}-\phi\left(-\frac{t_{si}}{2},z\right)\right)=-\varepsilon_{si}\left.\frac{\partial\phi\ x,z}{\partial x}\right|_{x=-\frac{t_{si}}{2}} \quad (4)$$

$$\frac{\varepsilon_{ox}}{t_{ox}}\left(V_{gs}-V_{fb}-\phi\left(\frac{t_{si}}{2},z\right)\right)=\varepsilon_{si}\left.\frac{\partial\phi\ x,z}{\partial x}\right|_{x=\frac{t_{si}}{2}} \quad (5)$$

$$\phi\ x,0\ =V_{bi} \quad (6)$$

$$\phi\ x,L\ =V_{bi}+V_{ds} \quad (7)$$

$$\phi\ x,z\ \big|_{x=-\frac{t_{si}}{2}}=\phi_{fg}\ \ z \quad (8)$$

$$\phi\ x,z\ \big|_{x=\frac{t_{si}}{2}}=\phi_{bg}\ \ z \quad (9)$$

here, $\phi_0\ \ x$ is assumed as the potential function along the center of the channel, ε_{si} is the permittivity of silicon, ε_{ox} is the permittivity of the gate-oxide SiO_2. ϕ_{tg} , Is the top surface potential, $\phi_{bg}\ \ z$ is the bottom surface potential, $V_{bi}=\frac{kT}{q}\ln\frac{N_{S}N_a}{n_i^2}$ is the built-in potential, N_S is the doping concentration of heavily doped n^+ source (drain) region, V_{DS} is the drain-source voltage, and

$V_{fbf(fbb)}=\phi_{mf(mb)}-\left(\chi_s+\frac{E_g}{2}+\frac{kT}{q}\ln\left(\frac{N_{f(b)}}{n_i}\right)\right)$ is the flat-band voltage of the top (bottom) surface. where $\phi_{mf(mb)}$ is the top (bottom) metal work function, χ_s is electron affinity of silicon, E_g is the energy band gap of the silicon material, k is Boltzmann constant ,T is absolute temperature ,q is the charge on one electron and N_a is the channel doping concentration. According to Young *et al*. [58], the 2-D channel potential function can be approximated as parabolic in nature and expressed as:

$$\phi\ x,z\ =c_0\ \ z\ +c_1\ \ z\ \ x+c_2\ \ z\ \ x^2\quad . \quad (10)$$

Equation (2) and Equation (10), we get

$$c_0\ \ z\ =\phi_0\ \ z \quad (11)$$

Putting the value of Φ(x, z) from equation (10) to equation (4) and (5) and after solving we get the value of C_1 (z)

$$c_1\ \ z\ =\frac{\varepsilon_{ox}\ V_{fbt}-V_{fbb}}{t_{ox}\left(\varepsilon_{si}+\frac{\varepsilon_{ox}t_{si}}{2t_{ox}}\right)} \quad . \quad (12)$$

For Symmetrical DG MOSFETs,

$$c_1\ \ z\ =0\ . \quad (13)$$

Further, by using the above Equation's. (10)-(13) in Eq. (4), we get,

$$c_2\ \ z\ =\frac{V_{gs}-\frac{V_{fbt}-V_{fbb}}{2}-\phi_0\ \ z}{\left(\frac{1}{4}+\frac{t_{ox}\varepsilon_{si}}{\varepsilon_{ox}t_{si}}\right)t_{si}^2} \quad (14)$$

$$\lambda^2=\frac{1}{\left(\frac{1}{4}+\frac{t_{ox}\varepsilon_{si}}{\varepsilon_{ox}t_{si}}\right)t_{si}^2}\ . \quad (15)$$

where λ^2, is called the characteristic length associated with the Centre channel potential.

Now, substituting the value of $c_0\ \ z$, $c_1\ \ z$ and $c_2\ \ z$ in Eq. (10) then, the 2D potential function can be written as

$$\phi\ x,z\ =\phi_0\ \ z\ \ 1-\lambda^2x^2\ +\ V_{gs}-V_{fb}\ \ \lambda^2x^2 \quad (16)$$

Since Eq. (1) is usable over all the channel region. So, we can write the Poisson's equation at the SOI center in the form as:

$$\left.\frac{\partial^2\varphi(x,z)}{\partial x^2}\right|_{x=0}+\left.\frac{\partial^2\varphi(x,z)}{\partial z^2}\right|_{x=0}=\frac{qN_a}{\varepsilon_{si}} \quad (17)$$

Using Eq. (16) in Eq. (17), we obtain

$$\frac{\partial^2\varphi_0(z)}{\partial z^2}-2\lambda^2\phi_0\ \ z\ =\frac{qN_a}{\varepsilon_{si}}-2\ \ V_{gs}-V_{fb}\ \ \lambda^2 \quad (18)$$

Above equation is a second order differential equation and its solution having both complementary as well as particular integral part, which is given below

$$\phi_0\ \ z\ =Ae^{\sqrt{2}\lambda z}+Be^{-\sqrt{2}\lambda z}+\gamma \quad (19)$$

where

$$\gamma=\ V_{gs}-V_{fb}\ -\frac{qN_a}{2\lambda^2\varepsilon_{si}}\ . \quad (20)$$

By using Eq. (19) in Eq. (16), the 2D channel potential of the fully depleted doped symmetric DG MOSFETs can be expressed as

$$\phi\ x,z\ =\ Ae^{\sqrt{2}\lambda z}+Be^{-\sqrt{2}\lambda z}+\gamma\ \ 1-\lambda^2x^2\ +\ V_{gs}-V_{fb}\ \ \lambda^2x^2\ . \quad (21)$$

In the above equation A and B are arbitrary constant and it is obtained by using the above boundary conditions.

$$A=\frac{\left(V_{bi}-\ V_{gs}-V_{fb}\ +\frac{qN_a}{2\lambda^2\varepsilon_{si}}\right)1-e^{-\sqrt{2}\lambda L}\ +V_{ds}}{e^{\sqrt{2}\lambda L}-e^{-\sqrt{2}\lambda L}} \quad (22)$$

$$B=-\frac{\left(V_{bi}-\ V_{gs}-V_{fb}\ +\frac{qN_a}{2\lambda^2\varepsilon_{si}}\right)1-e^{\sqrt{2}\lambda L}\ +V_{ds}}{e^{\sqrt{2}\lambda L}-e^{-\sqrt{2}\lambda L}} \quad (23)$$

In the above equation if we have put the value of x =t_{si}/2 then we get the surface potential of the channel as:

$$\phi_s\ \ z\ =\phi\left(\frac{t_{si}}{2},z\right)=\phi_0\ \ z\ \left(1-\lambda^2\frac{t_{si}^2}{4}\right)+\ V_{gs}-V_{fb}\ \ \lambda^2\frac{t_{si}^2}{4}. \quad (24)$$

III. 2 Channel Potential Derivation of the double gate MOSFET across cutline (BB')

As we have find the threshold voltage of the symmetrical double gate MOSFETs using the concept of center potential and surface potential of the schematic diagram shown in Figure1. In the same way we can find the threshold voltage of the structure shown in Figure3.

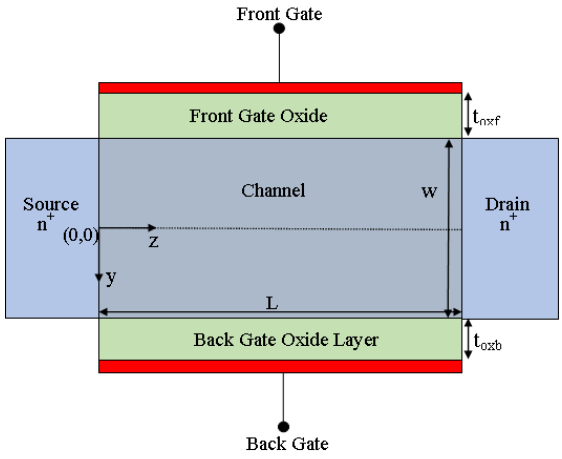

Figure 3: Schematic structure of the double gate MOSFET used for modeling and simulation

The y- axes of the 2D structure are considered to be along the channel width and z-axes along the channel length which is shown in the Figure 3. For the distinction of the two gates, we use the nomenclatures of the gates as to front-gate and back-gate of the device. Let $\phi(y,z)$ be the potential distribution function in the channel, According to the Poisson equation, the channel potential is expressed by eq. (25).

$$\frac{\partial^2\varphi(y,z)}{\partial y^2}+\frac{\partial^2\varphi(y,z)}{\partial z^2}=\frac{qN_a}{\varepsilon_{si}}\ . \quad (25)$$

The Poisson equation expressed can be solved by using the following boundary conditions:

$$\phi\ \ y,z\ \big|_{y=0} = \phi_{01}\ \ z \qquad (26)$$

$$\left.\frac{\partial \phi\ \ y,z}{\partial y}\right|_{y=0} = 0 \qquad . \qquad (27)$$

$$\frac{\varepsilon_{ox}}{t_{ox}}\left(V_{gs} - V_{fb} - \phi\left(-\frac{w}{2},z\right)\right) = -\varepsilon_{si}\left.\frac{\partial \phi\ \ y,z}{\partial y}\right|_{y=-\frac{w}{2}} \qquad (28)$$

$$\frac{\varepsilon_{ox}}{t_{ox}}\left(V_{gs} - V_{fb} - \phi\left(\frac{w}{2},z\right)\right) = \varepsilon_{si}\left.\frac{\partial \phi\ \ y,z}{\partial y}\right|_{y=\frac{w}{2}} \qquad (29)$$

$$\phi\ \ y,0\ = V_{bi} \quad (2.51)$$

$$\phi\ \ y,L\ = V_{bi} + V_{ds} \quad (2.52)\ .$$

According to Young *et al*., the 2-D channel potential function can be approximated as parabolic in nature;

$$\phi\ \ y,z\ = c_3\ \ z\ + c_4\ \ z\ \ y + c_5\ \ z\ \ y^2 \qquad (30)$$

After solving the above equation from eq. 30, we get

$$\phi\ \ y,z\ = \phi_{01}\ \ z\ \ \ 1-\lambda_1^{\,2}y^2\ \ +\ V_{gs} - V_{fb}\ \ \lambda_1^{\,2}y^2 \qquad (31)$$

$$\lambda_1^{\,2} = \frac{1}{\left(\frac{1}{4} + \frac{t_{ox}\varepsilon_{si}}{\varepsilon_{ox}w}\right)w^2} \qquad (32)$$

where $\lambda_1^{\,2}$, is called the characteristic length associated with the Centre channel potential.

So, we get the surface potential as given below:

$$\phi\ \ y,z\ = \ A_1 e^{\sqrt{2}\lambda_1 z} + B_1 e^{-\sqrt{2}\lambda_1 z} + \gamma_1\ \ \ 1-\lambda_1^{\,2}y^2\ \ +\ V_{gs} - V_{fb}\ \ \lambda_1^{\,2}y^2 . \qquad (33)$$

In the above equation A_1 and B_1 are arbitrary constant and it is obtained by using the above boundary conditions.

$$A_1 = \frac{\left(V_{bi} - \ V_{gs} - V_{fb}\ + \frac{qN_a}{2\lambda_1^{\,2}\varepsilon_{si}}\right)1-e^{-\sqrt{2}\lambda_1 L}\ \ + V_{ds}}{e^{\sqrt{2}\lambda_1 L} - e^{-\sqrt{2}\lambda_1 L}} \qquad (34)$$

$$B_1 = -\frac{\left(V_{bi} - \ V_{gs} - V_{fb}\ + \frac{qN_a}{2\lambda_1^{\,2}\varepsilon_{si}}\right)1-e^{\sqrt{2}\lambda_1 L}\ \ + V_{ds}}{e^{\sqrt{2}\lambda_1 L} - e^{-\sqrt{2}\lambda_1 L}} \qquad (35)$$

In the above equation if we have put the value of y =w/2 then we get the surface potential of the channel as:

$$\phi_s\ \ z\ = \phi\left(\frac{w}{2},z\right) = \phi_{01}\ \ z\ \left(1-\lambda_1^{\,2}\frac{w^2}{4}\right) + \ V_{gs} - V_{fb}\ \ \lambda_1^{\,2}\frac{w^2}{4}. \qquad (36)$$

III. 3 Generalized Channel 3-D Potential Model

Due to fact that the leakiest path will be in the middle of the channel width as well as middle of the channel thickness for the quadruple gate device, the $3-D$ center potential of the device can be equivalently decomposed into two $2\text{-}D$ central potential for both symmetrical double gate device. By using the perimeter weighted sum method the analytical potential of the quadruple gate is expressed as

$$\phi\ \ x,y,z\ = \phi\ \ x,z\ \times\alpha + \phi\ \ y,z\ \times\ 1-\alpha \qquad (37)$$

where, $\alpha = \frac{w}{w + t_{si}}$, where $\phi\ \ x,y,z$, is the analytical potential for quadruple gate device and α is the ratio of symmetrical double gate MOSFETs device to the entire quadruple gate MOSFETs.

IV. SIMULATION AND RESULT

Figure 4 shows the variation of center potential with the channel length position. We get a good agreement between analytical model results with the numerical simulator results.

From Figure 4 it can be noted that source channel barrier height at channel center is lower than that of the surface and hence the threshold voltage should be calculated by using the center potential minima. Figure 5 shows the variation of surface potential with the channel length position for different channel thickness and we get a good agreement between analytical model results with the numerical simulator results. From Figure5, it is observed that the source to channel barrier increases with decreasing the channel thickness .when the channel thickness is decreases the control of gate on the channel is increases because the electric field in vertical direction is increased and hence potential of channel is also increases. We get a good agreement between analytical model results with the numerical simulator results.

Figure 6 shows the variation of surface potential with the channel length position for different oxide thickness. We get a good agreement between analytical model results with the numerical simulator results. From Figure 6, it is observed that the source to channel barrier increases when the thickness of the oxide layer is decreases.

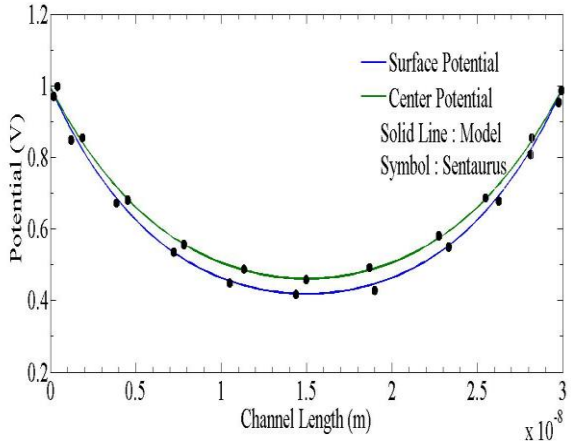

Figure 4: Variation of channel potential with the channel length. Parameter used is $t_{si} = 10nm$, $w = 10nm$, $V_{DS} = 0V$ and $V_{GS} = 0V$.

When the oxide thickness is decreases the control of gate on the channel is increases because the electric field in vertical direction is increased and hence potential of channel is also increases. But the carrier in channel may have got the enough energy and it penetrate the oxide layer and these trap charge may be degrade the threshold voltage. So we cannot decrease the oxide thickness too much. We get a good agreement between analytical model results with the numerical simulator results.

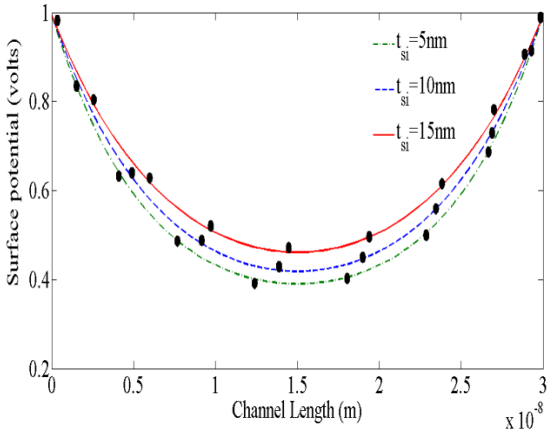

Figure 5: Variation of surface potential with the channel length. Parameter used are $t_{ox} = 10nm$, $w = 10nm$, $V_{DS} = 0V$ and $V_{GS} = 0V$.

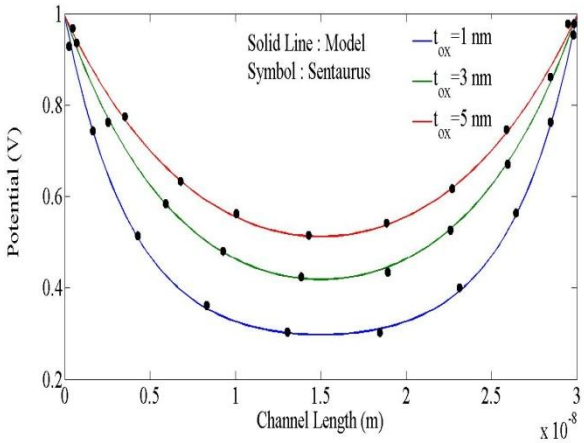

Figure 6: Variation of surface potential with the channel length. Parameter used are $t_{si} = 10nm$, $w = 10nm$, $V_{DS} = 0V$ and $V_{GS} = 0V$.

V. CONCLUSION

The paper models the 3-D channel potential for GAA MOSFET. The 3-D channel potential is plotted with the variation of channel length (L), channel thickness (t_{si}) and oxide thickness (t_{ox}). A good agreement is obtained

between analytical model results with the numerical simulator results. The model is useful in study of Quantum Mechanical Effects on short channel Quadruple gate GAA MOSFET.

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