Journal of Electron Devices, Vol. 21, 2015, pp. 1881-1887

© JED [ISSN: 1682 -3427]

Journal of Electron Devices
www.jeldev.org

TCAD SIMULATION ANALYSIS AND COMPARISON BETWEEN TRIPLE GATE RECTANGULAR AND TRAPEZOIDAL FinFET

Gaurav Musalgaonkar, Arun Kumar Chatterjee.
Department of Electronics and Communication Engineering Thapar University, Patiala, Punjab-147001, India
gaurav.musalgaonkar7@gmail.com

Received 12-05-2015, Revised 17-05-2015, Online 19-05-2015

ABSTRACT

FinFET are the modern day device structure. Presently we have rectangular shaped FinFETs as a leader in the electronic industry. Few years back, INTEL has proposed that as a result of some fabrication-process limitations there is redundant slope of the fabricated transistors with the original tri-gate FinFET, because of this some FinFETs have inclined surfaces, which results in trapezoidal cross sections instead of rectangular sections. This study analyzes the influence of the FinFET sidewall inclination angle on some relevant parameters such as threshold voltage, trans-conductance, drain current. Then we perform a comparative study between the rectangular shaped FinFET and trapezoidal shaped FinFET. Finaly, we analyze the corner effects in the rectangular FinFETs and trapezoidal FinFETs. All the simulations are done through a 3D numeric simulator COGENDA GENIUS TCAD.

Keywords: DGFinFETs, Re-TGFinFET, Tz-TGFinFET, Corner Effect.

I INTRODUCTION

According to Moore's law [1], which says that number of transistors per chip increases for every 18 months, in agreement with it the scaling of the devices has been done to accommodate more number of transistors on the chip. As the devices are scaled down, planar transistors has brought several detrimental effects such as gate oxide tunneling, increment of leakage currents and enhancement of Short-Channel-Effects (SCE)[2]. The effect of drain electric field over the channel increases which ultimately giving rise to unwanted short channel effects degrading the characteristics of the device [3]. Due to these short channel effects the existing devices cannot be scaled down further. Recently, the continuous downscaling of complementary metal-oxide semiconductor CMOS device for achieving the necessary performance for the growth of the microelectronics industry is required. There are some solutions which have extended the further possibility of scaling devices beyond the fundamental physical limits of bulk MOS transistors[4]. The silicon-on-insulator SOI technology has been an extremely attractive key in terms of performance and scalability. From the previous experience of having the best control of inversion charge by back and front gates of fully depleted SOI devices, the idea of multiple-gate devices has been developed[5]. In the recent years tri-gate (TG) field-effect transistors (FETs) such as fin-shaped FETs (FinFETs) have been proposed as the best option for sub-100 nm regime of MOSFETs due to their better gate control(from three sides) for suppressing the short channel effects and advantages to standard bulk planar CMOS processing [6].

In the Triple Gate FinFET the phenomenon caused by the presence of the top gate and side gates is the corner effect [7] which occurs due to the overlapping of two gate planes(vertical and horizontal plane) near the device corners. To reduce these corner effects Trapezoidal FinFETs can be used. Here, in this work we perform comparative study to analyze the electrical properties of rectangular FinFET as shown in the Figure 1 and trapezoidal FinFET as shown in the Figure 2. Then we analyzed that what will be the effect of inclined walls of a trapezoidal FinFET on electric field and charge distribution at the corners. We further investigated that what will be the effect of inclined walls on mobility when the angle of inclination changes by certain angles. Finally we analyzed the effect of inclined fins on I-V characteristics of trapezoidal FinFETs and compare all the results with rectangular FinFETs.

This paper is organized as follows: In section II, a description of the device design and its simulation setup along with what will be the design impact is given. However section III addresses the obtained results. Finally, summarizes the important findings of this study in Section IV

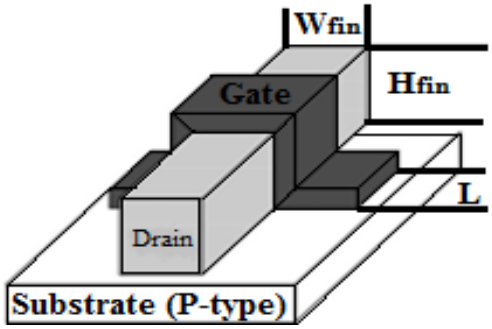

Figure 1. Schematic view of triple gate Rectangular shaped FinFET

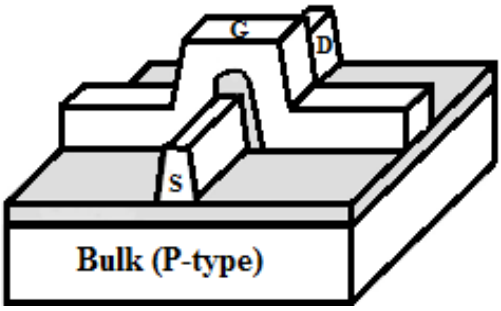

Figure 2. Schematic view of triple-gate trapezoidal shaped FinFET

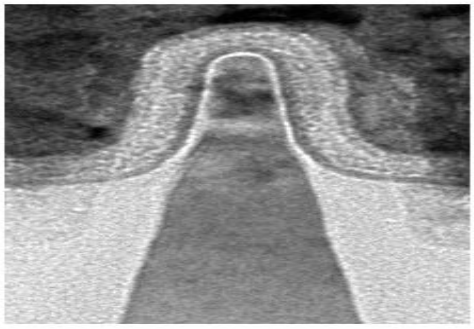

Figure 3. Microscopic view of FinFET shows that side walls are not perfectly straight but inclined at certain angle from the top gate.

The simulated device has the following parameters shown in the table 1 [8].

Table 1 Parameters used for simulations

Parameters	Value used
Top silicon width W_{FinTop}	16 nm
Silicon height H_{Fin}	30 nm
Gate-oxide thickness	1 nm
Gate work function	4.5 eV
channel length	50 nm
Source/drain doping	1e20 cm^{-3}
Channel doping	10^{16}, 10^{17}, 10^{18} cm^{-3}

II DEVICE STRUCTURE, OPERATION, AND SIMULATION SETUP

Several independent studies conducted over the past decade, which have suggested various device architectures that offer better solution to short channel effects and allow transistor to shrink bellow sub 100 nm regime. There are several compact models which are developed for the rectangular double and triple gate FinFET [9]-[12]. In the recent study by the Intel [13], it is shown that tri-gate transistors are in fact trapezoidal and almost triangular in cross-section as shown in Figure 3. It was not clear by that time whether the non-vertical sides to the fins were a non-critical manufacturing aftermath or deliberately engineered by Intel, What were its impact on electron mobility or other device parameters. There was a lot of speculation about the possible advantages and disadvantages of the trapezoidal shaped FinFET such as corner effect, threshold voltage, mobility and so on. In this paper, we performed a simulation analysis to see the impact of the non vertical sidewalls by varying the angle of inclination as shown in Figure 4 on the performance of the FinFET using 3-D TCAD simulator COGENDA GENIUS. Table 1 which follows the device dimensions according to ITRS 2013 roadmap and Figure 5 shows the device nomenclature. For the simulation we have drift-diffusion, mobility, density-gradient quantum correction models being turned on. Enhanced Lombardi mobility model was activated which accounts for mobility degradation at si-sio2 interface. To find accurate threshold voltage maximum transconductance method is used.

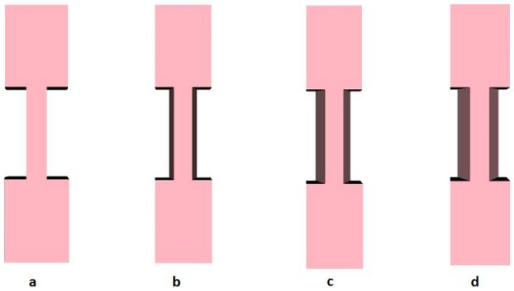

Figure 4. FinFET's structures. (a) rectangular shaped, (b) trapezoidal shaped withangle θ_1 (c) trapezoidal shaped with angle θ_2 (d) trapezoidal shaped with angle θ_3 where ($\theta_1 < \theta_2 < \theta_3$) and is the angle between top gate and side walls of the FinFET

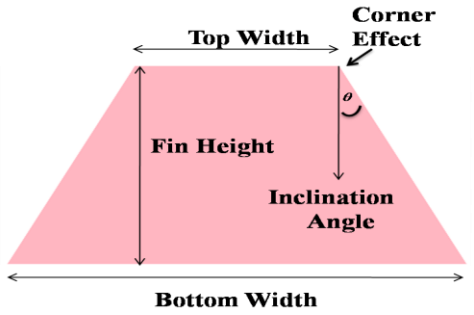

Figure 5. Cross sectional view of Trapezoidal FinFET

III RESULT AND DISCUSSION

III.1 Threshold voltage analysis

The threshold voltage value which is the most important electrical parameter in modelling of MOSFETs can be extracted from either measured drain current or capacitance characteristics of a MOSFET. There are some of the most common methods which are available to measure the threshold voltage [14]. Here in this paper we have used maximum transconductance method which suggest that the value of gate voltage at which first derivative of transconductance i.e. $dg_m/dv_g=d^2I_d/dV_g^2$ is maximum is the threshold voltage of the device. Plot for the threshold voltage detection using the maximum transconductance is shown in Figure 6.

The threshold voltage equation for rectangular trigate FinFET is given by equation 1[15].

$$V_t = V_{fb} - \frac{1}{(1-(A_1-A_2))} \times \begin{pmatrix} A_1(V_{bi}+V_d)+A_2V_{bi} \\ -V_{th}\ln\left[\frac{Q_{th}N_a}{n^2{}_iW_{fin}}\right] \end{pmatrix} \quad ..(1)$$

where $V_{fb} = \phi_{ms} - V_t \ln\left(\frac{N_a}{n_i}\right)$ is the flat band voltage, N_a is doping concentration of silicon channel, V_{bi} is built in potential across the source and drain junctions given as

$$V_{bi} = \frac{kt}{q}\ln\left(\frac{N_a N_d}{n^2{}_i}\right) \qquad (2)$$

and Q_{th} is the minimum carrier charge density which is required to turn it on in the strong inversion conditions. The analytic expression for Q_{th} is presented in Appendix. It is a function of the device natural length. We can extend equation (1) of the threshold voltage for the trapezoidal FinFET by doing appropriate changes to A_1 and A_2 presented in Appendix.

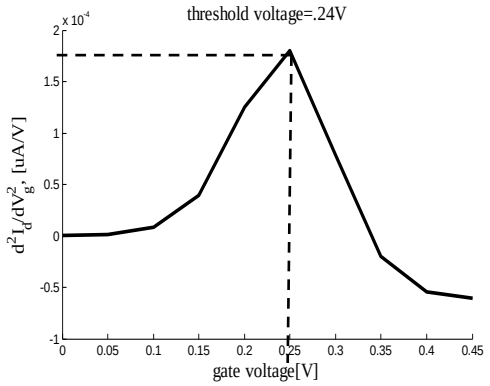

Figure 6.a Maximum transconductance method implemented on the plot of d^2I_d/dV^2_g versus V_g. . Gate-voltage at which d^2I_d/dV^2_g exhibits a maximum value is equal to threshold voltage of device. Here L=50nm, H=30nm, Wtop=16nm, Wbot=16nm, V_d=0.05V, Na=$10^{17}cm^{-3}$ (Rectangular FinFET)

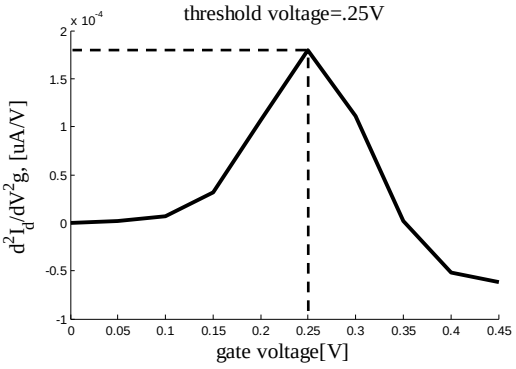

Figure 6.b Maximum transconductance method implemented on the plot of d^2I_d/dV^2_g versus V_g. Gate-voltage at which d^2I_d/dV^2_g exhibits a maximum value is equal to threshold voltage of device. Here L=50nm, H=30nm, Wtop=16nm, Wbot=30nm, V_d=0.05V, Na=$10^{17}cm^{-3}$ (Trapezoidal FinFET)

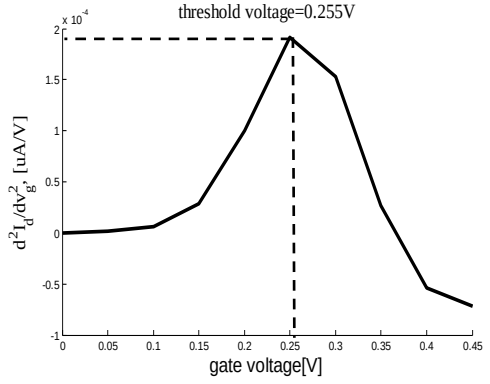

Figure 6.c Maximum transconductance method implemented on the plot of d^2I_d/dV^2_g versus V_g. Gate-voltage at which d^2I_d/dV^2_g exhibits a maximum value is equal to threshold voltage of device. Here L=50nm, H=30nm, Wtop=16nm, Wbot=30nm, V_d=0.05V, Na=$10^{17}cm^{-3}$, (Trapezoidal FinFET)

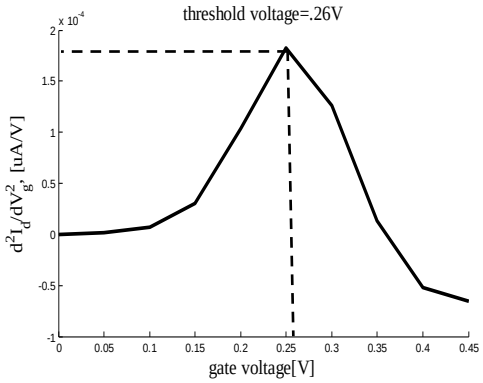

Figure 6.d Maximum transconductance method implemented on the plot of d^2I_d/dV^2_g versus V_g. Gate-voltage at which d^2I_d/dV^2_g exhibits a maximum value is equal to threshold voltage of device. Here L=50nm, H=30nm, Wtop=16nm, Wbot=35nm, Vd=0.05V, Na=10^{17}cm^{-3}**,** (Trapezoidal FinFET)

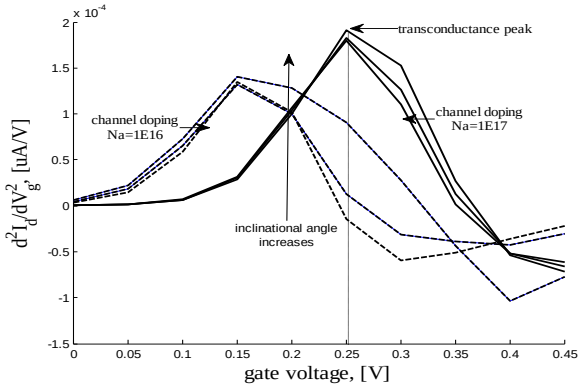

Figure 7. Maximum transconductance method implemented on the plot of d^2I_d/dV^2_g versus V_g for two different doping levels. Here L=50nm,H=30nm, Wtop=16nm, Wbot=24nm to 35nm,N_a=10^{16}cm^{-3} to 10^{17}cm^{-3}, Vd=.05V (Trapezoidal FinFET).

Table. 2 Comparison between threshold voltage for different angles of inclination and for two doing levels.

Angle of inclination	Threshold voltage Na=10^{16}cm^{-3}	Threshold voltage Na=10^{17}cm^{-3}
0^0	.15V	.24V
9.46^0	.16V	.25V
13.40^0	.165V	.255V
18^0	.17V	.26V

It can be observed from the figure 6 and figure 7 that the threshold voltage depends on the inclination angle and on the channel doping level. This is because of the dependence on the composition of charges present in the silicon-film. In the recent years, structures used for the rectangular FinFET typically, the (1 1 0) side walls crystallographic orientation and the variation on the sidewall angles leads to a change in the surface crystallographic orientation. Which ultimately leads to change in the carrier mobility and threshold voltage. It is also found that as we change the shape from rectangular to trapezoidal the position of minium potential is also shifted which is a function of the width of the FinFET. Figure 8 and Figure 9 show the electron density across the channel of the FinFET. The electron concentration data is taken from the cross section far from the drain at half of channel length and it can be seen -(Table 2) that for smaller inclination angle electron concentration value is more as compare to higher inclination angle which ultimately leads to more corner effect in smaller inclination angle FinFET than higher inclination angle FinFET. There are two types of charges present in the silicon film, depletion charge and inversion charge. For both doping levels the electron concentration is above 10^{16} cm^{-3}.

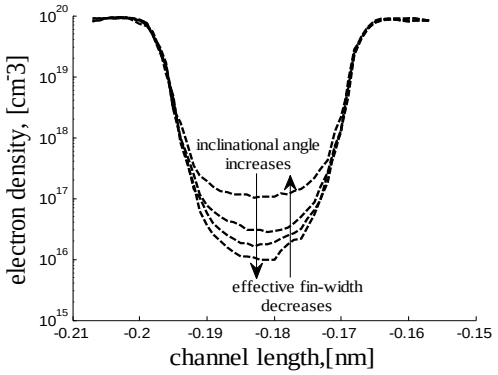

Figure 8. Electron density as a function of angle of inclination. Channel doping=10^{-18}cm^{-3}, V_d=0.05V, L=50nm, H=30nm, W_{top}=16nm, W_{bot}=24nm to 35nm (Trapezoidal FinFET).

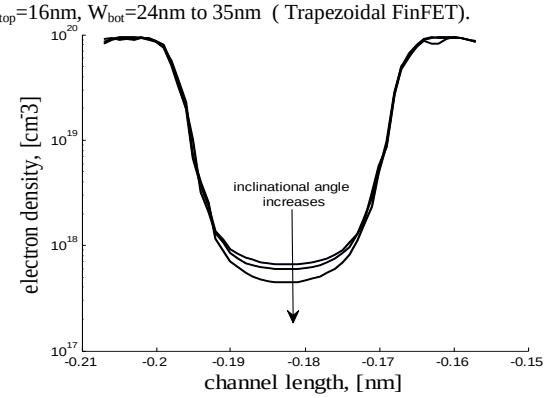

Figure 9 Electron density as a function of angle of inclination. Channel doping=10^{16}cm^{-3}, V_d=0.05V, L=50nm, H=30nm, W_{top}=16nm, W_{bot}=24nm to 35nm (Trapezoidal FinFET).

From the Figure 8 and Figure 9 we can easily understand that in silicon film charges mostly composed of depletion charge for the device with a doping level of 10^{17} cm^{-3} and for the device with doping level 10^{16} cm^{-3}, minority carriers are responsible for the charge composition as the depletion charge density is now limited 10^{16} cm^{-3}. In both the cases during volume inversion there is

a difference in the charge distribution profile. This is because as we increases the channel doping concentration the carrier concentration increase near the corners and decreases in the center of the device. The main consequence of this phenomena is threshold voltage variation and it depends upon the variation in fin-width.

Table.3 Comparison between electron mobility for different angle of inclination and with two doing levels.

Angle of inclination	Channel doping=$10^{18}cm^{-3}$, Mobility $Cm^2/V/S$	Channel doping=$10^{16}cm^{-3}$, Mobility $Cm^2/V/S$
0^0	149.68	688.71
9.46^0	142	620.72
13.40^0	140	585.64
18^0	136	579.52

Table 3 shows the mobility values of electrons through the surface for different structures of trapezoidal FinFET. It can be seen that the mobility decrease as the angle of inclination increases. As the geometry of the device changed from rectangular to trapezoidal different crystal planes are exposed which have a huge impact on mobility.

III.2 Corner Effect Analysis

The corner Effect can be defined as the leakage at the interface of top and side gate. It is caused by the increase of inversion charge carriers in the proximity of the corners, which ultimately leads to leakage current. In order to evaluate the sidewall inclination angle influence on the corners, net charge concentration and electric field was chosen as an electrostatic parameter. In this work we analysed the effect of both on device structure. Figure 10 shows the net charge distribution throughout the structure. It is clear from the Figure 10 the effect of charge carrier in the corners is less as we increase the inclination angle. Figure 11 shows the effect of net electric field across the corners. Effective electric field is lesser at the corners as the angle of inclination increases. This indicates that influence of corner effect is less in trapezoidal FinFET as compare to rectangular FinFET. Also the corner effect becomes less significant as the channel doping decreases. This is because in that case, carrier can be more uniformly distributed across the top and side gate plane interface.

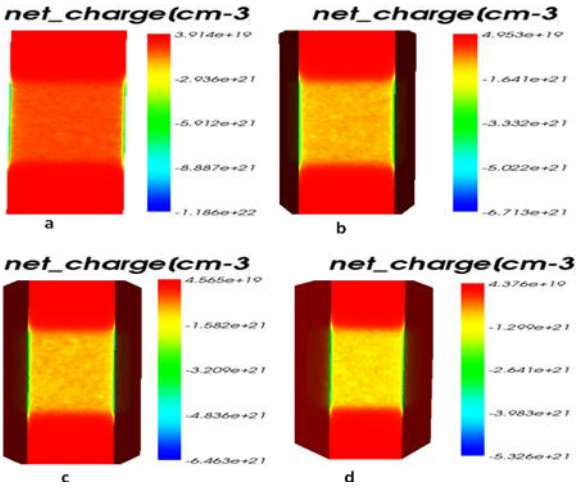

Figure 10 Simulation result of the Net charge present at the corner of the FinFET, (a) rectangular FinFET, from (b) to (d) trapezoidal FinFET with increasing angle of inclination. Channel doping $Na=10^{18}$ cm^{-3}, H=30nm, L=50nm and V_d=0.05V.

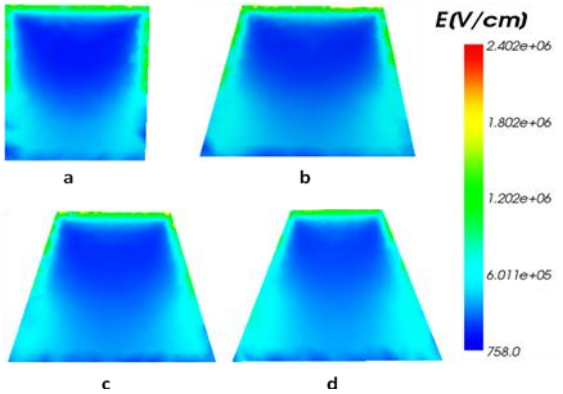

Figure 11 Simulation result of the distributed electric field across the corners, (a) rectangular FinFET, from (b) to (d) trapezoidal FinFET with increasing angle of inclination**.** Channel doping $Na=10^{18}$ cm^{-3}, H=30nm, L=50nm and V_d=0.05V.

III.3 Effect Of Inclined Fins On Drain Current

The simulation result for transfer characteristics and output characteristics is shown in Figure 12.a, 12.b and Figure 12.c. It is clear from the Figures that for smaller inclination angle drain current is more in the rectangular FinFET as compared to trapezoidal FinFET. So we can conclude that rectangular FinFET have better short channel effects but corner effect is lesser in trapezoidal FinFET as the angle of inclination increases. These results show that trapezoidal FinFET can improve the electrical characteristics of multigate FinFETs. With increasing the angle of inclination I_{on}/I_{off}, subthreshold slope and DIBL improved significantly because the thickness at the bottom increases and reduces at the top which ultimately provide better gate control over the channel.

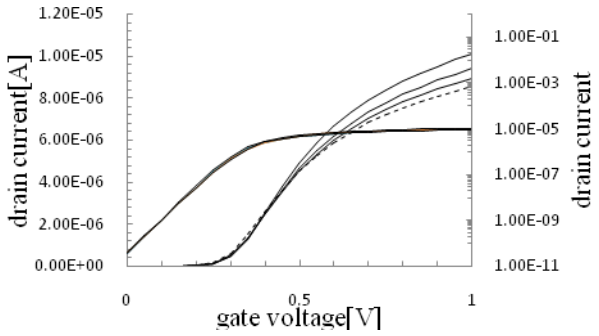

Figure 12.a Simulated result for drain current versus gate voltage (with increasing angle of inclination). Channel doping Na=10^{18} cm^{-3}, H=30nm, L=50nm and Vd=0.05V (linear region). Top curve for trapezoidal FinFET (continuous line) and bottom is for rectangular FinFET (dashed line) with higher angle of inclination.

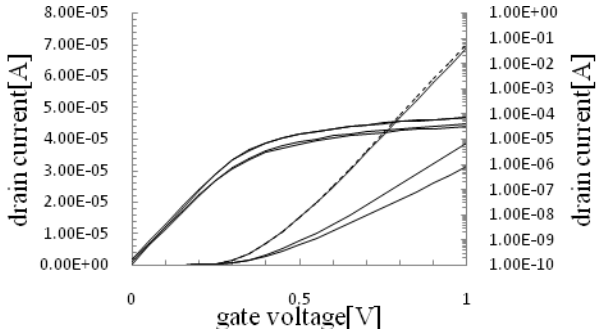

Figure 12.b Simulated result for drain current versus gate voltage, (with decreasing angle of inclination). Channel doping Na=10^{18} cm^{-3}, H=30nm,L=50nm and Vd=1V. (saturation region). Top curve for rectangular FinFET (dashed line) and bottom is for trapezoidal FinFET (continuous line) with higher angle of inclination.

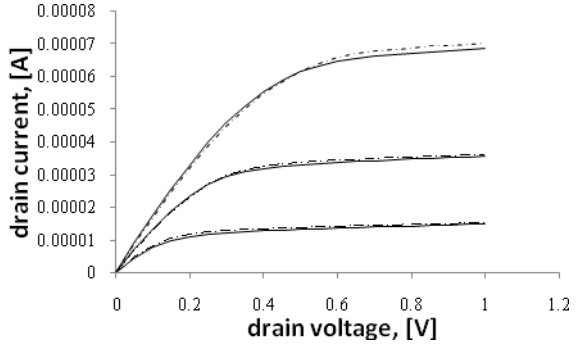

Figure 12.c Simulated result for drain current versus drain voltage. Channel doping Na=10^{18} cm^{-3}, H=30nm, L=50nm and V_d=1V. Dashed lines for rectangular FinFET. solid line for trapezoidal FinFET $(\theta = 9.36)$

IV. CONCLUSION

In this paper, simulations of rectangular FinFET and trapezoidal FinFET are carried out. We analyzed the effect of inclined fins on threshold voltage, electron mobility, electron charge density, electric field density. From the knowledge of threshold voltage for rectangular FinFET we can suggest that in trapezoidal FinFET, as the position of minimum potential changes so we can conclude that threshold voltage is a function of top and bottom fin width and is independent of its cross sectional shape. Also threshold voltage increases for the increase in inclination angle for lower doping and decreases for higher doping levels. Also we can conclude that Corner effect become lesser in trapezoidal FinFETs as the inclination angle increases. Short channel effect is lesser in rectangular FinFET as compare to trapezoidal FinFET at smaller drain voltages. Over all in trapezoidal FinFETs electrical characteristics are improved and it can be a good alternative for rectangular FinFETs

APPENDIX

Parameters A_1 and A_2 of trapezoidal FinFET for threshold voltage detection can be expressed as a function of device natural length given by

$$A_1 = \frac{2H_{fin}A_{1,sym} + W_{fin}A_{1,asym}}{W_{fin} + 2H_{fin}} \quad (1)$$

$$A_2 = \frac{2H_{fin}A_{2,sym} + W_{fin}A_{2,asym}}{W_{fin} + 2H_{fin}} \quad (2)$$

$$A_{1,sym} = \frac{e^{(L+Z_{mim})/\beta_{sym}} - e^{(L-Z_{mim})/\beta_{sym}}}{e^{2L/\beta_{sym}} - 1} \quad (3)$$

$$A_{2sym} = \frac{e^{(2L-Z_{mim})/\beta_{sym}} - e^{Z_{mim}/\beta_{sym}}}{e^{2L/\beta_{sym}} - 1} \quad (4)$$

$$A_{1,asym} = \frac{e^{(L+Z_{mim})/\beta_{asym}} - e^{(L-Z_{mim})/\beta_{asym}}}{e^{2L/\beta_{asym}} - 1} \quad (5)$$

$$A_{2,asym} = \frac{e^{(2L-Z_{mim})/\beta_{asym}} - e^{Z_{mim}/\beta_{asym}}}{e^{2L/\beta_{asym}} - 1} \quad (6)$$

$$Z_{min} = \frac{L}{2} - \frac{\beta_{eff}}{2} \times \ln\left(\frac{\left(V_{bi} + V_{fb} - V'_g\right)\left(e^{1/\beta_{eff}} - 1\right) + V_{drain}\left(e^{1/\beta_{eff}}\right)}{\left(V_{bi} + V_{fb} - V'_g\right)\left(e^{1/\beta_{eff}} - 1\right) - V_{drain}}\right) \quad (7)$$

here z_{min} is the location of minimum potential in the channel.

$$\beta_{sym} = \frac{1}{2}\sqrt{W_{fin}\left(\frac{\varepsilon_{si}t_{ox}}{\varepsilon_{ox}} + z - \frac{z^2}{W_{fin}}\right)} \qquad (8)$$

$$\beta_{\text{asym}} = \frac{1}{2}\sqrt{\mathrm{H}_{\text{fin}}\left(\frac{2\varepsilon_{\text{si}}\mathrm{t}_{\text{ox}}}{\varepsilon_{\text{ox}}} + 2\mathrm{x} - \frac{\mathrm{x}^2}{\mathrm{H}_{\text{fin}}}\right)} \; . \qquad (9)$$

For most Leakey path we consider

z =W/4;

x =H/4;

β_{sym} and β_{asym} is the characteristic field penetration length at the effective conductive path. For Re-TGFinFET we consider both the case of symmetric and asymmetric DGFinFET.

$$\beta_{eff} = \frac{1}{\sqrt{\left(\frac{1}{\beta_{sym}}\right)^2 + \left(\frac{0.5}{\beta_{asym}}\right)^2}} \qquad (10)$$

$$W_{fin} = \frac{W_{top} + W_{bottom}}{2} \qquad (11)$$

$$Q_{th} = \frac{2V_{th}}{q} \times \frac{C^2{}_{ox}}{C_{si}} \qquad (12)$$

where Q_{th} is minimum carrier sheet density required to turn on in the strong inversion condition.

Acknowledgement

The Author would like to thank to Mr. Amit Saini from COGENDA GENIUS TCAD for his kind support and motivation.

References

[1] G. Moore, "Cramming more components onto integrated circuits", Proc. of the IEEE, **86**, 82-85 (1998).

[2] Kaushik Roy, Saibal Mukhopadhyay, "Leakage Current Mechanisms and Leakage Reduction Techniques in Deep-Sub micrometer CMOS Circuits", Proc. of the IEEE, **91**, 305-327 (2003).

[3] J.-T. Park and J.-P. Colinge, "Multiple-gate SOI MOSFETs: Device design guidelines", IEEE Trans. Electron Devices, **49**, 2222-2229 (2002).

[4] Isabelle Ferain, Cynthia A. Colinge, Jean-Pierre Colinge, " Multigate transistors as the future of classical metal–oxide–semiconductor field-effect transistors", Review nature, **479**, 310-316 (2011).

[5] Sanchit Singhal, Sujeet Kumar, Shipra Upadhyay and R.K.Nagaria, "Comparative Study of Double Gate SOI FinFET and Trigate Bulk MOSFET Structures", IEEE conference on Engineering and Systems (SCES), Allahabad, India, 1-5 (2013).

[6] Debajit Bhattacharya and Niraj K. Jha, "FinFETs: From Devices to Architectures", Advances in Electronics, Hindawi Publishing Corporation, 2014.

[7] A. Burenkov, J. Lorenz, "Corner Effect in Double and Triple Gate FinFETs", IEEE conference on European Solid-State Device Research (ESSDERC), Estoril, Portugal, 135-138 (2003).

[8] Alexander Kloes, Michaela Weidemann, Daniel Goebel, and Bryan T. Bosworth, "Three dimensional closed-form model for potential barrier in undoped FinFETs resulting in analytical equations for V_T and sub threshold slope", IEEE Trans. Electron Devices, **55**, 3467-3475 (2008).

[9] Hyohyun Nam and Changhwan Shin, "Impact of Current Flow Shape in Tapered (Versus Rectangular) FinFET on Threshold Voltage Variation Induced by Work-Function Variation", IEEE transaction on electron device, **61**, 2007-2011 (2014).

[10] Vaidy Subramanian, Bertrand Parvais, Jonathan Borremans, Abdelkarim Mercha, Dimitri Linten, Piet Wambacq, Josine Loo, Morin Dehan, Cedric Gustin, Nadine Collaert, Stefan Kubicek, Robert Lander, Jacob Hooker, Florence Cubaynes, Stephane Donnay, Malgorzata Jurczak, Guido Groeseneken, Willy Sansen, and Stefaan Decoutere, "Planar Bulk MOSFETS Versus FinFETs: An Analog/RF Perspective", IEEE Trans. Electron Devices, **53**, 3071-3079 (2006).

[11] Yuan Taur, Xiaoping Liang, Wei Wang and Huaxin Lu, "A Continuous, Analytic Drain-Current Model for DG MOSFETs", IEEE Trans. Electron Devices, **25**, 107-109 (2004).

[12] A. Ortiz-Conde, F.J. Garcıa Sanchez, J.J. Liou, A. Cerdeira, M.Estrada, Y. Yue, "A review of recent MOSFET threshold voltage extraction methods", Microelectronics Reliability, **42**, 583-596 (2002).

[13] Nikolaos Fasarakis, Andreas Tsormpatzoglou, Dimitrios H. Tassis, Ilias Pappas, Konstantinos Papathanasiou Matthias Bucher, Gerard Ghibaudo and Charalabos A. Dimitriadis, "Compact Model of Drain Current in Short-Channel Triple-Gate FinFETs", IEEE transaction on electron device, **59**, 1891-1898 (2012).

[14] Tamara Rudenko, Valeriya Kilchytska, Nadine Collaert, Malgorzata Jurczak, Alexey Nazarov and Denis Flandre, "Carrier Mobility in Undoped Triple-Gate FinFET Structures and Limitations of Its Description in Terms of Top and Sidewall Channel Mobilities", IEEE Trans. Electron Devices, **55**, 3532-3541 (2008,).

[15] Renato Giacominia and João Antonio Martinob, Trapezoidal Cross-Sectional Influence on FinFET Threshold Voltage and Corner Effects", Journal of The Electrochemical Society, **155**, 213-217 (2008).