Journal of Electron Devices, Vol. 21, 2015, pp. 1801-1805

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Journal of Electron Devices
www.jeldev.org

# REALIZATION OF ULTRA LOW VOLTAGE CIRCUIT DESIGN FOR INTERNET OF THINGS

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Received 24-12-2014, online 6-01-2015

## ABSTRACT

This paper presents realization of ultra low voltage circuit design for Internet of Things. Internet of Things (IoT) is an emerging field and has gained more attention among the researchers. This is a rapidly emerging application that allows people and things to be connected anywhere and anytime, using any path or network. IoT devices can communicate among themselves and perform the desired action with or without human interface. Semiconductor industries are investing heavily in introducing power saving features by using ultra low voltage circuit design as these devices depend heavily on portable battery or external power source. Hence research is needed on reducing the power dissipation by designing ultra low voltage circuit design for IoT devices. Ultra low voltage circuit design for Internet of Things is realized by simulating a two input NAND gate in 120nm CMOS technology. All simulations are performed by using Microwind ver. 3.1 EDA tool.

**Keywords:** Internet of Things, Ultra low voltage circuit, Low power, MTCMOS technique, SCCMOS technique.

## I. INTRODUCTION

Internet of Things (IoT) is an integrated global network infrastructure where physical and virtual "things" have identities and use intelligent interfaces to communicate among themselves. This infrastructure allows interaction among interconnected nodes and objects (physical and virtual) by using different communication protocols and also acts an integrated network that can be deployed in inaccessible and remote areas [1]. In the IoT, "things" can interact and communicate among themselves and with the environment by collecting information and data from the environment, and perform the right action with or without human interaction [2]. Hence Internet of Things (IoT) can also be considered as an integrated part of future internet.

The Internet of Things allows "things" to be connected anytime with anything using any path or network and by using any service. Fig. 1 shows the interconnection among things in the Internet of Things [3]. The physical and virtual things can sense, communicate, interact, exchange data, information and knowledge among themselves and with the environment. This is done by addressing elements such as convergence, content, collections, computing, communication, and connectivity among the things.

Fig. 2 shows interactions among the physical, digital, virtual worlds in the Internet of Things [3].

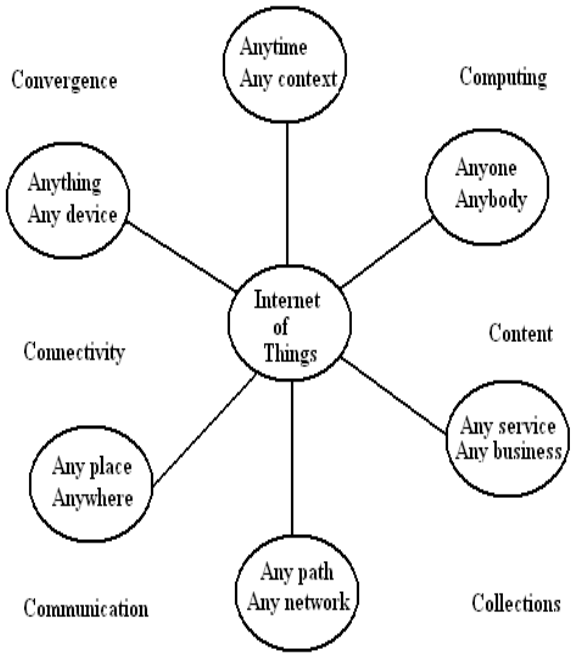


**Figure 1:** Interconnection among things in the Internet of Things

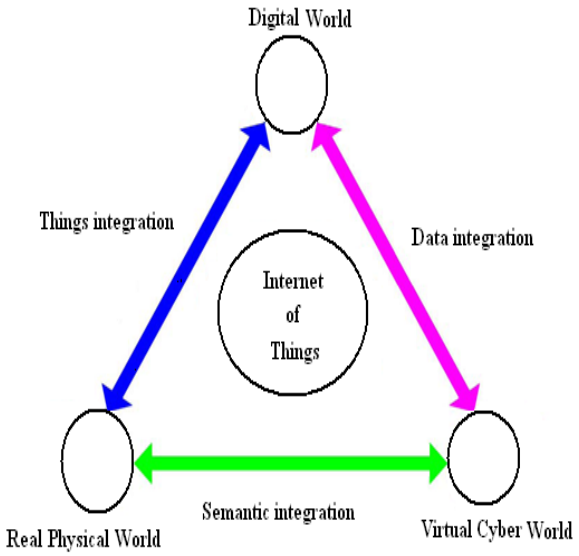


**Figure 2:** Internet of Things: Interactions among the physical, digital, virtual worlds

In this paper, ultra low voltage circuit design for Internet of Things is presented. Section II describes about ultra low voltage circuit design for Internet of Things. Reduction in the supply voltage is the most significant method for reducing the power dissipation. In section III, ultra low voltage circuit design is realized for internet of things through the layout design and simulation of a two input NAND gate in 120nm CMOS technology. A two input NAND gate is simulated using the existing MTCMOS and SCCMOS circuit techniques. Finally, conclusion is provided in section IV.

## II. ULTRA LOW VOLTAGE CIRCUIT DESIGN FOR INTERNET OF THINGS

The "things" in the IoT applications need external power to perform any function. As a result, IoT devices must offer superior power efficiency so that they can operate efficiently using a battery. In addition, these devices must operate for years without requiring battery replacement [4]. Hence ultra low voltage circuit design is highly desirable for ultra low power dissipation in these devices to meet the power requirements.

With the increasing demand of battery operated IoT devices, it is important to increase the battery life as much as possible. Although the battery industry has been making efforts to develop batteries with a higher energy capacity, however a revolutionary increase in the energy capacity does not seem imminent [5]. In the absence of ultra low voltage/ultra low power circuit design techniques, present and future IoT devices will either suffer from a very short battery life or a very heavy battery pack. So, IoT devices that are powered with batteries require low voltage circuit design for increasing their lifetime. Low voltage circuit design is highly desirable for burst mode type IoT devices also, where computation occurs for only short duration, and the system is inactive for the majority of time. For such type of battery operated devices, it is highly unacceptable to have excessive drainage of useful battery power during the long standby period. Consequently, reducing the power dissipation by utilizing low power circuit design is becoming a top priority issue.

Reduction in the supply voltage ($V_{DD}$) is the most significant method for reducing the power dissipation because of the quadratic relationship between the supply voltage and the dynamic power dissipation [6].

The generalized expression for the dynamic power dissipation can be written as [7]

$$P_d = \alpha_T C_{load} V_{DD}^2 f_{clk} \quad (1)$$

here $\alpha_T$ is the switching activity factor, $C_{load}$ represents the total load capacitance, $V_{DD}$ is the supply voltage, and $f_{clk}$ represents the switching frequency.

Eqn. (1) indicates that the supply voltage is the dominant factor in the dynamic power dissipation. Thus reducing the supply voltage ($V_{DD}$) is the most effective method to reduce the power dissipation.

To compensate for the performance loss in terms of speed due to a lower supply voltage, threshold voltage of device is also reduced. However, this causes an increase in the leakage current. Among all leakage currents, subthreshold leakage current is the most dominant [8]. The reduction in the threshold voltage leads to an increase in the subthreshold leakage current. This leakage current is caused by the inability to completely turn off a device. This leakage current in the standby mode will become a large component in the total power dissipation with further down scaling in technology. Therefore, today an important research area in achieving low power dissipation is to develop effective ultra low voltage circuit techniques to reduce this leakage current in the standby mode that is mainly caused by the reduction in the threshold voltage of MOS transistors and down scaling in technology [9-11].

The most commonly used subthreshold leakage reduction techniques are source biasing

technique [12], stack technique [13], dual VTH partitioning technique [14], variable threshold CMOS (VTCMOS) technique [15], multi-threshold CMOS (MTCMOS) technique [16], sleepy keeper technique [17], and super cutoff CMOS (SCCMOS) technique [18]. Out of these techniques, MTCMOS technique, and SCCMOS technique are mostly used for reducing the standby subthreshold leakage power dissipation. Minimizing this leakage power dissipation is highly desirable for IoT devices that are powered with batteries. In burst mode type battery operated IoT devices, reduction of this leakage power greatly improves their battery lifetime, as these systems spend majority of their time in the standby or idle mode [19]. Hence nowadays researchers are focusing on the development of effective and improved circuit techniques for further reduction of this standby leakage power dissipation.

## III. SIMULATION RESULTS AND OBSERVATIONS

Ultra low voltage circuit design is realized for internet of things through the layout design and simulation of a two input NAND gate at a temperature of $27^0$C and supply voltage of 0.90V using BSIM4 MOS parameter model in 120nm CMOS technology. W/L of low $V_{TH}$ nMOS and low $V_{TH}$ pMOS transistors are taken as 0.72µm/0.12µm and 1.20µm/0.12µm respectively. Similarly, W/L of high $V_{TH}$ nMOS (sleep nMOS) and high $V_{TH}$ pMOS (sleep pMOS) transistors are taken as 0.72µm/0.24µm and 1.20µm/0.24µm respectively. Performance characteristics such as subthreshold leakage power dissipation in the standby mode and circuit propagation delay of the logic gate are measured using existing circuit techniques (MTCMOS and SCCMOS techniques). Standby subthreshold leakage power dissipation for a two input NAND gate is measured by combining all possible static input combinations (A and B), in such a way that the voltage magnitude of the inputs are always less than the threshold voltage of low $V_{TH}$ MOS transistors of a two input NAND gate. This standby leakage power dissipation is measured for 50ns time interval using MTCMOS and SCCMOS techniques.

Circuit propagation delay of a two input NAND gate is measured from the trigger input edge reaching 50% of $V_{DD}$ to the circuit output edge reaching 50% of $V_{DD}$.

Figures 3-4 show the layout diagrams of a two input NAND gate using MTCMOS technique and SCCMOS technique respectively. In MTCMOS technique, sleep transistors are turned off during the standby mode by the application of sleep signal to sleep pMOS transistor and sleep bar signal to sleep nMOS transistor respectively. In SCCMOS technique, sleep transistors are completely cutoff during the standby mode due to the application of positive and negative gate voltages ($V_{GS1}$ and $V_{GS2}$) to sleep pMOS transistor and sleep nMOS transistor respectively. Hence the subthreshold leakage current in the standby mode reduces exponentially. Figs. 5 - 6 show the output waveforms of a two input NAND gate using MTCMOS technique and SCCMOS technique respectively. Table 1 show the performance characteristics, such as subthreshold leakage power dissipation in standby mode and propagation delay for a two input NAND gate by using the existing MTCMOS and SCCMOS techniques.

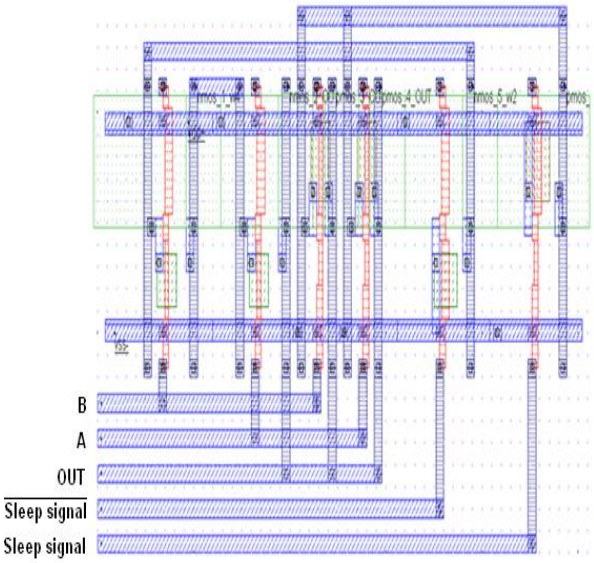


**Figure 3:** Layout of a two input NAND gate using MTCMOS technique

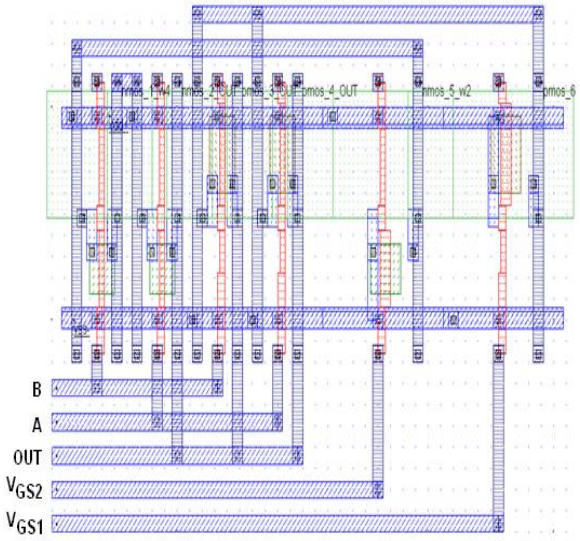


**Figure 4:** Layout of a two input NAND gate using SCCMOS technique

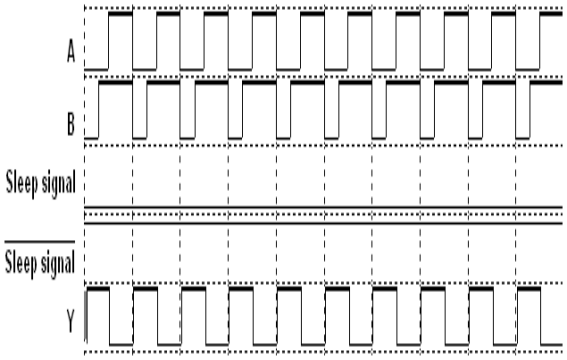


**Figure 5:** Output waveform of a two input NAND gate using MTCMOS technique

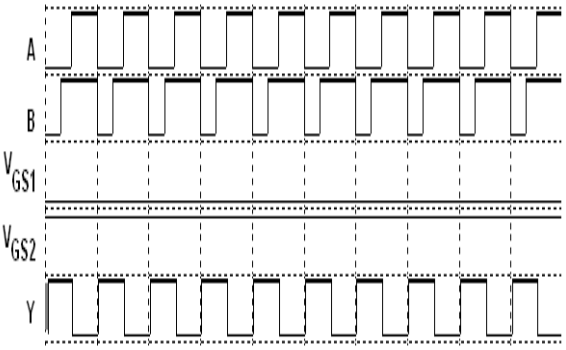


**Figure 6:** Output waveform of a two input NAND gate using SCCMOS technique

Table 1 Performance characteristics of a two input NAND gate using existing circuit techniques (MTCMOS and SCCMOS techniques)

| **Circuit design techniques** | **Technology** | **Standby subthreshold leakage power** | **Circuit propagation delay** |
|---|---|---|---|
| MTCMOS | 120nm CMOS | 0.039 nW | 16.2 x $10^{-12}$ sec |
| SCCMOS | 120nm CMOS | 0.030 nW | 12.8 x $10^{-12}$ sec |

It is observed from Table 1 that a two input NAND gate using the SCCMOS technique dissipates only 0.030 nW of subthreshold leakage power in the standby mode. A two input NAND gate designed using SCCMOS technique dissipates lesser standby subthreshold leakage power as compared to a two input NAND gate designed using MTCMOS technique. Effective ultra low voltage circuit design technique can be used for further minimizing this power dissipation, which would greatly benefit in extending the battery life of IoT devices.

## IV. CONCLUSION

The Internet of Things (IoT) is an emerging field and offers a vast opportunity for the semiconductor industries. However, severe power constraints provide serious challenges for the future aspect of IoT. Hence research is needed in designing ultra low voltage circuit for Internet of Things for reducing the power dissipation. The standby subthreshold leakage power increases exponentially with the down scaling in technology and thus it will contribute a larger percentage in the overall power dissipation with further down scaling in technology, especially in burst mode type IoT devices. Research is needed on introducing power saving features by using ultra low voltage circuit design in IoT devices. Hence, there is a great need for ultra low voltage circuit design for Internet of Things for further minimizing this standby leakage power for saving useful battery power.

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