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COMPARATIVE ANALYSIS OF LEAKAGE POWER WITH 10 NM CHANNEL LENGTH IN MOSFET/CNTFET DEVICES

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ABSTRACT

The exponential increase of leakage currents in a scaled device is an inevitable consequence of MOSFET physics. Unfortunately constant field scaling reaches a performance limit. As the devices scaled down in nanometer regime the threshold voltage is also scaled, consequently the leakage power increases. If the channel length becomes too short, the depletion region from the drain can reach the source side and reduces the barrier for electron injection. In this paper we have analyzed the impact of channel length over threshold voltage of the CNTFET and MOSFET devices. With an analysis of HSPICE simulation results we found that the threshold voltage increases with decreasing channel length over a wide range of channel length in CNTFET that is not possible to get in MOSFET devices. The increase in threshold voltage in nanometer regime leads to reduce the leakage power and hence the CNTFET emerges as a power saving devices.

Keywords: CNTFET, MOSFET, threshold voltage, channel length.

I. INTRODUCTION

VLSI is characterized by the exponential growth of the number of transistor per chip. Gordon Moore noted that the number of transistor per chip wills double every 18 to 24 month [1].The most important field effect transistor is the MOSFET. In silicon MOSFET, the gate contact is separated from the channel by an insulating silicon dioxide layer. The charge carriers of the conducting channel constitute an inversion charge, that is, electrons in the case of n-channel device or holes in the case of p-channel device. The electrons enter and exit the channel at n^+ source and drain contacts in the case of an *n*-channel MOSFET, and at p^+ contacts in the case of a *p*-channel MOSFET. Beside the speed of a digital integrated circuit, the power dissipation has always been an important issue. Power delivery to the chip and thermal management are the challenges for high performance applications. As the performance is the main driver of technology development, ideal scaling rules have often been involved. However, leakage current shows a scaling behavior inverse to dynamic losses, so leakage power consumption is a new challenge which arises in the nanometer regime. The exponential increase of leakage currents in a scaled device is an inevitable consequence of MOSFET physics. Unfortunately constant field scaling reaches a performance limit. This is due to some non scaling quantities that make an ideal constant field scaling impossible. Several circuit techniques to reduce the leakage power consumption have been proposed in literature. Even though the principle of these techniques is simple, the devil is in the implementation details. The first challenge is to determine whether a certain technique works in a particular technology. These limits can be overcome to some extent and facilitate further scaling down of device dimensions by modifying the channel material in the traditional MOSFET structure with a single carbon nanotube [2]. Field-effect transistors based on carbon nanotubes have been a focus of active research in recent years [3-9].

II. PHYSICS

MOSFET is voltage controlled device, which has four terminals such as source, Drain, gate and body. If no positive voltage is applied between gate and source the MOSFET is always none conducting. When we apply a positive voltage (in case of N-type MOSFET), as shown in Fig.1, to the gate, the positive gate voltage will push away the holes inside the p-type substrate and attracts the electrons in the n-type regions under the source and drain electrodes. This produces a layer on silicon surface just under the gate oxide through which electrons can get into and move along from source to drain. The positive gate voltage therefore creates a channel in the top layer of material between oxide and p-Si. Increasing the value of the positive gate voltage pushes the p-type holes further away and enlarges the thickness of the created channel. As a result we find that the size of the channel increases with the size of the gate voltage and enhances the amount of current which can go from source to drain.

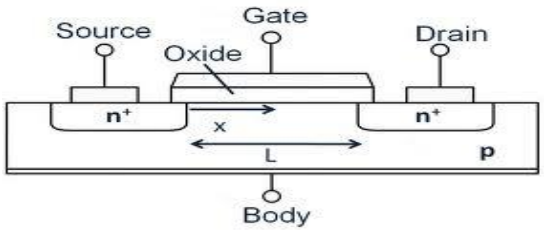

Fig.1: Structure of MOSFET device.

As the gate length is reduced, the characteristics of a MOSFET changes due to short channel effects. At short gate lengths, MOSFETs suffer from following parameters such as threshold voltage shift, increase leakage current and increased output conductance.

CNTFET uses CNT shown in Fig.2 (a), as a channel between source and drain in conventional silicon MOSFET. It may be single wall nanotube or multi wall nanotube, depending upon the number of tubes used as a channel.

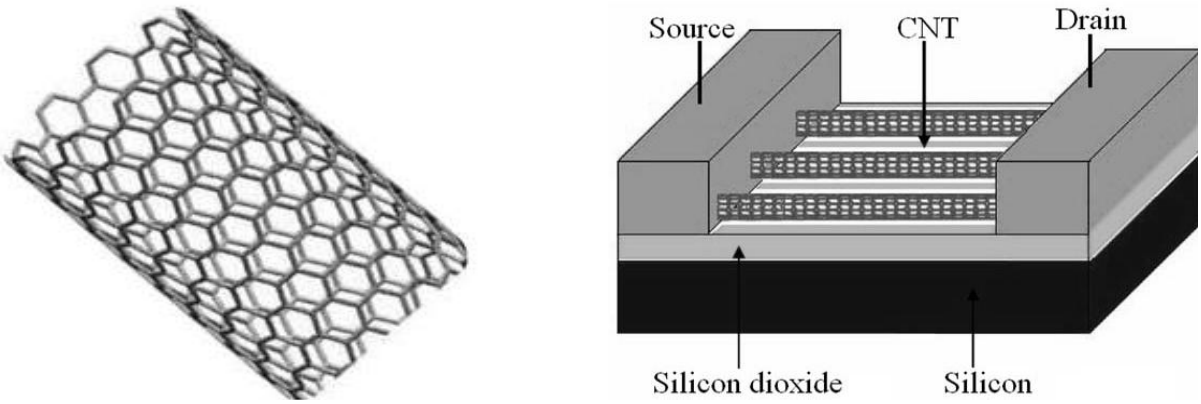

Fig.2: (a) Carbon nanotube ; (b) Structure of CNTFET device

The structure of CNTFET shown in Fig.2 (b), is almost the same like silicon MOSFET except the CNT is attached in the transistor and acts as the channel. CNTFET operates on the same principle of MOSFET as the electrons travel from the source terminal to the drain terminal.
Carbon nanotube (CNT) is a promising alternative to conventional silicon technology for future nanoelectronics because of their unique electrical properties. Carbon nanotubes are rolled up sheets of grapheme. CNT is exceptional in that it has a perfect crystalline structure, which is composed of strong covalent C-C bonds. Semiconducting SWNTs are of special interest because they are promising in producing semiconducting devices that rival devices made by traditional Si technology [10]-[11].

Quantum capacitance (Qc) has important impact in nanoscale devices [13], it is the properties of channel material. Since the density of state is finite in a semiconductor quantum well, the Fermi level needs to move up above the conduction band edge as the charge in the quantum well increases. This movement of Fermi level requires energy and this conceptually corresponds to quantum capacitance [14].

In the result shown in Table I, the input parameters for single gate MOSFET such as body thickness (which is of silicon) is 1.00E-08 m and insulator dielectric constant is 3.9 at 30 K temperature are considered. The step gate voltage is considered for simulation is 0.083V, where the initial gate voltage is 0 V and the final gate voltage is 1 V. These considerations are the same for all oxide thickness values (0.7 nm, 0.9 nm, 1.2 nm, 1.5 nm). In the result shown in Table II, the input parameters for CNTFET such as nanotube diameter is 1.00E-09 m and insulator dielectric constant is 3.9 at 30 K temperature are

considered. Here the step gate voltage 0.O83 V is also considered for simulation, the initial gate voltage is 0 V and the final gate voltage is 1 V.

TABLE I
CHARACTERISTICS OF MOSFET

MOSFET				
Gate Voltage (V)	Quantum Capacitance (F/cm2)			
	Tox = 0.7nm	Tox = 0.9nm	Tox = 1.2nm	Tox = 1.5nm
0	2.10E-10	2.10E-10	2.10E-10	2.10E-10
0.083333	3.58E-09	3.58E-09	3.57E-09	3.57E-09
0.166667	6.00E-08	5.98E-08	5.95E-08	5.93E-08
0.25	8.31E-07	8.03E-07	7.65E-07	7.32E-07
0.333333	4.41E-06	4.01E-06	3.56E-06	3.21E-06
0.416667	8.47E-06	7.74E-06	6.86E-06	6.17E-06
0.5	1.08E-05	1.02E-05	9.25E-06	8.47E-06
0.583333	1.19E-05	1.15E-05	1.07E-05	1.00E-05
0.666667	1.24E-05	1.21E-05	1.16E-05	1.11E-05
0.75	1.26E-05	1.25E-05	1.21E-05	1.17E-05
0.833333	1.27E-05	1.26E-05	1.24E-05	1.21E-05
0.916667	1.28E-05	1.27E-05	1.26E-05	1.24E-05
1	1.28E-05	1.27E-05	1.27E-05	1.25E-05

TABLE II
CHARACTERISTICS OF CNTFET

CNTFET				
Gate Voltage (V)	Quantum Capacitance (F/cm)			
	Tox = 0.7nm	Tox = 0.9nm	Tox = 1.2nm	Tox = 1.5nm
0	1.37E-16	1.37E-16	1.37E-16	1.37E-16
0.083333	2.32E-15	2.32E-15	2.32E-15	2.32E-15
0.166667	3.88E-14	3.87E-14	3.86E-14	3.85E-14
0.25	5.09E-13	4.96E-13	4.82E-13	4.70E-13
0.333333	2.30E-12	2.18E-12	2.04E-12	1.94E-12
0.416667	3.67E-12	3.57E-12	3.42E-12	3.20E-12
0.5	3.37E-12	3.78E-12	3.82E-12	3.81E-12
0.583333	3.21E-12	3.38E-12	3.56E-12	3.67E-12
0.666667	2.74E-12	2.91E-12	3.12E-12	3.28E-12
0.75	2.43E-12	2.56E-12	2.74E-12	2.89E-12
0.833333	2.24E-12	2.33E-12	2.47E-12	2.60E-12
0.916667	2.11E-12	2.18E-12	2.29E-12	2.39E-12
1	2.02E-12	2.08E-12	2.16E-12	2.24E-12

Plot of gate voltage vs. quantum capacitance of MOSFET, is shown here in Fig. 3(a), where we can see that after decreasing the gate oxide thickness the quantum capacitance increases for the different gate voltages leading to higher gate capacitance. Whereas in case of CNTFET under identical simulating condition as in case of single gate MOSFET, we observe that as the oxide thickness goes down from 1.5 nm to 0.7 nm the quantum capacitance decreases as shown in Fig. 3(b), when we apply gate voltages from 0.5 V and above leading reduced quantum capacitance [15].

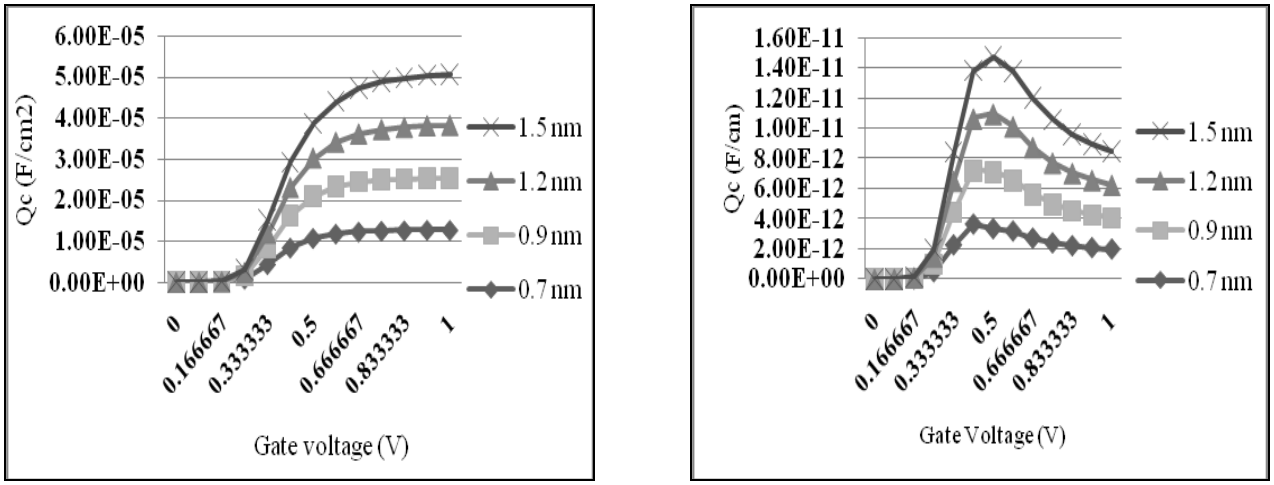

Fig.3: (a) MOSFET characteristics; (b) CNTFET characteristics

For CNTFET quantum capacitance goes to lesser and lesser values, while in MOSFET the value of quantum capacitance goes on increasing which leads increased propagation delay and hence performance degradation [13].

III. LEAKAGE POWER ANALYSIS

Leakage current has become the limiting factor for oxide thickness thinner than 1.5 nm. Decreasing the channel length increases the current drive of the transistor. Much of the scaling is therefore driven by decrease in channel length. If only this parameter is scaled many problems are encountered, such as increased electric field. If the channel length becomes too short, the depletion region from the drain can reach the source side and reduces the barrier for electron injection [16]. This is known as punch through, and because of this, devices characteristics degrade as shown in Fig.4. Minimization of leakage currents is important in VLSI. As the devices scaled down in nanometer regime the threshold voltage is also scaled, consequently the leakage power increases [17-19].

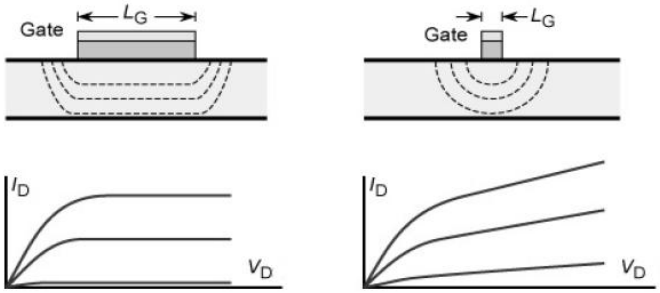

Fig.4: Short channel effect on MISFET device.

In long channel length devices, the gate is responsible for depleting the semiconductor. In short channel devices, part of the depletion is accomplished by the drain and source bias. Since less gate voltage is required to transistor deplete, the barrier for electron injection from source to drain decreases. This is known as drain induced barrier lowering.

IV. RESULT AND DISCUSSIONS

For MOSFET and CNTFET devices we have considered the channel length range from 100 nm to 10 nm. It can be observed that in CNTFET as the channel length goes down from 20 nm to 10 nm the threshold voltage increases rapidly. Plot of characteristics of threshold voltage with respect to different channel length of CNTFET devices is shown in Fig.5, whereas in the case of MOSFET devices the threshold voltage decreases sharply while channel length reduces from 20 nm to 10 nm.

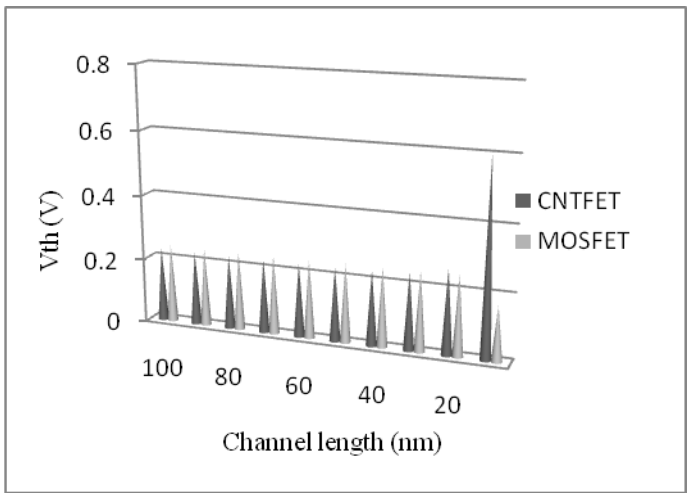

Fig.5: Threshold voltage w.r.t channel length.

Comparison of threshold voltage with respect to channel length of CNTFET and MOSFET devices is shown in Fig. 6. Below 20 nm channel length the threshold voltage increases rapidly in case of CNTFET device and the threshold voltage goes on decrease

in case of MOSFET, which leads to more leakage power and finally device degrades in term of performance. The advantage of using CNTFET device in nanometer regime is to increased threshold voltage at 10 nm and beyond channel length. In case of MOSFET while reducing the channel length the threshold voltage is also reduced which lead to more leakage power.

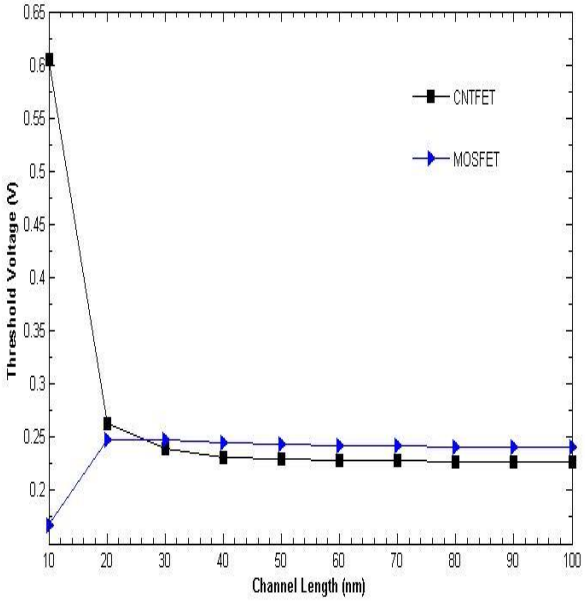

Fig.6: Threshold voltage with respect to channel length of CNTFET and MOSFET devices

V. CONCLUSION

In this paper we have justified the advantage of CNTFET over MOSFET. We have analyzed the impact of channel length over threshold voltage of the CNTFET and MOSFET devices. As the devices scaled down in nanometer regime the threshold voltage is also scaled, consequently the leakage power increases. After analysis of simulation results obtained with HSPICE we found that the threshold voltage increases with decreasing channel length over a wide range of channel length in CNTFET that is not possible to get in MOSFET devices. The increase in threshold voltage in nanometer regime leads to reduce the leakage power and hence CNTFET device emerges as a power saving devices.

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