Journal of Electron Devices, Vol. 20, 2014, pp. 1724-1728

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Journal of Electron Devices
www.jeldev.org

INFLUENCE OF THE TWO-DIMENSIONAL ANALYSIS ON THE MESFET TRANSISTOR CHARACTERISTICS

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Received 10-06-2014, online 24-06-2014

ABSTRACT

A two-dimensional numerical analysis is presented to investigate the field effect transistor characteristics. Our main aim is related to the optimization of a two dimensional (2D) analytical model for the static characteristics of short gate-length GaAs MESFET's. The model takes into account the different physical specific phenomena of the device and we consider also the influence of the two-dimensional analysis on the variation of some intrinsic elements (transconductance and drain conductance). The suggested model enables to calculate and trace informative curves. The results obtained are well represented and interpreted.

Key words: MESFET, Two-dimensional modeling, Edge effects, Characteristics (I-V, Gm, Gd).

I. INTRODUCTION

With current technological progress, the submicron components are more powerful, but the complexity of their function increases as soon as dimensions are reduced. The development and the improvement of new dies of components require new results from modelling, new realisations and new characterisations [1,6]. It is thus very significant to predetermine the characteristic of the component, physical-modelling finds here one of its principal application.

In order to take into account the complexity of the structure of field-effect transistors with submicron gate, the designers must know the influence of the technological parameters for predictions on the behaviour of the device. In this paper the edge effects have been taken into account and their influence on the current voltage characteristics, on the transconductance, and on drain conductance are investigated.

In this work we perform two-dimensional simulations of components and we consider the effects of edge and the parasitic resistances, of source, and of drain, for our proposed structure.

II. MODEL AND VOLTAGE-CURRENT (I-V) EQUATIONS

In a submicron MESFET, the channel potential cannot be entirely controlled by the gate bias and will be shifted by the penetration of lateral electric field. Therefore the lateral field distribution at the gate edges plays an important role for the short channel effects.

Thus solution for 2D Poisson's equation satisfying suitable boundary conditions is required to model the short channel effect. A simplified [1] self aligned GaAs MESFET is shown in Fig.1. Poisson's equation is solved for the potential distribution $V_c(x,y)$, where 'L' is the gate length. '**a**' is the thickness of the active layer.

In order to avoid the problems resulting from different surface boundary conditions, the n-GaAs layer is assumed to contact directly to the gate metal, and the absorption of electric field by the depletion charges near the source/drain is not taken into account.

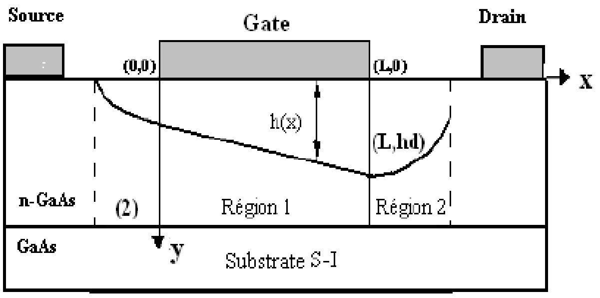

Figure1: Schematic diagram of a self-aligned GaAs MESFET

II.1 Calculation of the potential in the channel and the electrical field

The 2D Poisson equation for the depletion region, assuming complete depletion, is

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$$\nabla^2 V_c(x,y) = \frac{d^2V_c}{dx^2} + \frac{d^2V_c}{dy^2} = -\frac{q}{\varepsilon} N_d(y) \qquad (1)$$

$V_c(x,y)$ is the electrostatic potential, *q* is electron charge, *ε* is the dielectric permittivity of GaAs semiconductor, *$N_d(y)$* is the doping concentration. The doping is considered to be uniform.

According to the superposition technique [2], Eq. (1) can be resolved as

$$V_c(x,y) = V(x,y) + V_l(x,y) \qquad (2)$$

where *$V(x,y)$* is the solution of Poisson's equation (3) for the MESFET structure in one dimension along y-axis near the mid of the channel (region 1). It is this potential profile that would result if the device were completely unaffected by lateral electric fields from the source and the drain. *$V_l(x,y)$* is the 2D potential function responsible for the short channel effects [6], it represents the voltage brought by the overflow of the depletion region at the drain and source sides (region2):

$$\frac{d^2V(x,y)}{dy^2} = -\frac{q}{\varepsilon} N_d(y) \qquad (3)$$

$$\frac{d^2V_l}{dx^2} + \frac{d^2V_l}{dy^2} = 0 . \qquad (4)$$

To find solution of equations (3) and (4), we used the boundary conditions expressed as [3]:

$$V(x,y)\big|_{y=0} = Vg - Vbi \qquad (5)$$

$$\left.\frac{dV(x,y)}{dy}\right|_{y=a} = 0 \qquad (6)$$

$$V_c(L,y) = V_{bi} + V_d , \quad V_l(L,y) = V_{bi} + V_d - V(y) \qquad (7)$$

$$\frac{dV_c(x,a)}{dy} = 0, \quad \frac{dV_l(x,a)}{dy} = 0, \quad \frac{dV_c(L,a)}{dx} = E_s \qquad (8)$$

where V_{bi} is the potential of built-in Schottky-barrier, V_g is the applied gate-source voltage, V_d is the applied drain-source voltage and E_s is the saturation electric field.

Using (5) and (6) in (3), the solution of 1D Poisson's equation is based on the fact that the depletion layer thickness under the gate, *$h(x)$* is a slowly varying function in the channel.

The channel potential is obtained by integration limits with y = h(x)

$$V(x,y) = \frac{q}{\varepsilon}\int_0^{h(x)} yNd(y)dy + Vg - Vbi \qquad (9)$$

So :

$$V(x) = \frac{qN_d}{2\varepsilon} h^2(x) + Vg - Vbi \qquad (10)$$

$$h(x) = \sqrt{\frac{2\varepsilon\left(V(x) + V_{bi} - V_g\right)}{qN_d}} \qquad (11\text{-}1)$$

where *$V(x)$* is the potential of the neutral channel with *$V(0) = 0$* at the source-end and *$V(L) = V_d$* at the drain-end. So that the depletion widths at the source and drain ends given respectively by :

$$h_s = \sqrt{\frac{2\varepsilon\left(V_{bi} - V_g\right)}{qN_d}} \qquad (11\text{-}2)$$

$$h_d = \sqrt{\frac{2\varepsilon\left(V_d + V_{bi} - V_g\right)}{qN_d}} . \qquad (11\text{-}3)$$

To determine the two-dimensional term *$V_l(x,y)$* in the frame of boundary condition Eqs (4,7,8), the solution suggested in this study may be written in the following form[1,6].

$$V_l(x,y) = \alpha\left[Sinh(k(L-x)) + Sinh(kx)\right]Sin(ky) \qquad (12)$$

where

$$k = \frac{\pi}{2a} \qquad \alpha = \frac{2aE_s}{\pi(\cosh(kL) - 1)} .$$

Following (2), (10) and (12) the expression for the two dimensional potential of the channel under the gate with edge effects, is given as follows:

$$V_c(x,y) = \frac{qN_d}{2\varepsilon} h^2(x) + Vg - Vbi + V_l(x,y) . \qquad (13)$$

II.2 Current-voltage characteristics I –V

In order to calculate the drain current expression as a function of the drain voltage for different values of the gate voltage, we use the following hypothesis:

- We neglect the current in the Y axis; this approximation is valid for the short gate components.
- The channel is divided in two regions according to the value of the electric field.
- The analytical expression of the variations of the electron mobility with electric field [4] is given by:

• For the low electric fields: *$E < E_0$*

$$\mu = \mu_0 \qquad (14\text{-}1)$$

• For the electric fields higher than *E_0* : (*$E \geq E_0$*)

$$\mu = \frac{\mu_0}{\left[1 + \left(\frac{E - E_0}{E_s}\right)^2\right]^{1/2}} \qquad (14\text{-}2)$$

where: *E* is the electric field, *μ_0* is the low mobility, and *E_0* is a critical field (*E_0* = 3, 5 kV/cm for the *GaAs* [4]) .

The density of the current is given by:

$$j_x = \sigma(x, y, z).E_x \qquad (15)$$

$$j_x = q\mu N_d.E_x = -q\mu N_d.\frac{dV_c(x, y)}{dx} \ . \qquad (16)$$

The drain current I_d *is* obtained by integrating J_x across the conductor section of the channel:

$$I_d = -\int_0^Z \int_{h(x)}^{a} j_x d_y d_z = -Z \int_{h(x)}^{a} j_x d_y \ . \qquad (17)$$

Using single integrals, the current expression is obtained by relation:

$$I_d = \frac{(qN_d)^2 Z\mu}{\varepsilon L}\left[\frac{a}{2}\left(W_d^2 - W_s^2\right) - \frac{1}{3}\left(W_d^3 - W_s^3\right)\right] \qquad (18)$$

where W_s and W_d are the two dimensional widths of the depletion layer side source and drain respectively. They are calculate by considering first the one-dimensional approximation *h(x)* then we have added the corrective term $V_l(x, h(x))$ which results [3] from the two dimensional analysis.

Equations (11-1, 11-2, 11-3) becomes as follows:

$$W(x) = \sqrt{\frac{2\varepsilon\left(V(x) + V_{bi} - V_g - V_l(x, h(x))\right)}{qN_d}} \qquad (19\text{-}1)$$

$$W_s = \sqrt{\frac{2\varepsilon\left(V_{bi} - V_g - V_l(0, h_s)\right)}{qN_d}} \qquad (19\text{-}2)$$

$$W_d = \sqrt{\frac{2\varepsilon\left(V_d + V_{bi} - V_g - V_l(L, h_d)\right)}{qN_d}} \ . \qquad (19\text{-}3)$$

By deferring two expressions (19-2) and (19-3) in equation (18) the general equation of current becomes:

Linear regime

the electric field in the channel is low and the electron mobility is equal to μ_0. Expression of the drain current in this regime can be written as:

$$I_d(V_d, V_g) = I_p\left[\begin{matrix}\dfrac{V_d - \left(V_l(L, h_d) + V_l(0, h_s)\right)}{V_p} - \dfrac{2}{3}\left(\dfrac{V_d + V_{bi} - V_g - V_l(L, h_d)}{V_p}\right)^{3/2} \\ + \dfrac{2}{3}\left(\dfrac{V_{bi} - V_g - V_l(0, h_s)}{V_p}\right)^{\frac{3}{2}}\end{matrix}\right] \qquad (20)$$

where $I_p = \dfrac{(qN_d)^2 Z\mu_0 a^3}{2\varepsilon L}$ and $V_p = \dfrac{qN_d}{2\varepsilon} a^2$

Saturation regime

drain voltage increases when the electric field in the channel increases beyond E_0. The electron mobility is given by (14-2).

The saturation value V_{dsat} is taken as the voltage where the conduction channel depleted near the drain. So:

$$V_{dsat} = V_p + V_g - V_{bi} + V_l(L, h_d) \ . \qquad (21)$$

The simplified expression for the saturation drain current is:

$$I_{dsat} = I_p\left[\frac{1}{3} - \left(\frac{V_{bi} - V_g - V_l(0, h_s)}{V_p}\right) + \frac{2}{3}\left(\frac{V_{bi} - V_g - V_l(0, h_s)}{V_p}\right)^{\frac{3}{2}}\right] \qquad (22)$$

with: $I_p = \dfrac{(qN_d)^2 Z\mu a^3}{2\varepsilon L}$

III. TRANSCONDUCTANCE AND DRAIN CONDUCTANCE

The expression of I_d is used to calculate the two basic parameters of the transistor, which are the transconductance g_m and the channel conductance g_d more commonly known as drain conductance.

The transconductance is the expression of the control mechanism of a transistor: it is an indication [5] of the variation of the current in the channel modulated by the gate voltage at constant drain-source voltage:

In the Linear regime

$$g_m = \frac{Z\mu_0}{L}(2\varepsilon qN_d)^{1/2}\left[\begin{matrix}\left(V_d + V_{bi} - V_g - V_l(L, h_d)\right)^{1/2} \\ -\left(V_{bi} - V_g - V_l(0, h_s)\right)^{1/2}\end{matrix}\right] . \qquad (23)$$

In the saturation regime

$$g_{msat} = \frac{Z\mu}{L}(2\varepsilon qN_d)^{1/2}\left[(V_p)^{1/2} - \left(V_{bi} - V_g - V_l(0, h_s)\right)^{1/2}\right] . \qquad (24)$$

The conductance reflects the resistance of the channel: it is the variation of the drain current according to the V_d voltage variation, with constant polarization of the gate:

In the Linear regime

$$g_d = \frac{Z\mu_0}{L}(2\varepsilon qN_d)^{1/2}\left[(V_p)^{1/2} - \left(V_d + V_{bi} - V_g - V_l(L, h_d)\right)^{1/2}\right] \qquad (25)$$

In the saturation regime

$$g_{dsat} = 0 \; . \qquad (26)$$

IV. INFLUENCE OF PARASITIC RESISTANCES

The characteristics that we have presented are those of the internal or intrinsic sizes *(I_d V_d, V_g)*. to obtain the external or extrinsic characteristics of the component *(I_{ds} V_{ds}, V_{gs})*, it is enough to take into account the effect of parasitic resistances to access of source and drain , and also the effect of parallel resistance to the canal on the values of polarization voltages [4] as shown in figure 2.

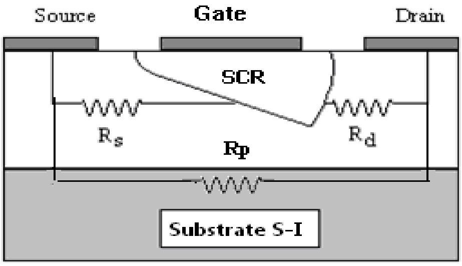

Figure 2 : Parasitic resistances in the MESFET GaAs.

To obtain the real expressions of characteristics I_d, g_d *and* g_m , it is enough to replace the intrinsic terms by the extrinsic terms in all the preceding relations:

$$\begin{aligned} I_d &= I_{ds} - (V_{ds} / R_p) \\ V_d &= V_{ds} - (R_s + R_d) I_d \\ V_g &= V_{gs} - R_s I_d \end{aligned} \qquad (27)$$

V. RESULTS AND DISCUSSIONS

Software of simulation based on the expressions established in the preceding paragraphs is realized in Matlab, The study was carried out on a submicron gate GaAs MESFET transistor which parameters gathered in the table (1).

L (μm)	a(μm)	Z(μm)	μo(m^2/Vcm)
1	0,153	100	0,2800
Nd(At/m^3)	**Vs(m/s)**	**Vbi(V)**	**Vp(V)**
1,17 10^{23}	3.6 10^5	0,85	1.93

Table 1: GaAs MESFET transistor parameters

Figures (3) and (4) shows the variation of the potential *$V_l(x,y)$*, which result on the two dimensional analysis (Eq. (12)). Where the voltages *$V_l(0,hs)$* and *$V_l(L,hd)$* are plotted as a function of drain and gate bias .

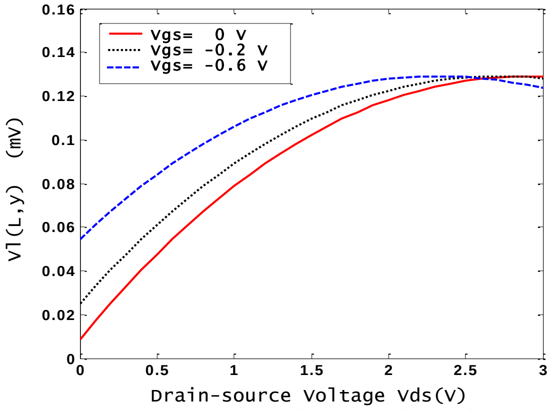

Figure 3: Variations *Vl(L,hd)* voltages according to drain bias

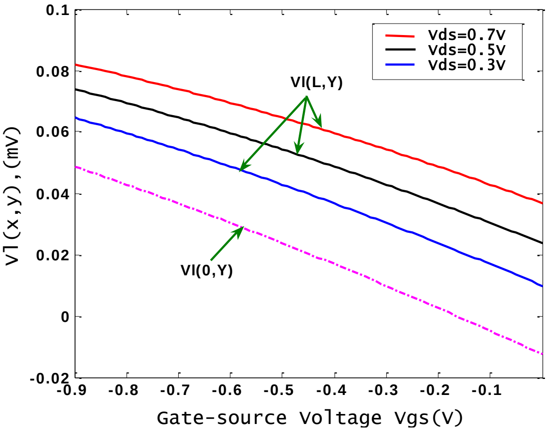

Figure 4: Variations *$V_l(0,hs)$ and $V_l(L,hd)$ voltages* according to gate bias

We noticed that the voltages *$V_l(0,hs)$* and *$V_l(L,hd)$* of the edge effects are found to be positive and both these quantities increases gradually as the absolute value of the gate voltage "*Vgs"* increases, and also with the increase of the voltage drain *"Vds"*.

For a long channel device, V_g controls the depleting semiconductor channel. However in short channel devices, part of channel depletion is under the control of source and drain bias. As the channel length shortens, the close proximity of the source and drain region occurs the fraction of the depletion charge in the channel. In other words, both the gate and source–drain voltages share control of the charge density below the gate. This effect is described by the figures (5), (6) and (7) were effects of *$V_l(0,hs)$* and *$V_l(L,hd)$* voltages on the drain current, transconductance and drain conductance of the GaAs MESFET are plotted with and without edge effects.

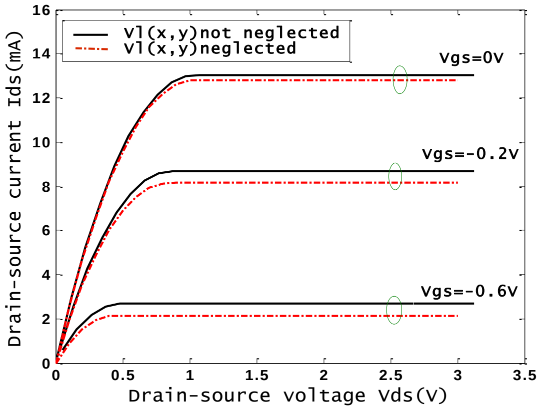

Figure 5: Variations I-V characteristics of the MESFET transistor

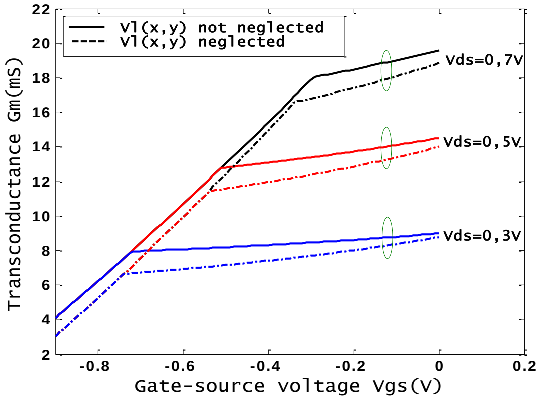

Figure 6 : Variation of the transconductance according to the gate voltage for the MESFET

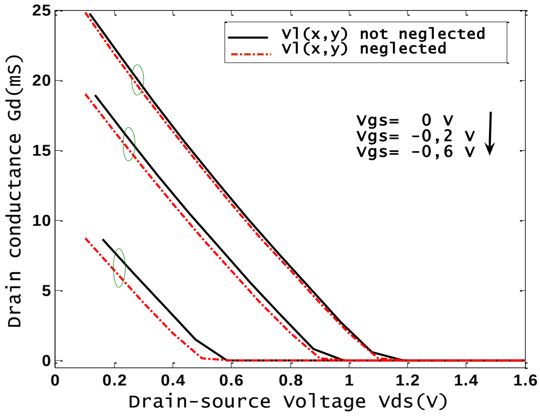

Figure 7: Variation of the conductance according to the drain voltage for the MESFET

Figure (5) shows a comparison between the drain current characteristics with and without edge effects. From the figure it is clear that edge effects $V_l(x,y)$ promotes the passage of more drain current. This is mainly due to the depletion region from the source and drain which are overlapped with the channel charge. In long channel devices, this part is negligible comparing with the area of effective device channel. However, in short channel device, this overlapped part cannot be neglected anymore and the previous approximation does not work. With the consideration of overlapped parts, the shape of the depletion charge cross-section can be described as shown in figure (1) and drain current can be calculated with expressions (20) et (22).

Such a functional dependence of the drain current suggests more involved relations for the drain conductance g_d and the transconductance g_m of the device. Like drain current, both g_d and g_m are also functions of edge effects. Figures (6) and (7) shows the changes in the values of drain conductance and transconductance caused by the voltages $V_l(0,hs)$ and $V_l(L,hd)$, that are relatively sharper with the increase of Vg and Vd .

VI. CONCLUSION

After we solved analytically the two-dimensional Poisson equation, we have presented the influences of edge effects on I-V characteristic, transconductance and drain conductance of the MESFET. When the depletion region extends at the drain side and source side, the depletion width is also affected by the edge effects. This has a direct influence on the characteristics of the transistor.

The simulation results are well presented and discussed, the corrective term $V_l(x,y)$ gives a real approximation for the potential distributions and depletion-layer form, that are used for the calculation of the short canal device characteristics .

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