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# STRUCTURAL PROPERTIES AND I-V, C-V CHARACTERISTIC FOR a-Ge:In/c-Si HETEROJUNCTION

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#### **ABSTRACT**

Ge:In films with thickness ( $1\mu m$ ) have been deposited by thermal evaporation technique on glass substrate and c-Si (111) wafer at room temperature, under vacuum of  $10^{-5}$  mbar with rate of deposition equal to 15 Å/sec. These films have been annealed at different temperatures (373, 473) K. The structural characteristic of the films prepared on glass substrates have been studied by using X-ray diffraction, the tests show that all the films have amorphous structure for all annealing temperatures. From C-V measurement of a-Ge:In/c-Si heterojunciton at frequency 10 KHz we found for built—in potential ( $V_{bi}$ ) the same value 0.48 V with  $T_a$  increasing from room temperature (RT) to 473 K. Also from I-V characteristic we found that the quality factor decreases from 3.01 to 2.19 for same annealing temperature, this may be interpreted in term improvement of crystal structure with heat treatment and reduction the defects state densities at interface layers of diodes.

**Key word:** Heterojunction, a-Ge doping.

# I. INTRODUCTION

In 1951, Shockley proposed the abrupt heterojunction (HJ) to be used as an efficient emitter-base junction in a bipolar transistor. Since then, heterojunctions have been extensively studied, and many important applications have been made, among them light emitter diode, photodetector, and solar cell [1]. The abrupt HJ are classified into two types, abrupt anisotype HJ and abrupt isotype HJ, Oldham and Milnes have constructed a model for HJ in which the effect of junction grading (i.e. continuous variation of energy gap and electron affinity through the transition region ) during fabrication has been included [2,3].

In the formation of a heterojunction with a narrow-bandgap material and a wide-bandgap material, the alignment of the bandgap energies is important in determining the characteristics of the junction [4].

Ge/Si abrupt heterojunction and the lattice parameter mismatch between Ge and Si is 4.2%. heteroepitaxial growth of Ge films on Si substrates is of high interest due to their potential

application in near-infrared photodetector or as high-mobility channels in FETs [5]. The growth of high-quality strain-relaxed thin Ge epilayers with smooth surface, low defect density, and thin buffer layers on Si substrates has attracted great attention due to its compatibility with Si process technology and the application in photonic and electronic devices. Ge epilayers on Si substrates can be used for fabrication of high-performance Si- based Ge photodetectors operating at long wave length of  $1.3-1.55~\mu m$ , high mobility metal-oxide-semiconductor field-effect transistors (MOSFETs) [6]. In this paper we study the structural properties and I-V, C-V characteristics for a-Ge:In/c-Si heterojunction.

#### II. EXPERIMENTAL PROCEDURE

a-Ge:In thin film were prepared by thermal evaporation technique in vacuum system supplied by Balzers model (BAE 370). For preparation of the heterojunction, thin film a-Ge:In were deposited on c-Si.

All samples were prepared under constant conditions (press, substrate temperature and rate of deposition), the main parameters that control the nature of the film properties are thickness (1 $\mu$ m) and annealing temperature ( $T_a$ ) (RT, 373, 473) K.

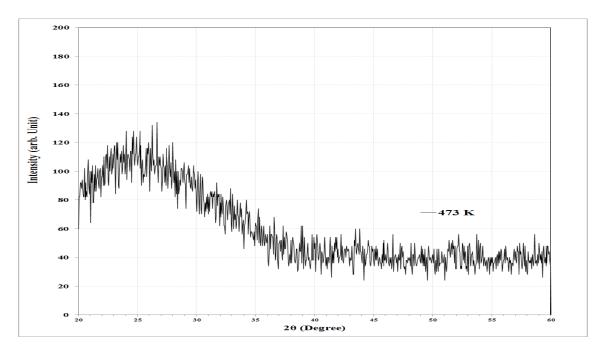
The capacitance of the heterojunction was measured as a function of the reverse bias voltage in the range (0-1) Volt with a fixed frequency of 10 KHz by using HP-R2C unit model 4274A multifrequency LCR meter.

Current voltage measurements were made for a-Ge:In/c-Si heterojunction when they were exposed to halogen lamp light Philips 120W and  $105 \text{ mW/cm}^2$  using Keithly digital electrometer 616, D.C power supply under forward and reverse bias voltage which was in the range (-1.5 V to 1.5 V).

### II. RESULTS AND DISCUSSION

The XRD results of Ge films prepared on glass at substrate temperatures equal to room temperature for different annealing temperatures (RT,373, 473) K are shown in figure (1).

We observed that Ge:In films are with amorphous structure. This result is in agreement with H.Howari [7], Kobayashi et al. [8], Ammar [9] and Akram [10].



**Figure 1:** X-ray diffraction of a-Ge:In films for different annealing temperatures.

Figure (2) shows C-V characteristic for a-Ge:In/c-Si heterojunction at reverse bias voltage (0-1) Volt and constant frequency 10 kHz for different annealing temperatures (303, 373 and 473) K.

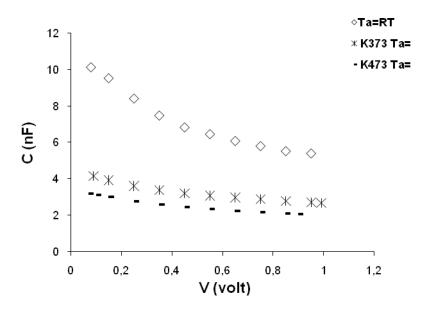
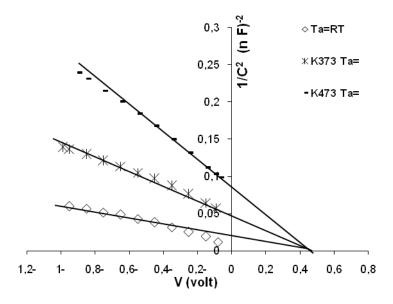


Figure 2: variation of capacitance versus reverse bias voltage for a-Ge:In/c-Si heterojunction at different annealing temperatures values  $T_a$ .

We can notice from this figure that the value of capacitance decreases with the increases of the reverse bias voltage and annealing temperature. This behavior is attributed to the increasing in the

depletion region width which leads to increase the value of built in potential. These results were in agreement with A.Shehab [11].

The value of built in potential can be found from the plots the relation between  $1/C^2$  and the reverse bias voltage. The interception of the straight line with the voltage axis represents the built in potential  $(V_{bi})$  as shown in Figure(3).



**Figure 3:** variation of 1/C<sup>2</sup> versus reverse bias voltage for a-Ge:In/c-Si heterojunction at different T<sub>a</sub>.

T <sub>a</sub> (K)	V <sub>bi</sub> (Volt)
303	0.48
373	0.48
473	0.48

Table 1: measured built in potential

We can see from table(1) and figure(3) the constant value of  $V_{bi}$  when annealing temperature change from (303-473) K. This means, that all discrete levels at energy gap values are filled [12].

Figure 4 shows I-V characteristic for a-Ge:In/c-Si heterojunction at forward and reverse bias voltage (-1.5-1.5) Volt for different annealing temperatures (303, 373, 473) K.

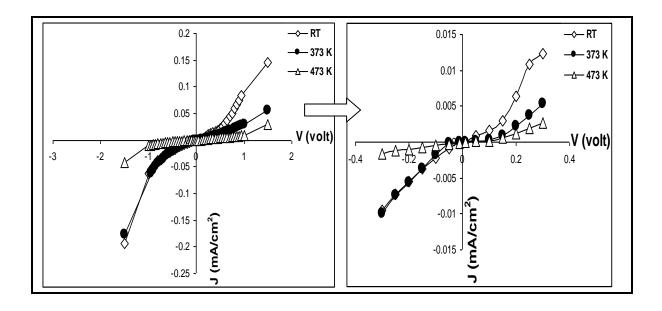


Figure 4: the current voltage characteristics in the dark at different annealing temperatures values (Ta)

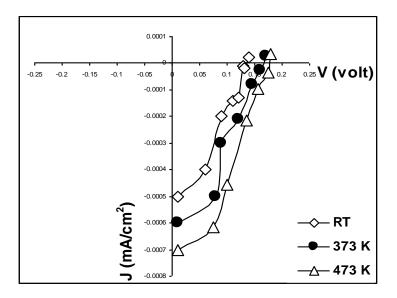
We observed that the current decreases slightly with increasing of annealing temperature.

$T_a(K)$	$J_{s}(\mu A)$	β
303	0.74	3.01
373	0.12	2.35
473	0.045	2.19

Table 2 experimental results

The variations of saturation current  $(J_s)$  and ideality factor  $(\beta)$  with different annealing temperatures are shown in Table (2). The data indicate that the values of the saturation current decrease with increasing annealing temperature.

This behavior attributed to the improvement of crystal structure at interface layer, also the reduction of dangling bonds and tails localized state in term density of state in a-Ge:In films.



**Figure 5:** I-V characteristics under illumination for a-Ge:In/c-Si heterojunction for thickness of 1  $\mu m$  at different annealing temperatures.

In another attempt we have studied the relation between the photocurrent density  $(J_{ph})$  and bias voltage of the a-Ge:In/c-Si diodes at different annealing temperatures. The measurement were carried out under incident power density equal to (105) mW/cm<sup>2</sup>.

In figure(5) all samples show a photocurrent density increases with increasing of the bias voltage and annealing temperature, this may be attributed to the increasing in the grain size and reducing the grain boundaries and improvement of structure which leads to increase the mobility and photocurrent densities. In general through looking at figure (5) we can notice that the short circuit current density ( $J_{sc}$ ) decreases together with the open circuit voltage ( $V_{oc}$ ). This parameter is very important because related to the region on which the heterojunction operates, and it can separate the generated pairs without the need to any apply external field.

The  $V_{oc}$  increases with increasing of annealing temperature is related to the reduction in defects and dislocation of interface states densities. This result is in agreement with and Abdul Razaq et al. [13].

# IV. CONCLUSION

a-Ge:In/c-Si heterojunction were prepared by thermal evaporation technique in vacuum system supplied by Blazers Model [BAE 370].

a-Ge/c-Si abrupt heterojunction. Heteroepitaxial growth of Ge films on Si substrates, the barrier high, saturation current and ideality factor which dependence on thickness and annealing temperature. The short circuit current density, open circuit voltage and fill factor which are controlled by the defect state density, lead to low efficiency of solar cell because of recombination centers. Ge epilayers on Si substrates can be used for fabrication of high-

performance Si- based Ge photodetectors operating at long wave length in the range (1.3-1.55) µm, high mobility metal-oxide-semiconductor field-effect transistors (MOSFETs).

We observed that the films have amorphous structure for all annealing temperatures using X-ray diffraction.

The C-V measurement of a-Ge:In/c-Si heterojunction shown the built-in potential ( $V_{bi}$ ) increase with increasing annealing temperatures. Also from I-V characteristic we found that the quality factor decreases with the increase of annealing temperature, this may be interpreted in term of improvement of the crystal structure with heat treatment.

Poor efficiency for solar cell and IR detector because of large density of states in mid-gap and high recombination centers that lead to excess of leakage current.

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