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ELECTRICAL PROPERTIES AND SCHEMATIC BAND DIAGRAMS OF Sn/PS/p-Si HETEROJUNCTION

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ABSTRACT
This paper presents a study of Sn/PS/p-Si heterojunction device which is fabricated by growing Sn thin film onto p-type porous Si substrate by using thermal evaporation deposition and electrochemical etching (ECE) in crystalline p-Si method. Effect etching current density on the morphology of the porous silicon surface is checked using atomic force microscopy AFM. Current–voltage (I–V), capacitance–voltage (C–V) characteristics. The ideality factor and series resistance are found to be large than the one (11.18 and 25 kΩ) respectively by the analysis of the dark I–V characteristics of Sn/PS/p-Si. While the analysis of the dark C–V, the built-in voltage and carrier's concentrations are found to be 0.59V and $1.1\times10^{17}cm^{-3}$ respectively. These characteristics are interpreted by assuming the abrupt heterojunction model from C-V measurement. The barrier height potential is measured by both I–V and C–V which is found to be 0.74eV. The Energy band diagram of heterojunction relevant by I-V and C-V measurements is sketched.
Keywords: porous silicon, electrochemical etching (ECE), Schottky Barrier, AFM

I. INTRODUCTION

The formation of PS (porous silicon) layers on crystalline Si (c-Si) wafers using electrochemical etching (ECE) exhibits photoluminescent and electroluminescent properties similar to those of semiconductors with direct energy gap [1].Porous silicon composites provide modified functionality comparing to as-prepared porous silicon and expand its applicability. Porous structure of the material and large internal surface imply high sensitivity of physical and chemical properties [2]. In all PS applications, information about the pore size and their distribution and surface chemistry and their dependence on the fabrication conditions plays decisive role. Correlation of observed physical properties with the morphology of PS films and the relationship between PS morphology and preparation parameters is necessary. Principal parameters controlling macro pore formation depend on the properties of silicon substrate (crystal orientation, doping), anodizing solution and temperature [3]. Porous silicon photoconductors are commonly fabricated by depositing aluminium film on top of oxidized porous silicon structure. The passivation of the surface by oxidation could improve the external quantum efficiency of porous silicon photodiode [4]. The morphology of porous silicon formed

by electrochemical etching of Si crystals was investigated by atomic force microscopy (AFM).Today, the nanoporous silicon is very interesting material for both its optical and electrical properties. Since the observation of strong room temperature visible photoluminescence from nanoporous silicon, there have been extensive researches to develop optoelectronics [5].

The practical applications are oriented towards the fabrication of new structures and devices. The compatibility of the nanocrystalline silicon-based materials with the classic mono- and/or polycrystalline silicon (bulk or thin films) permits the use of these new materials for the integrated micro- and optoelectronics, photonic crystals, biomedical applications or efficient sensors [6].When metal and semiconductor are in intimate contact because the work functions of both materials are different, built-in barrier is created at their interface, which is called Schottky barrier [7]. The barrier height is directly related to the difference in the Fermi levels between the metal and semiconductor material. The larger the difference is, the higher will be the barrier height is. The barrier opposes the flow of the free charge carriers from one side to another. The electrical behavior of M- S contacts is identified depending on the barrier height [7, 8].Schottky suggested that the rectifying behavior could arise from potential barrier as a result of the stable space charges in the semiconductor. This model is known as the Schottky Barrier (SB). Metal semiconductor devices can also show non-rectifying behavior; that is, the contact has negligible resistance regardless of the polarity of the applied voltage. Such a contact is called an ohmic contact. The C-V characteristic of heterojunction is one of the most important measurements since it determines different parameters such as built-in potential, junction capacitance and junction type.In this work, Sn films were deposited onto porous layer /Si wafers by thermal evaporation to form rectifying junctions. The electrical properties of the junctions were determined by current-voltage (I-V) and capacitance-voltage (C-V) measurements.

II. EXPERIMENT

Several methods are developed to make the porous layer with wide variation of pore morphologies having the pore dimensions from micro to nanometers. In most cases, the porous silicon structure is formed by electrochemical etching of Si wafers in electrolytes including hydrofluoric acid (HF) and methanol. Figure 1 illustrates the Cross-sectional view of lateral anodization cell used to fabricate the porous layer reported here. PS layers were prepared by the anodization of (111) oriented, p-type silicon substrates in 1:1 solution of hydrofluoric acid HF (40%) and methanol at current density of 33 mA/cm^2 for 11 min in the dark as shown in same figure. The substrate material p-type silicon wafers with resistivity of 11-16 Ω.cm corresponding with doping density of $\mathbf{2.75 \times 10^{14} - 2.94 \times 10^{14}\ cm^{-3}}$.

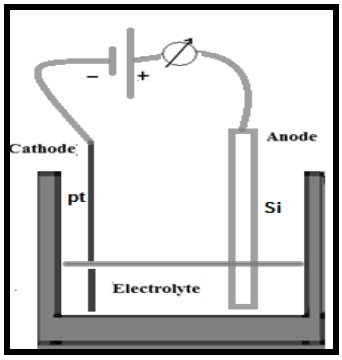

Figure 1: Cross-sectional view of lateral anodization cell.

Before anodization, Ohmic contacts were deposited on the backside of the wafers by Al evaporation followed by oxidization in air at 300℃ for 30 min. Following anodization, rinsed in distilled water treated ultrasonically followed by drying in hot air stream. Metallization on PS has also become another important area of interest, especially in the Schottky diode structure. The evaporation is performed in vacuum pressure of 10^{-6} torr, using an evaporation plant model "E306 A manufactured by Edwards high vacuum". After the evaporation process, the thickness of evaporated film on glass substrate is measured using gravimetric method. To ensure as uniform current distribution as possible, the samples are coated with thick layer of aluminum on the backside. The samples are prepared in sandwich configuration, top Sn/PS/c-Si/bottom Al, the top one (Sn) semi-transparent electrode thermally evaporated thin layer .The rear-side ohmic contacts were fabricated by the electro-chemical deposition of thick Al film to get sandwich structure as shown in cross section of Sn/PS/p-Si/Al of figure 2. Dark current – voltage in forward and reverse directions Sn/PS/c-Si/Al measurements are carried out by applying voltage supplied to the sample from stabilized d. c. Power supply, type LONG WEI DC PS-305D 30 ranges (-10 to +10) V. The current passing through the device is measured using UNI-T UT61E Digital Multimeters. The measurement is done under light of different illumination power densities supplied by Halogen lamp 150W which is connected to variance and calibrated by power meter. Capacitance-Voltage characteristics of the Sn/PS/c-Si HJ heterojunction are measured using a LCZ meter at room temperature. The C-V measurements at reverse bias voltage range from (2-10) V at 200 kHz.

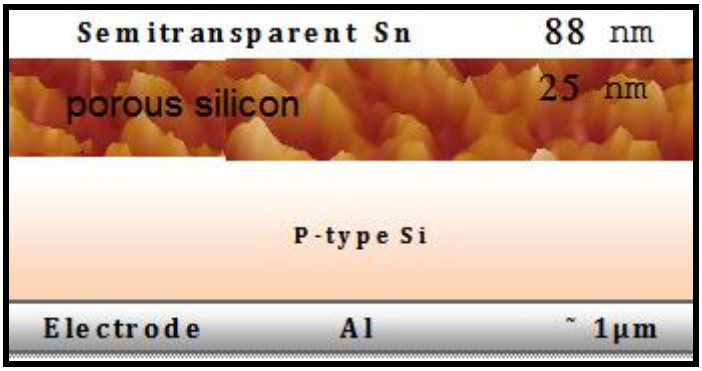

Figure 2: Cross-sectional view of Sn/PS/p-Si/Al metal semiconductor metal structure.

III. RESULTS AND DISCUSSION

Atomic force microscope images of freshly prepared porous silicon two and three dimension were shown in Figure 3. The irregular and randomly distributed nano-crystalline silicon pillars and voids over the entire surface can be seen in 3D AFM image. Also shows the surface roughness and pyramid like hillocks with un-uniform different heights surface. The scanning area used, is 5μm ×5μm. The RMS surface roughness is 3.34 nm. Sz (ten points height) 25.7 nm, roughness average 2.08nm.

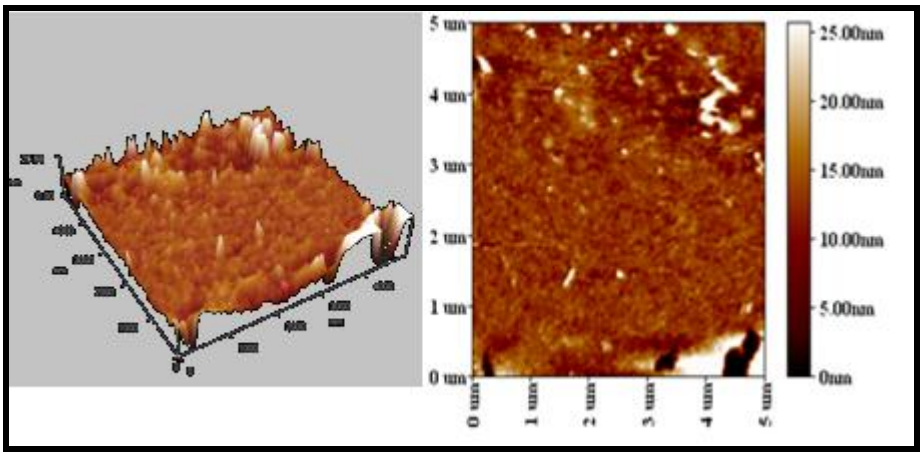

Figure 3: 2D and 3D AFM image of porous silicon prepared at 33 mA/cm^2 etched current density and 11min etching time.

IV. DARK CURRENT-VOLTAGE MEASUREMENTS:

Dc measurements were made in the dark of Sn/PS/p-Si/Al structures at room temperature. Figure 4 shows the I-V characteristics of the heterojunction Sn/PS in the range −10 to +10 V in a semi log plot at 33mA/cm^2 etching current density and 11min etching time. I-V characteristic of the heterostructure, Sn/PS/c-Si, is shown in Figure 4. I–V characteristics can be described by the thermionic emission model [9] and the equation, which describes the current as a function of the applied voltage of the junction can be expressed as [10]:

$$\mathbf{I_o = I_s[exp\left(\frac{qV}{nKT}\right) - 1]} \quad (1)$$

here, I_o is the reverse saturation current and is given as:

$$\mathbf{I_s = A^* T^2 exp\left(\frac{-q\emptyset_B}{nKT}\right)} \quad (2)$$

Where $\mathbf{A^*}$ Richardson constant, n the value of ideality factor, V is the applied voltage and T is the temperature in Kelvin. The barrier height and ideality factor of Sn/PS surface type Schottky diode is calculated from the current-voltage characteristics by using the following equation [11]:

$$\mathbf{\emptyset_B = \frac{kT}{q} ln\left(\frac{AA^* T^2}{I_s}\right)} \quad (3)$$

$$\mathbf{n = \frac{q}{KT}\left(\frac{dV}{d\,ln I}\right)}. \quad (4)$$

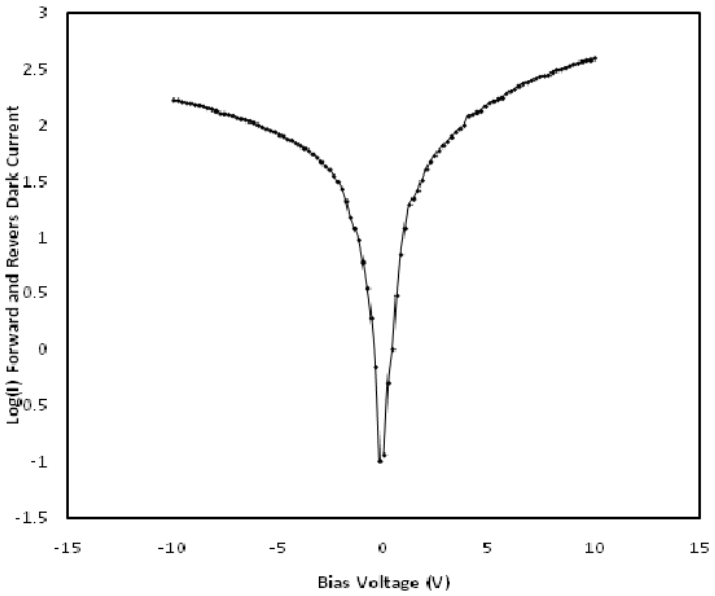

Figure 4: log (I) –V curves of a Sn/PS/n-Si/Al structure.

I-V characteristics give information about the junction properties such as rectification factor (R_f), Ideality factor (n), Series resistance (r_s) and Saturation current (I_s). The electrical parameters of the heterojunction Sn/PS/n-Si/Al is presented in table (1). These parameter were obtained from dark (I-V) characteristics. The experimental data presented in Figure 4 were fitted with a simple diode model [12]. Rectification factor which represented the ratio of the forward current to the reverse current at a certain applied voltage calculated .The junction Sn/PS/p-Si exhibits rectifying characteristics showing diode-like behavior of rectification factor was 3.6 at ∓ 1 V.

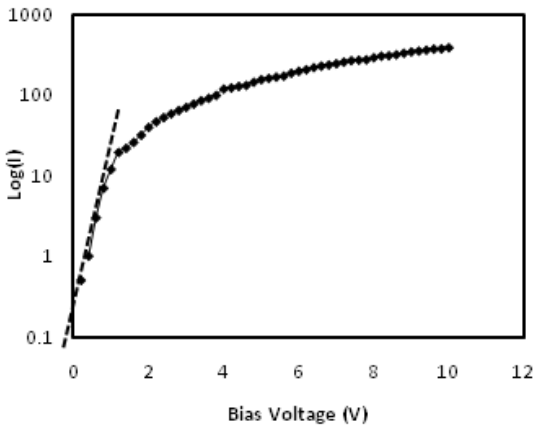

Figure 5: log (I) - V measurement.

The reverse saturation current, barrier height and ideality factor of the diode can be determined from the forward-biased characteristic in figure 5, and have been calculated using equations (3 and 4). It has been found that the reverse saturation current ($\mathbf{I_s}$), barrier height ($\mathbf{\emptyset_B}$) and ideality factor of Sn/PS/p-Si junction is 1.12 µA, 0.74 eV and 11.8 respectively. Increasing saturation etching current is due to the effect of the interface layer between PS/n-Si has large amount of pinning, which acts as a defect in the interface and lead to increase saturation etching

current density and hence to decreasing the barrier height of PS [12].When the structure has a series resistance and interface states, ideality factor (n) becomes higher than unity as showing in the table (1); most practical Schottky diodes shows deviation from the ideal thermionic theory. The fact that such recombination currents are flowing not homogeneously in the structure. The high ideality factor can be attributed to the sum of the ideality factors of the individual rectifying junctions (i.e., the actual PS/c-Si heterojunction junction and Schottky diodes at the Sn/PS or the two metal-semiconductor junctions (Sn/PS, c-Si/Al) of a diode ideally have Ohmic characteristics) [13, 14] The nature of porous silicon implies a very large effective surface area, and consequently, a large concentration of dangling bonds. Porous layers act as series resistance in Sn/PS/c-Si/Al structure, so we have a large value of dynamic (series) resistance (see table 1).

Table 1: Values obtained from I-V measurements

Rectification factor (R_f)	**Ideality factor (n)**	**Series resistances (r_s) kΩ**	**Saturation current (I_s) μA**	**Barrier potential ($\emptyset_B$) eV**
3.67	**11.18**	**25**	**1.12**	**0.74**

IV.1 Dark capacitance-voltage measurements:

It is known that a capacitance of a Schottky diode can be represented by the relation between voltage and capacitance which expressed as a standard Mott−Schottky relationship [15]:

$$\frac{1}{C^2} = \frac{2(V_{bi} - V_i)}{q\varepsilon_s\varepsilon_o N_d A^2} \qquad (5)$$

The plots of C^{-2} versus V is linear which indicates the formation of Schottky junction where C is the diode capacitance, V_{bi} is the built in voltage, ε_s is the semiconductor dielectric constant, ε_o is the permittivity in vacuum, V_i is the applied voltage, q is the charge, A is the diode active area, and N_d is the charge carrier concentration. By plotting C^{-2}versus V as shown in figure 5 and applying Equation **5**, a straight line is obtained, the slope gives the free carrier concentration N_c and it was found to be $1.1 \times 10^{17}\ cm^{-3}$ by applying the relation:

$$slope = \frac{2}{A^2 N_c \varepsilon_s q} = \frac{V_{bi}}{c^2} \qquad (6)$$

Also, the intercept at $C^{-2} = 0$ gives the built-in-voltage V_{bi} by linear fitting as shown in figure 6 The capacitance of the Sn/PS/p-Si heterojunction was measured at a low frequency of 200 kHz in dark and at room temperature as shown in left inset of figure 6 the junction capacitance is inversely proportional to the bias voltage. There was a decrease in the capacitance at bias.

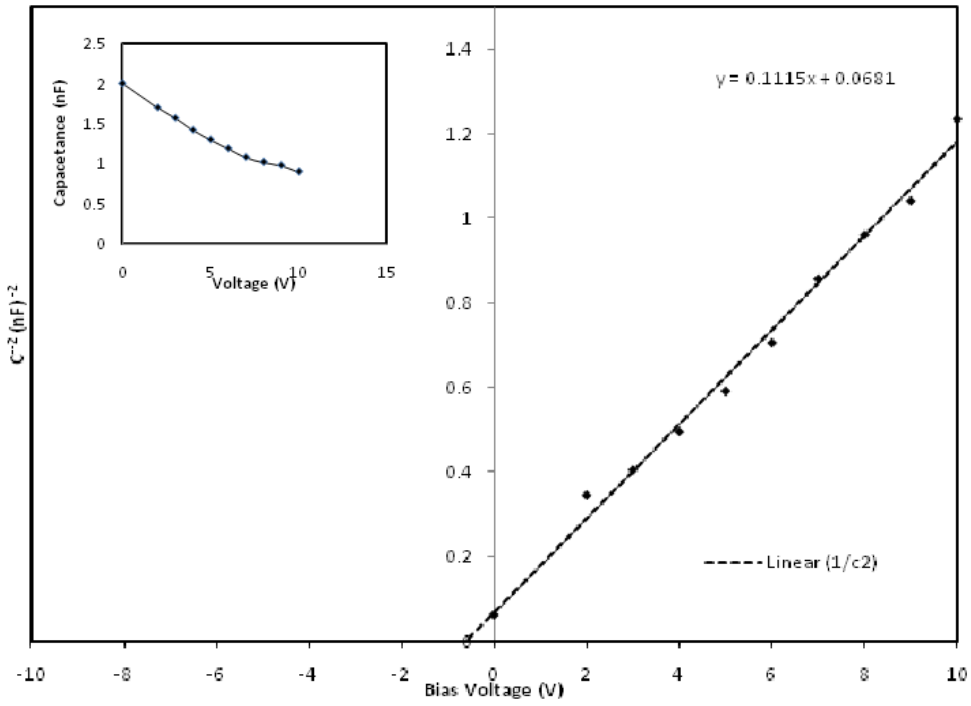

Figure 6: $\mathbf{C^{-2}}$ of Sn/ PS/p-Si/Al structure vs. the applied voltage and left inset of figure the Junction capacitance of Sn/PS/p-Si/Al structure vs. the applied voltage.

The value of barrier height can be obtained by using following relation []:

$$\emptyset_B = V_{bi} + \frac{kT}{q} \ln\left(\frac{N_c}{N_A}\right) \quad (7)$$

where, N_A is the accepter concentration, V_{bi} is built in potential and $N_c$is the effective density of states in the conduction band of silicon N_c is calculated from the slope of $C^{-2} - V$ plot as shown in table (2).

Table 2: Values obtained from C-V measurements

Effective carrier density $N_c cm^{-3}$	Built in voltage V_{bi} (V)	Capacitance Co (nF)	barrier height $\emptyset_B$(eV)
1.1E+17	0.59	2.31	0.743

As observed from the figure **6**, $C^{-2} - V$ variation is linear in the voltage range studied indicating that the junction is of abrupt nature. That means the carrier concentration will be constant at the depletion layer [16]. That means the carrier concentration will be constant at the depletion layer. The reduction in the junction capacitance with increasing the bias voltage results from the expansion of depletion layer with the built-in potential. The linearity of this dependence indicates that the junction is reasonably interpreted by assuming that an abrupt

heterojunction, this property give an indication of the behavior of the charge transition from the donor to the acceptor region, that mean the depletion layer is constant

The thickness of the surface space-charge region W can be given by:

$$\mathbf{W} = \sqrt{\frac{2\varepsilon_s V_{bi}}{q N_A}} \qquad (8)$$

where $\boldsymbol{\varepsilon_s}$ is the relative dielectric constant, $\mathbf{q}$ is the elementary charge, $\mathbf{V_{bi}}$ is the built in voltage at the surface see Figure 6 and $\mathbf{N_A}$ is the concentration. We obtain W=15 nm Therefore, any change in the concentration $\mathbf{N_A}$ will change the depletion layer width

IV.2 Energy gap of porous silicon:

The photosensitivity of the photodetector is investigated in the wavelength with the aid of Joban-Yvon monochromatic and standard Si power meter. The value of energy gap is determined by the photoresponse spectrum curve between photocurrent and energy of quanta of the incident light. In the case of nano- or micro-porous silicones, quantum confinement causes spatial fluctuations of the effective band gap as can be seen in Figure 7, so as [17, 18] reported that the porous layer behaves as wide band semiconductor sensitive to the visible light. The photoelectrical method of definition of effective band gap in the vicinity of PS/c-Si heterojunction is proposed. As it is known the width of the band gap of crystal silicon is 1.12 eV. The enhancing of band gap in PS is connected with quantum-size effect. The main quantum confinement effect is represented by the appearance of new energy levels in the silicon band gap. Band diagram of Sn/PS/p-Si/Al heterojunction using Anderson model indicated in figure 8.

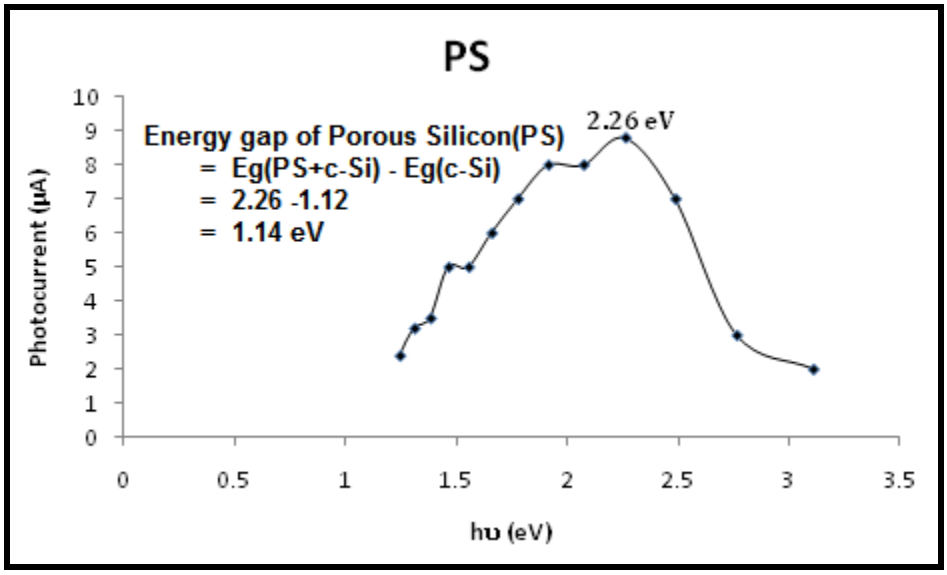

Figure 7: The spectrum of photocurrent of Sn/PS/p-Si/Al structure vs. incident photon energy.

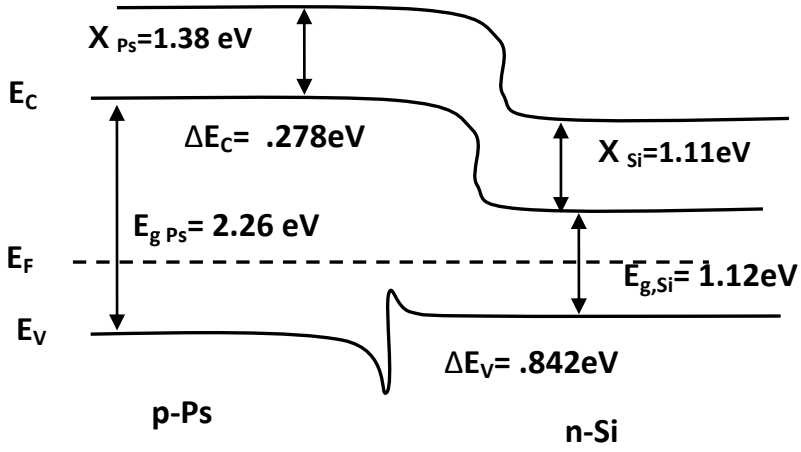

Figure 8: Band diagram of Sn/PS/p-Si/Al heterojunction

V. CONCLUSIONS

In this work the preparation of nanocrystalline porous silicon (PS) by electrochemical anodization has been described .Morphology and electrical properties of porous silicon have been mentioned. Sn was chosen as the top semitransparent metal electrode to fabricate the Sn/PS/p-Si/Al photodetector heterojunction structure. The junctions were characterized by I-V and C-V studies and were confirmed to behave as Schottky devices. No difference is observable between the values of barrier height calculated by I-V or obtained from C-V measurement.

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