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ANALYSIS OF GIDL AND IMPACT IONIZATION WRITING METHODS IN 100nm SOI Z-DRAM

Bhuwan Chandra Joshi, S. Intekhab Amin and R. K. Sarin

Department of Electronics and Communication, National Institute of Technology Jalandhar, India

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ABSTRACT

A capacitorless dynamic random access memory (DRAM) is very useful for large scale integrated DRAM having high performance. In this paper the comparison between GIDL and Impact Ionization (II) writing techniques in terms of power consumption and sensing margin in 100nm gate length capacitorless 1T DRAM has been done. GIDL improves power consumption and sensing margin in comparison to impact ionization writing method. But beyond 100nm as device size is scaled down, drain current of the device increases due to reduction in threshold voltage of the device. GIDL is not so beneficial in terms of power consumption at this scaling because drain current is normally high. Although change in substrate doping directly impacts the value of drain current. There is a narrow range of substrate doping at which GIDL proves to be beneficial in terms of power consumption.

Keywords: DRAM, capacitorless, GIDL, impact ionization, low power consumption.

I. INTRODUCTION

There are mainly two kinds of memories, embedded static random access memory and embedded dynamic random access memory. Static random access memory (SRAM) mainly is used in high speed applications but it comprises of six transistors. Whereas a conventional dynamic random access memory (DRAM) cell uses 1transistor/1capacitor (1T/1C). Due to this reason it is not as dense as DRAM. The advantage of DRAM is simplicity in its structure. DRAM requires only a capacitor and one transistor. This allows DRAM to achieve very high packaging density. The DRAM industry has ability to accommodate more and more memory bits per unit area in silicon die [1-7]. But the scaling of the conventional 1T/1C DRAM is becoming difficult in sub-nanometer range, in particular due to the capacitor which is harder to scale [2].This is due to the fact that there should be minimum size of capacitor (around 30fF/cell) to store the signals with good noise immunity [1]. Recently the capacitorless single transistor (1T) DRAMs (Z-DRAM) have attracted attention due to the lack of the capacitor having problems associated with the scaling [1][8]. Since capacitor is absent so has the ability to achieve higher device density. The information is stored at a capacitor in conventional 1T/1C DRAM whereas the 1T Z-DRAM employs floating body effects within the transistor to store the information without the need of an extra external capacitor. The absence of the capacitor is advantageous in terms of scalability, complexity of process and fabrication, compatibility with the logic processing steps, device density which improves yield and cost. Due to all these advantages of capacitorless DRAM and also to solve the scaling problem of conventional DRAM, it has become a very attractive option for conventional DRAM replacements [3]. This paper compares the results of power consumption and sensing margin using II and GIDL technique for writing '1' data in Z-DRAM.

II. MECHANISM OF MEMORY OPERATION USING IMPACT IONIZATION CURRENT

One of the methods to write the data in floating body DRAM is impact ionization. Impact ionization process occurs in drain body junction. A positive drain voltage V_D is applied which is shown in Figure 2(b), to create a positive body charge by breaking covalent bonds (impact ionization) and the body voltage charge reduces the threshold voltage of the device which results in increasing the drain current I_d ('1'state). During writing the drain voltage V_D must be high enough (V_D>V_{G1}) in order to form the pinch-off region where the hole–electron pairs are generated. Since V_{G1}>V_{TH1}, the power consumption during the body charging is substantial [4]. During write '1', the majority carriers are initially injected from drain or pinch-off region towards the quasi-neutral zone (by applying a

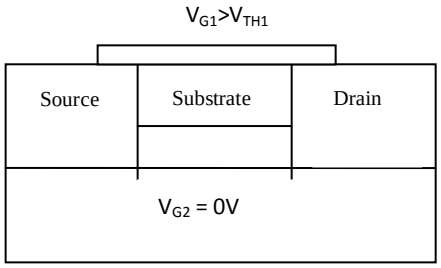

Fig. 1: Schematic of NMOS using as Z-RAM

positive drain voltage V_D). The body potential increases from its equilibrium value. There is a probability of discharging the storage charge in the body. Due to storage of holes, body potential move towards positive value and source is at ground which makes body source junction forward bias resulting stored charge to move toward source area and recombine there. There is also a probability of storage holes to recombine in the body. So the proper bias conditions are required to slow down the body discharging [4]. For reading data '1', drain to source voltage should be such that the device will operate in linear region. The biasing for reading data will be $V_{GS}>V_{TH}$ and $V_{DS}<V_{GS}$ [4].

III. MECHANISM OF MEMORY WRITE '1' OPERATION USING GIDL CURRENT

The gate-induced drain leakage (GIDL) effect is used to modify the floating body charge by applying negative front gate and positive voltage pulses at drain [4].

Figure 2(a) shows the required biasing voltages for occurring GIDL phenomenon. For GIDL to happen gate voltage should be negative and drain voltage should be positive. If we apply a more negative gate voltage then writing speed of device will increase. This is because the GIDL current depends on voltage difference between the gate and the drain. The large lateral electric field is produced due to negative voltage applied at gate which increases band to band tunneling current. In GIDL writing process the number of holes stored at floating body is small in comparison to II writing process. This means the modified equilibrium body potential will be less in GIDL process with comparison to II which will increase the write '1' hold time. The power consumption of the write '1' operation can be reduced significantly if GIDL current is used instead of impact ionization current [5]. For obtaining same writing speed in GIDL and II process gate voltage applied in GIDL process will be higher than that for

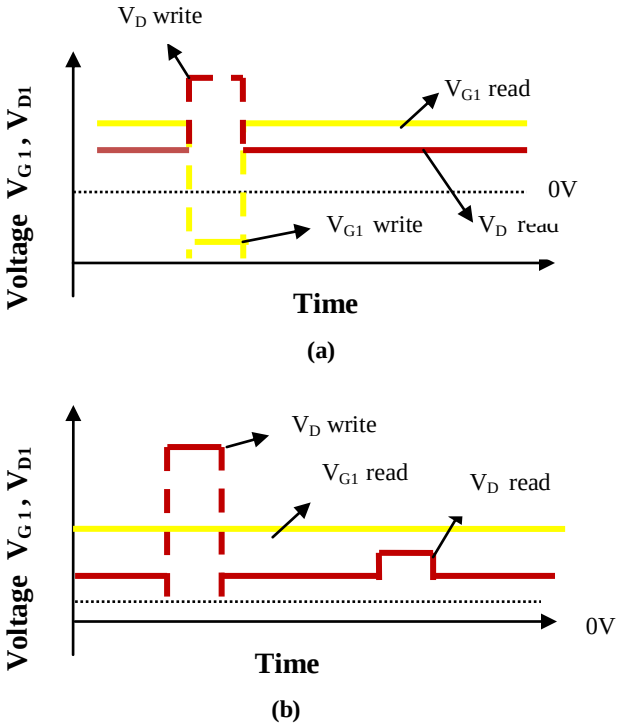

Fig. 2: (a) Applying voltages sequence in GIDL for the write/read '1'-state (Z-RAM) (b) Applying voltages sequence in Impact Ionization for the write/read '1'-state (Z-RAM) II process [5].

IV. DEVICE STRUCTURE AND SIMULATION CONDITIONS

Figure 3 shows schematic of SOI 1T DRAM. Substrate doping of 10^{18}/c.m3 is used [6]. The dimensions of device are shown in Table 1.Front gate oxide thickness (T_{FO})=4nm, thickness of substrate on insulator (T_{SOI})=45nm, thickness of back oxide (T_{BO})=8nm and channel length (L_{GATE})=100nm [6]. Figure 4 shows the graph between drain current and gate to source voltage at V_{DS} =1.2V. During write '1' condition generated charges are stored in the body and due to storage of charge threshold voltage of device will reduce which leads to the increasing value of drain current. This shows storing '1' data. Removal of stored charge from body will increase the threshold voltage of device resulting in decrement the value of drain current. The difference in the drain current between blue and red graph shows excess and deficit of charge carriers in floating body respectively. Figure 5 shows write and read current waveform and required biasing voltages have shown in Table 2.

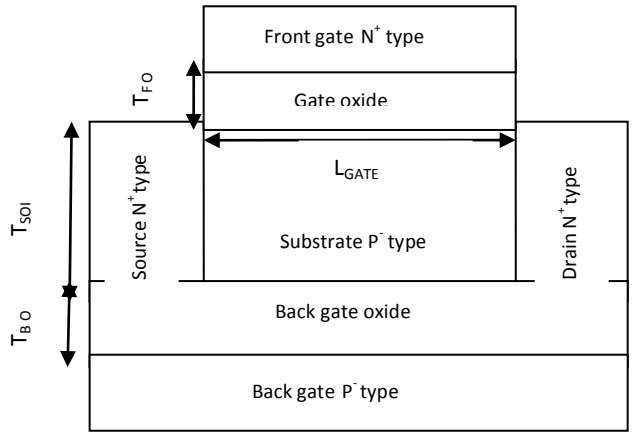

Fig. 3: Schematic of SOI 1T DRAM

Table 1: Dimensions of 100nm SOI 1T DRAM

Parameter	SOI 1T DRAM
T_{FO} (nm)	4
T_{BO} (nm)	8
T_{SOI} (nm)	45
L_{GATE} (nm)	100
N_{SOI} (cm^{-3})	10^{18}

During write'1' operation the drain current obtained is 299µA/µm but during read '1' the value is 50µA/µm. This is due to recombination of stored charge carries in floating body by forward biasing body source junction. Hold time is 10ns. At writing data '1' the biasing voltages are 1.2 V at gate, ground at source, 1.2V at drain and -0.5 at substrate. The drain current obtained is approximately 299µA/µm. During read data '1' the required biasing voltages are 0.6V at gate, ground at source, 1.2V at drain and -0.5V at substrate. The value of drain current obtained is 50µA/µm. The reduction in value of current is due to reduction in stored charges during hold time. If hold time is further increased then it may be possible the value of drain current during read '1' further reduces. Actually hold time is directly related to device retention time. During write '0' biasing voltages are 0.6V at gate, ground at source, 1.2V at drain and -0.5V at substrate. The value of drain current in this case is approximately -550 µA/µm.

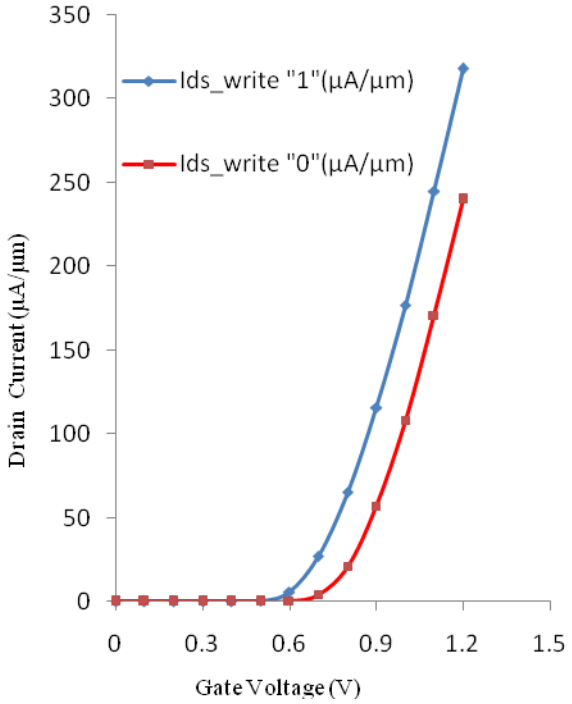

Fig.4: I_D/V_{GS} Characterstics with V_{DS}=1.2V

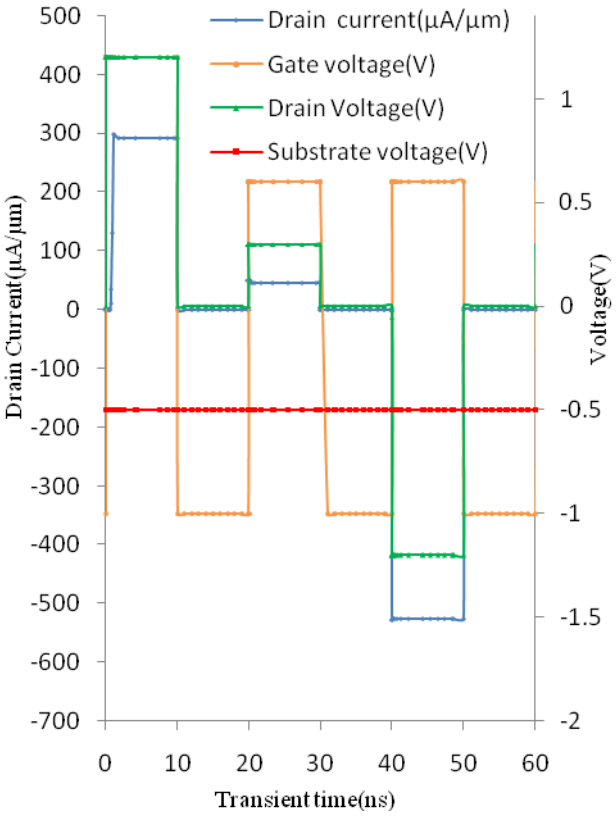

Fig.5: 100nm floating body DRAM reading and writing operation

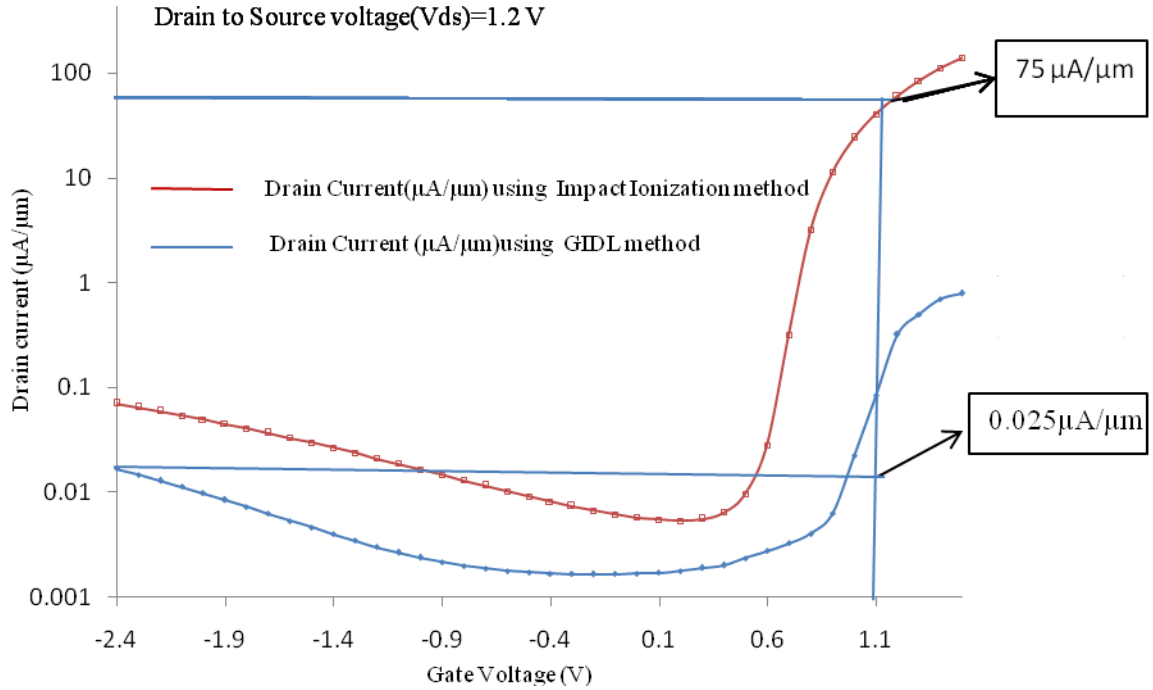

Fig.6: Dependence of drain current and body current on gate voltage.

Table 2: Operating voltages of 100nm SOI 1T DRAM

Electrode	Program	Erase	Hold	Read
Gate	1.2	0.6	-1.0	0.6
Source	0.0	0.0	0.0	0.0
Drain	1.2	1.2	1.2	1.2
Substrate	-0.5	-0.5	-0.5	-0.5

V. POWER CONSUMPTION

By using the II and GIDL method for writing '1' data the power consumption is lowered in case of GIDL in comparison to II. Current obtained in case of II is 75µA/µm and in case of GIDL is 0.025 µA/µm which have shown in Figure 6. Power consumption is calculated by taking product of drain current and drain voltage. The value of power consumption has shown in Table 3. While comparing the power consumption the writing speed of floating body DRAM using GIDL and II should be same in nanosecond range. For this drain source voltage =1.2 V is applied for both cases.

Table 3: Drain current and power consumption in 100 nm SOI1T DRAM using II and GIDL

	Drain current	Power consumption
I.I	75 µA/µm	$1.2*10^{-6}$ W
GIDL	0.025 µA/µm	$0.03*10^{-6}$ W

VI. SENSING MARGIN

Sensing margin defines the drain current difference between '0' state and '1' state during reading. When GIDL writing condition is used sensing margin will improve in comparison to II. This improves noise immunity. Actually drain current difference depends on threshold voltage difference of device and threshold voltage difference further depends on floating body potential. Figure 7 shows comparison of body potential while either GIDL or II writing method is used. Device parameters used for simulation are as follows. t_{ox} =4nm, t_{soi} = 45nm, t_{box} = 8nm, L_{gate} =100nm, N_{soi} = 10^{18}/c.m^3. The simulation was performed using two dimensional device simulator ATLAS.

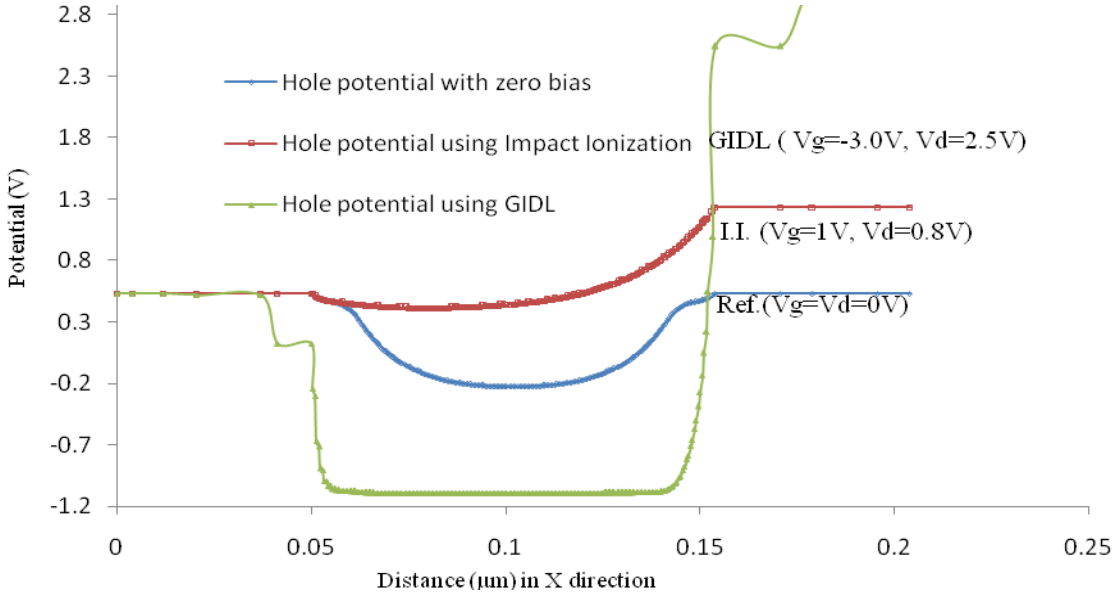

Fig. 7 Hole potential immediately after write '1' voltage is applied

Figure 7 shows the simulated results of the hole potential in cases where either GIDL or II is used just after application of write'1' voltages. In order to compare both writing method under same writing speed the gate and drain voltage should be selected such that same body current will flow. For a GIDL case drain voltage = 2.5V and gate voltage = -3.0 V is used. For the case gate voltage = 1V and drain voltage = 0.8V is used. For the GIDL case body potential become negatively large because of the capacitive coupling between gate and body. This body potential will lead to an increase in accumulated holes because barrier height between body and source is higher than that for II case.

VII. CONCLUSION

In this paper two different writing methods (II and GIDL) for 1T DRAM have been analyzed. It is found that using GIDL instead of Impact Ionization improves the power consumption. At constant drain to source voltage (V_{DS}) =1.2 V, the current obtained is 75µA/µm in case of II and 0.025µA/µm in case of GIDL. This difference in drain current will led to power consumption difference. Simulation result in figure 7 shows that sensing margin also improves in case of using GIDL writing method instead of Impact Ionization. Sensing margin is actually the difference between write '1' and read '1' current.. This difference depends on threshold voltage difference. This voltage difference further depends on storage of charge carriers in floating body. In case of GIDL the number of storage of charge carriers are large in amount in comparison to the II. Simulated results of hole potential proves that argument. So sense margin has large value which directly shows higher noise immunity [5]. Finally it is concluded that while using GIDL for writing data '1' improves power consumption and sensing margin in comparison to II writing method. GIDL writing method proves beneficial in terms of power consumption upto 100nm**.** But beyond 100nm as device size is scaled down, threshold voltage of the device reduces and drain current of device increases i.e. drain current will normally high at this scaling. So GIDL writing method will not be so effective at this scaling. Although drain current can be varied by changing the substrate doping i.e. there will be narrow range of substrate doping at which GIDL writing method proves beneficial in terms of power consumption.

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