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FAST AND SLOW-STATE TRAPS AT THE MOSFET OXIDE INTERFACE WITH A TEMPERATURE DEPENDENT C-V METHOD.

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Abstract: The present experiments are intended to characterize defects in very thin MOS oxide at its Si/SiO_2 interface using temperature-dependent electrical C (V) measurements. This method is shown to be useful in analyzing the correlation between slow and fast state traps. It has an original insight for hightemperature-activated processes and also the advantage of cryogenic temperatures to investigate defect properties. In this work, fast-state and slow-state trap cross-sections are calculated and their temperature activated relationship elucidated for oxide thickness as thin as 5.4 nm.

KEYWORDS: MOSFET transistor, C-V characteristics, hysteresis , defects, slow-state and fast state traps, TDCV.

1. Introduction

High-Low Frequency Capacitance Voltage (HLFCV) or Charge-Pumping techniques are classical C(V) measurement techniques used by many researchers today to measure the density of interface traps D_{it} in metal-oxide-semiconductor (MOS) devices [1-6], including high-oxide-field stressing experiment at 78K [7]. Derived to these techniques, we have developed [9] a new Temperature Dependent C-V method (TDCV), which is easy to perform and its implementation requires widely available high-frequency capacitance-voltage (C-V) instrumentation. For this method, voltage shifts obtained along an hysteresis cycle are measured and lead to the determination of interface traps densities. It has been shown useful to differentiate slow interface states compared to

typical fast interface states.

Such studies are of importance since interface states induced device degradation processes, which appear in thin oxide caused by high electric fields. In this paper, we discuss the kinetics process from measurements as a function of temperature and of current injection densities in the oxide from the gate.

2. Experiments

Samples are conventional process MOSFET structures with poly-Si gates. The Boron concentration in the substrate ranges from $5x10^{16}$ cm^{-3} to $1x10^{17}$ cm^{-3}. The channel length is 200 and the gate area is $4x10^{-4}$ cm^2. The gate oxide was C and post-annealed at 900 C for 90 min. SiO_2 <100> Oxide thicknesses are 5.4 and 9.4 nm. The post-metallization annealing was performed at 420 C for 20 min in H_2/N_2 = 10%. Toyota Central Laboratory, Aichi, Japan provided all these samples.

Fowler Nordheim (FN) stress was applied at temperatures of 77 K, 300 K, 400 K, 450 K, and 500 K, through a constant current intensity of $2x10^{7}$ A, a total charge of 0.5 C/cm^2 was injected during 1000s and high temperature stresses can then create heavy damage to MOSFET structures. Stronger stress conditions (1 C/cm^2, for example), or shorter injection times, are difficult to apply since they led to oxide breakdown for temperatures higher than 400 K in our experiments.

In this high/low temperature C(V) method, the measurements are performed at a temperature as low as 77 K. The sample is then warmed up to various temperatures being kept in the deep depletion mode where the depletion layer is at its largest. By this process, thermal energy generates carrier injection and results in an inversion regime. Minority carriers remain sufficiently trapped by defects, so it is possible to distinguish between fast-state traps and slow-state traps, and also, between negative charge, positive charge and hydrogen species. In this work, injecting at different temperatures, we have investigated the creation mechanisms of fast and slow-state defects. A general mechanism for slow-state traps is then proposed by chemical equation governing water migration in various kinds of oxides.

3. Slow and fast-state defect relationship

Figure 1 shows that fast-state trap densities increase drastically as stress temperature does. The injection of charge at high temperatures generates more fast-state trap defects than at room and low temperatures. Such fast-state traps densities are very high: $7.4x10^{11}$ cm^{-2} at 500 K, $4.5x10^{11}$ cm^{-2} at 450 K, and the density at 500 K is about seven times higher than the density found after room temperature stress injection. Figure 2 displays the effect of the injection level on the trap densities.

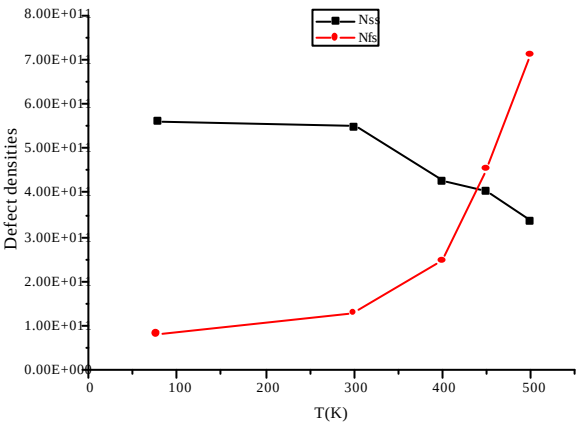
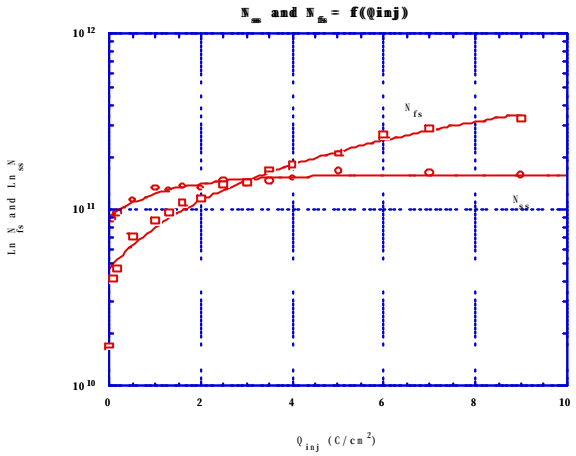


Fig 1: Degradation level for slow-state and fast-state trap injection temperature injection from 77 K to



As fast-state trap density (N_{fs}) increases with injection temperature, simultaneously, slow-state trap density (N_{ss}) decreases. This is an original result that leads to differentiate slow-state traps that are not distinguished from oxide-fixed trap. A slow-state trap can be taken not only as an oxide trap but alsoas an interface trap. In this case, the capture and emission kinetics of individual Si/SiO_2 interface traps, described by Shockley Read Hall (SRH) statistics and recombination-generation kinetics can be extended to slow-state traps [9]. And then, we can model a trap in the oxide by an energy level in the SiO_2 band-gap as a fast-state trap is represented by an energy level in the Si band-gap. This is a simple extension of interface state emission/capture equation for each individual slow-state trap:

$$T^{3/2}\tau_e = \frac{1}{B\nu_{th}\sigma}\exp\left(-\frac{\Delta S_n}{k}+\frac{\Delta H_n}{kT}\right) \qquad (1)$$

where B is a constant which comes from the effective density of state in the conduction band, $N_c=BT^{3/2}$. ΔS_n is the entropy change before and after electron excitation from the defect states to the conduction band. ΔH_n is the enthalpy needed to transfer an electron from the trap to the conduction band. We can consider the ionization process of slow-state traps at the inversion condition as the capture and emission of an electron or hole similar to the case of interface-localized defects. In our experiments, we have a global combination of all these microscopic relaxation times. The tunnel effect occurs between defect traps and the silicon substrate but this effect is clearly not a thermally activated mechanism. Then, equation (1) is suitable for our experiments because we can ionize the slow-state traps by trap-assisted impact ionization. Figure 1 and 2 show connected but different behaviors of slow-state and fast-state traps. The decrease of slow state traps density and, simultaneously, the increase of fast-state trap density can be explained by the difference in increase/decrease of creation sections values. Table 1 displays values of these creation section values we have obtained by fitting curves such as those shown on Figure 2. At high temperature, the fast state traps creation section is more important than the oxide traps creation section and inversely at low temperature [10]. For 9.4 nm oxide thin samples at 77 K, σ_{ss} = $2.0\text{x}10^{-20}$ cm^2 whereas σ_{fs} (77 K) = $9.5\text{x}10^{-26}$ cm^2. Slow-state traps are of another microscopic nature than faststate ones but they are connected by the same emission or capture kinetics. The densities of both fast state and slow state traps follow two kinetic creation mechanisms by fitting the two curves in figure 2, i.e. an exponential law and a linear law [11].

	Fast-state traps (N_{fs})	Slow-state traps (N_{ss})
9.4 nm 300 K	$1.3\text{x}10^{-19}$	$1.1\text{x}10^{-18}$
9.4 nm 77 K	$9.5\text{x}10^{-26}$	$2.0\text{x}10^{-20}$
5.4 nm 300 K	$2.9\text{x}10^{-26}$	$4.2\text{x}10^{-19}$
5.4 nm 77 K	$< 4\text{x}10^{-27}$	$8.8\text{x}10^{-20}$

Tab. 1: Values of creation sections σ (cm^2) at different temperatures and for two oxide thicknesses. The 77K value for 5.4 nm is at the limit detection for TDCV, which is about D_{fs} (min) ~ 10^9 cm^{-2} eV^{-1}.

As a model, for a sensitive interface defect method, dangling bonds of several natures in a 3-nm thickness from this surface, can communicate with the silicon. Several previous published results place the oxide charge centroid $\overline{x}$ roughly inside this 3-nm depth [5, 12, 13] and slow states are also oxide defects. At a microscopic level oxide and interface are not definite frontiers and chemical communication occurs between traps. Hydrogen or ion hydroxyl are implicated in traps exchange, it produced water damage to structure where mobile species can move [11, 12]. The following chemical equations are very likely to produce slow state traps (a fast-state trap is known as a Pb center and an oxygen vacancy is not linked in this case [10, 11, 14, 15]):

(1) Dissociation of H_3O^+ at the interface Si/SiO_2:

$$H_3O^+ + e^- \rightarrow H_2O + H$$

(2) H_3O^+ generation by the chemical reaction:

$$\equiv Si - O - H + H_2O \leftrightarrow \equiv Si - O^- + H_3O^+$$

4. Conclusion

The comparison of two kinds of traps occurring at the interface Si/ SiO_2 has been performed by using the new temperature dependent C(V) method (TDCV).

These two kinds of defects are different microscopically but intermingled in electron exchange being boosted by temperature effect. The slow-fast state correlation is thermally activated even without tunneling from oxide to silicon.

This technique is easy to implement requiring only widely available high-frequency capacitance-voltage (C-V) instrumentation. Measurements are easy to perform, and require only one C-V curve. Data analysis is uncomplicated for very thin 5.3 nm oxides and C-V step increments need to be low, 0.01V/s is a maximum value.

Because slow traps are responsible for long time electrical instabilities in MOSFET, it is of importance, from a theoretical and an experimental point of view, to compare slow-state traps with fast state traps. This study leads to infer that oxide defects are generally slow-oxide traps and oxide thickness shrinking would transform the oxide layer into a true interface.

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