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A SIMPLE ANALYTICAL CENTER POTENTIAL MODEL FOR CYLINDRICAL GATE ALL AROUND (CGAA) MOSFET

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ABSTRACT
In this paper, an analytical threshold voltage model is proposed for a Cylindrical Gate-All-Around (CGAA) MOSFET by solving the 2-D Poisson's equation in the cylindrical coordinate system. Both the center and the surface potential models are obtained and a comparison is made between them for CGAA MOSFET. This paper claims that the calculation of threshold voltage using center potential is more accurate rather than the calculation from surface potential. The effects of the device parameters like the cylinder diameter, oxide thickness, channel thickness, etc., on the center potential are also studied in this paper. The model is verified with commercially available 3D numerical device simulator Sentaurus from Synopsys.
Keywords: Gate All Around (GAA) MOSFET, Center Potential, Short Channel Effects (SCEs).

I. INTRODUCTION

The close proximity between source and drain reduces the capability of gate electrode to control the potential distribution as the dimensions of conventional Metal Oxide Semiconductor Field Effect Transistor (MOSFET) are scaled down. As a result the bulk silicon transistor is facing serious problem like Short Channel Effect (SCE). The two main manifestations of SCE are Drain Induced Barrier Lowering (DIBL) and the threshold voltage roll off. Consequently, the off state current increases and the on-off current ratio are degraded.

In coming future multiple gate MOSFETs (MuGFETs) are strong candidate for replacing conventional single gate MOSFETs. The electrostatic control of channel by gate increases in case of MuGFETs which dramatically reduces SCEs and also the lightly doped channel helps to alleviate the mobility degradation problem [1]. The Gate all around (GAA) MOSFET is considered one of the most promising device structures for further scaling down of CMOS technology. In this architecture, the channel is completely surrounded by the gate so that the gate has more control over the channel and SCEs can also be suppressed. The downscaling is the primary factor for the improvement in IC performance and cost, which contributes to rapid growth in

semiconductor industry. Because of the shorter dimension and higher drive current, GAA MOSFETs can achieve higher packing density as compared to double gate (DG) MOSFETs [2-3]. So, the GAA MOSFET has excellent electrostatic control of the channel, robustness against SCE, better scaling options, no floating body effect, larger Equivalent Number of Gate, ideal subthreshold swing, suppress corner effects, non-confinement of carriers near to Si/SiO2 interface, reduced natural length as compared to other MuGFETs and gives volume inversion [1,4,5].

In this paper, it has been observed that solving the channel potential at center may produce more accurate results as compared to surface potential. A simplified method has been adopted to solve the Poisson's equation. Again the threshold voltage expression of GAA MOSFET can also be derived by using the center potential model. The model results are verified with commercially available device simulator Sentaurus from Synopsis.

II. DEVICE STRUCTURE

The schematic diagram of the fully depleted GAA MOSFET structure used for modeling and simulation is shown in Fig. 1. The radial and lateral directions are assumed to be along the radius and the *z*-axis of the cylinder as shown in Fig. 1. The device has uniformly doped source–drain with doping concentration of $N_D = 1\times 10^{20}$ cm^{-3}. The channel is kept lightly doped with doping concentration of $N_A = 1\times 10^{16}$ cm^{-3}. The gate oxide thickness and the diameter of the silicon pillar are t_{ox} = 2 nm and t_{Si} = 10 nm, respectively. The work function of the gate material is: ϕ_M = 4.6 eV (e.g., Au).

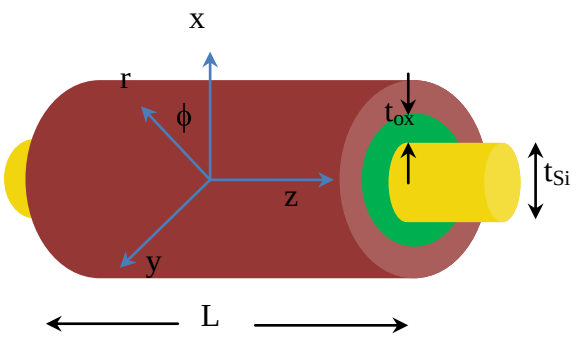

Fig.1: Schematic Structure of Cylindrical Gate All Around (CGAA) MOSFET

III. ANALYTICAL MODELLING OF CENTER POTENTIAL

The potential distribution $\phi(r,z)$ in the channel region has been obtained by solving the following 2-D Poisson's equation in cylindrical coordinate system.

$$\frac{1}{r}\frac{\partial}{\partial}\left(r\frac{\partial}{\partial r}\phi(r,z)\right)+\frac{\partial^2}{\partial z^2}\phi(r,z)=\frac{q\times N_a}{\varepsilon_{si}} \quad (1)$$

The potential distributions inside the channel region are approximated by a parabolic polynomial as:

$$\phi(r,z)=c_0(z)+c_1(z)\,r+c_2(z)\,r^2. \quad (2)$$

The coefficients c_0, c_1 and c_2 are functions of z only, and can be determined by using the given boundary conditions.

$$\phi(0,0)=V_{bi} \quad (3)$$

$$\phi(0,L)=V_{bi}+V_{ds} \quad (4)$$

where V_{ds} is the drain to source voltage and V_{bi} is the built in potential between the source/drain and Si channel junction and is given by

$$V_{bi}=\frac{KT}{q}\ln\left(\frac{N_A N_D}{n_i^2}\right) \quad (5)$$

From equation (2), if we consider $r = 0$ then that will become our center potential as given below:

$$\phi\ r,z\ \big|_{r=0} = c_0\ z \tag{6}$$

$$\phi\ 0,z\ = \phi_c\ z\ = c_0\ z \tag{7}$$

where $c_0\ z$ will be the center potential and is a function of z - only. The electric field at the center of the film is zero

$$\frac{\partial}{\partial r}\phi\ r,z\ \Big|_{r=0} = 0. \tag{8}$$

The electric field at the silicon oxide interface is given by

$$\frac{\partial}{\partial}\phi\ r,z\ \Big|_{r=t_{si}} = \frac{\varepsilon_{ox}}{\varepsilon_{si}}\frac{V_{gs} - V_{fb} - \phi\ r,z}{t'_{ox}} \tag{9}$$

where $t'_{ox} = \frac{t_{Si}}{2}\ln\left(1 + \frac{2t_{ox}}{t_{si}}\right)$, V_{gs} is gate to source voltage ε_{ox} and ε_{si} are the permittivity of SiO_2 and Si respectively and V_{fb} is the flat band voltage which is given as below:

$$V_{fb} = \phi_M - \phi_S \tag{10}$$

$$\phi_S = \frac{\chi_{Si}}{q} + \frac{E_{g,Si}}{2q} + \frac{kT}{q}\ln\left(\frac{N_a}{n_i}\right). \tag{11}$$

By differentiating the equation (2) with respect to 'r' and equating it with equation (8), one can get

$$c_1\ z\ = 0. \tag{12}$$

Further putting equation (12) in equation (2), we can get as

$$\phi\ r,z\ = c_0\ z\ + c_2\ z\ r^2. \tag{13}$$

Then by solving equation (13) using the given boundary conditions, the value of $c_2\ z$ can be calculated.

$$c_2\ z\ = V_{gs} - V_{fb} - c_0\ z\ \left(t_{si}^2\left(1 + \frac{2\varepsilon_{si}t'_{ox}}{\varepsilon_{ox}t_{si}}\right)\right)^{-1} \tag{14}$$

From equation (7), we can express the center potential as:

$$\phi\ r,z\ = \phi_c\ z\ + c_2\ z\ r^2. \tag{15}$$

The center potential can be calculated by calculating the potential at $r = 0$

$$\frac{1}{r}\frac{\partial}{\partial}\left(r\frac{\partial}{\partial r}\ \phi\ r,z\ \right)\Big|_{r=0} +$$

$$\frac{\partial^2}{\partial z^2}\ \phi\ r,z\ \Big|_{r=0} = \frac{qN_a}{\varepsilon_{si}}. \tag{16}$$

So, finally by solving the equation (16) at $r = 0$ with the help of above said boundary conditions and other expressions, one can get the center potential as given below:

$$\phi_c\ z\ = A\exp\left(\sqrt{\frac{4}{\lambda}}z\right) +$$

$$B\exp\left(-\sqrt{\frac{4}{\lambda}}z\right) + \left(V_{gs} - V_{fb} - \frac{\lambda qN_a}{4\varepsilon_{si}}\right) \tag{17}$$

where $\lambda = t_{si}^2\left(1 + \frac{2\varepsilon_{si}t'_{ox}}{\varepsilon_{ox}t_{si}}\right)$ (18)

and

$$A=\left[\frac{\left(V_{bi}-\left(V_{gs}-V_{fb}-\frac{\lambda qN_a}{4\varepsilon_{si}}\right)\right)\left(1-\exp\left(-\sqrt{\frac{4}{\lambda}}z\right)\right)+V_{ds}}{\exp\left(\sqrt{\frac{4}{\lambda}}L\right)-\exp\left(-\sqrt{\frac{4}{\lambda}}L\right)}\right] \tag{19}$$

$$B=-\left[\frac{\left(V_{bi}-\left(V_{gs}-V_{fb}-\frac{\lambda qN_a}{4\varepsilon_{si}}\right)\right)\left(1-\exp\left(\sqrt{\frac{4}{\lambda}}z\right)\right)+V_{ds}}{\exp\left(\sqrt{\frac{4}{\lambda}}L\right)-\exp\left(-\sqrt{\frac{4}{\lambda}}L\right)}\right]. \tag{20}$$

IV. RESULTS AND DISCUSSION

In this section, results obtained from theoretical models of the center potential are compared with the numerical simulation results.

The simulation is carried out by commercially available device simulator Sentaurus, a 3-D numerical simulator from Synopsis Inc. [6]. To study the center potential along the channel we have taken the cutline at the middle of the channel thickness across the x-axis of all the devices. In Figs. 2, 3, 4, and 5 the lateral position 15 nm in x-axis indicates the center of the channel of all the structures. To obtain accurate results for MOSFET simulation we need to account for the mobility degradation that occurs inside inversion layers. The degradation normally occurs as a result of the higher surface scattering near the semiconductor to insulator interface. So, in the simulation, the inversion layer Lombardi constant voltage and temperature (CVT) mobility model is used, that takes into account the effect of transverse fields along with doping and temperature dependent parameters of the mobility. The Shockley–Read–Hall (SRH) model simulates the leakage currents that exist due to thermal generation. Electrons in thermal equilibrium at given temperature with a semiconductor lattice obey Fermi-Dirac statistics. The use of Boltzmann statistics is normally justified in semiconductor device theory, but Fermi-Dirac statistics are necessary to account for certain properties of very highly doped (degenerate) materials. The Fermi-Dirac model uses a Rational Chebyshev approximation that gives results close to the exact values. The Auger recombination models for minority carrier recombination have been used. Furthermore, we chose Gummel's method (or the decoupled method) which performs a Gummel iteration for Newton solution [6]. In the simulation all the structure junctions assumed as abrupt, the biasing conditions considered at room temperature T=25^{0}C.

The center potential, $\phi\ 0,z$, and the surface potential, $\phi\left(\frac{t_{Si}}{2},z\right)$ for the CGAA MOSFET are compared in Fig. 2. The center potential curve lies above the surface potential one along with their minimum potential points.

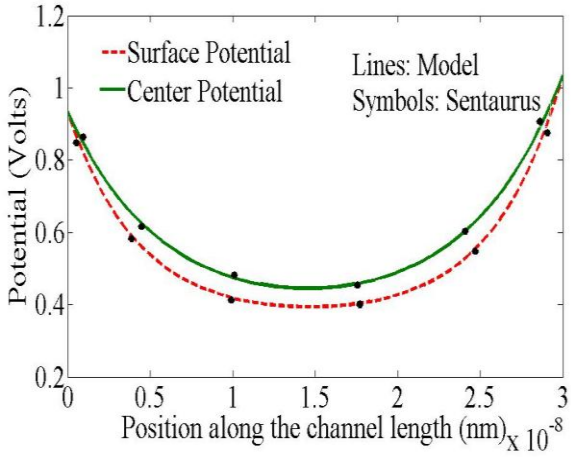

Fig.2: Potential along the channel length at body center and at the surface. Parameters used ϕ_M= 4.6 eV, N_A =1× 10^{16} cm^{-3}, t_{Si}=7.5 nm, L=30 nm, t_{ox}=2 nm, V_{GS}=0.1 V and V_{DS}=0.1 V.

It can be noted that source channel barrier height at channel center is lower than that of the surface and hence the threshold voltage should be calculated by using the center potential minima.

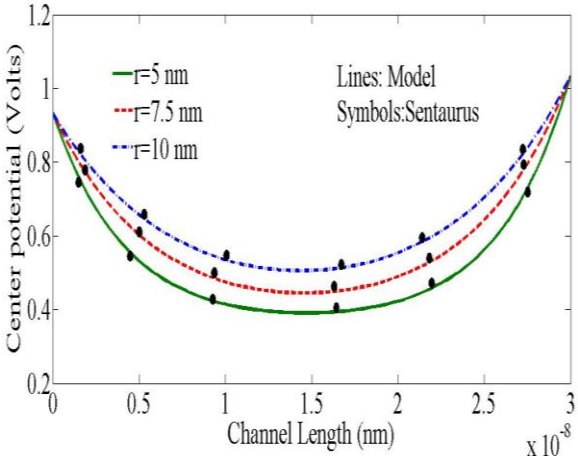

Fig.3: Center Potential along the channel length at various silicon thicknesses. Parameters used ϕ_M= 4.6 eV, N_A =1× 10^{16} cm^{-3}, L=30 nm, t_{ox}=2 nm, V_{GS}=0.1 V and V_{DS}=0.1 V.

Fig. 3 shows the variation of the center potential along the channel for three different radius/thin film thicknesses of GAA MOSFET. When the thin film thickness is reduced, the controllability of the gate over the channel becomes stronger in comparison to the influence exerted by the source/drain.

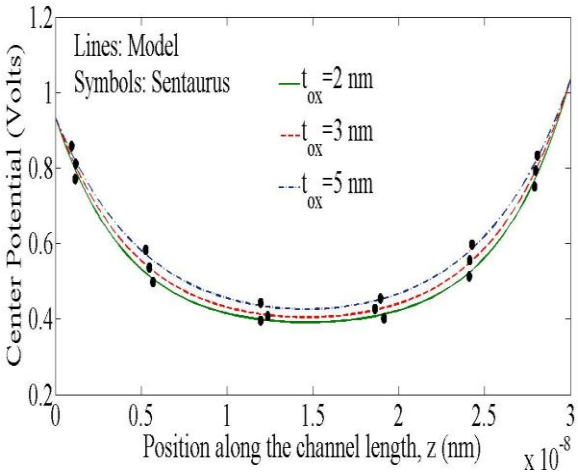

Fig.4: Center Potential along the channel length at various oxide thicknesses. Parameters used ϕ_M= 4.6 eV, N_A =1× 10^{16} cm^{-3}, t_{Si}=7.5 nm, L=30 nm, V_{GS}=0.1 V and V_{DS}=0.1 V.

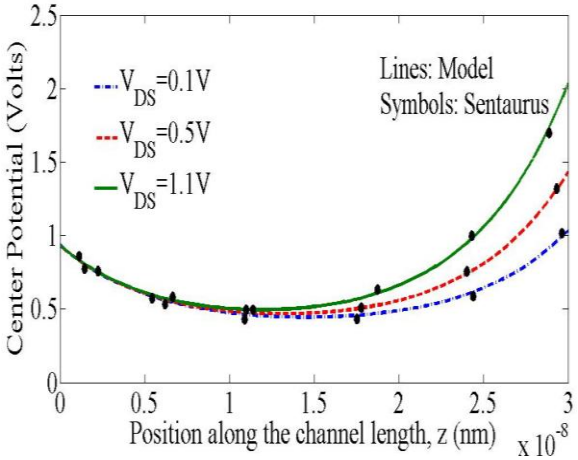

Fig.5: Center Potential along the channel length at various Drain Voltages. Parameters used ϕ_M= 4.6 eV, N_A =1× 10^{16} cm^{-3}, t_{Si}=7.5 nm, L=30 nm, and V_{GS}=0.1 V.

Fig. 4 shows the variation of the center potential along the channel for different oxide thicknesses. When the oxide thickness is reduced, the controllability of the gate over the channel potential increases, but at the same time it becomes more prominent to SCEs. Therefore, continuous scaling down

of the oxide thickness reduces SCEs. Also oxide thickness cannot be scaled down to very small values because tunneling through the thin oxide and hot-carrier effects become prominent.

Fig. 5 displays the center potential curve along the channel length at various values of the drain voltage. The presence of DIBL effect can be easily observed from Fig. 5 as the center potential minima point shows an upward movement with the increasing of drain voltage.

V. CONCLUSION

An analytical center potential model for the CGAA MOSFET is derived using a parabolic approximation of the channel profile. The paper proposes the threshold voltage calculation using center potential is more accurate than to the previous work wherein the threshold voltage based on surface potential. An extensive analysis is carried out to find the impact of numerous device parameters on the center potential of the CGAA MOSFET. Also, an appropriate selection of the oxide and the silicon thickness, gives an optimum threshold voltage at a given channel length. The derived 2-D analytical model is well matched with the simulation results obtained from Sentaurus^{TM} from Synopsys. The developed model may further be used for calculation of threshold voltage and Drain Induced Barrier Lowering (DIBL) of the device.

I. REFERENCES

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