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THRESHOLD VOLTAGE MODELING ON NANOCRYSTALLINE SILICON THIN FILM TRANSISTORS

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ABSTRACT

This paper presents an analytical model for calculating the threshold voltage in nanocrystalline silicon (nc-Si) thin film transistors using one-dimensional Poisson's equation. In this present study, it is assumed that gate insulator-silicon interface traps are uniformly distributed and the channel of the device contains large number of grain boundaries. Further, the effects of the gate insulator thickness and temperature on threshold voltage and hence on transfer characteristics has also been incorporated in this paper. It is observed that scaling down of the insulator thickness reduces the threshold voltage and hence improves the device characteristics at different temperatures and trap densities. The numerical calculations also demonstrate that the effect of the gate insulator thickness is less prominent at high temperature. The results so obtained are compared with the available experimental data which shows a satisfactory match thus justifying the validity of the model.

Keywords: Threshold-voltage (V_T); Thin-film transistors (TFTs); Nanocrystalline silicon (nc-Si:H); Gate insulator; Grain boundaries (GBs).

I. INTRODUCTION

Large area thin film transistors (TFTs) have been developed since the 1990's, for applications such as active matrix liquid crystal displays (AMLCDs) [1], organic light-emitting diode displays (OLEDs) [2], radio-frequency identification (RFID) tags [3] and medical X-ray imager [4]. In thin film electronics, thin film transistors are used as switching elements and for the fabrication of their peripheral driving circuits. Nanocrystalline silicon (nc-Si) thin film transistors (TFTs) are remarkable in terms of high-field effect mobility and uniformity in active-matrix liquid crystal displays. Nanocrystalline silicon (nc-Si:H) has been proposed as a promising alternative material to a-Si:H and poly-Si. The advantages of nc-Si:H over a-Si:H are high carrier mobility and better stability [5]. The advantages of nc-Si:H over poly-Si are low processing temperatures (as low as 150˚C), low manufacturing cost and better uniformity [6].

In nc-Si TFTs, there is a difference between threshold voltage and the ON voltage, same as in a-Si:H TFTs. Basically, the threshold voltage is defined as the gate voltage at which the inversion channel begin to appear within the grain and the ON voltage is defined as the knee of the characteristics [7]. Therefore it is required to develop an accurate model for threshold voltage which will be further useful for the device characterization.

Various models [8-10] have been proposed on threshold voltage in poly-Si TFTs however very limited work has been reported in case of nc-Si TFTs. Moreover, it is valuable to study how the threshold voltage in nc-Si TFTs is affected by gate insulator thickness and grain boundary trapping states at different doping density and temperature. In this study, it is assumed that the gate insulator and silicon interface traps are uniformly distributed across the interface region. Based on this assumption, this paper presents a simple and unique model for the extracting the threshold voltage in nc-Si TFTs.

This paper is organized as follows. First, we describe the theory used for the threshold voltage modeling. Next, we discuss the results of this developed model. Finally, we conclude this paper by giving important outcome of the study.

II. THEORY

Figure 1 shows the schematic view of top-gated nc-Si:H TFTs assumed for the modeling.

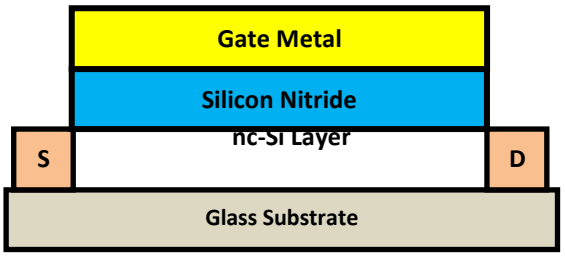

Figure 1: Schematic view of top-gated nc-Si:H TFTs.

The Poisson's equation in one dimensional form, used for determining the band bending at the gate insulator/nc-Si layer interface of the TFT, can be written as

$$\frac{\partial^2\varphi}{\partial x^2} = -\frac{\rho}{\varepsilon_{nc-Si}} \quad (1)$$

where φ is the electrostatic potential, ρ is the charge density and ε_{nc-Si} is the screening dielectric constant of nc-Si layer which can be theoretically calculated with the formula below[11]

$$\varepsilon_{nc-Si}(D_G) = 1 + \frac{10.4}{1+\left(\frac{1.88}{D_G \times 10^7}\right)^{1.37}} \quad (2)$$

where D_G is the average grain size in cm.

The charge density ρ is related to the density of trapping states N_t ($cm^{-3}eV^{-1}$) in nc-Si film, by the following equation

$$\rho = -q^2 N_t \varphi \quad . \quad (3)$$

Equation (1) can also be written in the form of electric field E as

$$E\frac{\partial E}{\partial \varphi} = q^2 N_t \frac{\varphi}{\varepsilon_{nc-Si}} \quad . \quad (4)$$

In order to get surface electric field, integrating equation (3) from the bulk towards the surface

$$\int_{Bulk}^{Surface} E\,\partial E = \frac{q^2 N_t}{\varepsilon_{nc-Si}} \int_{Bulk}^{Surface} \varphi\,\partial\varphi \quad (5)$$

which gives surface electric field as

$$E_s = q\,\varphi_s\sqrt{\frac{N_t}{\varepsilon_{nc-Si}}} \quad (6)$$

where φ_s is the surface potential and under strong inversion can be given as

$$\varphi_{s\,(inv)} \approx 2\varphi_F \approx 2\frac{kT}{q}\ln\left(\frac{N_a}{n_i}\right) \quad (7)$$

where φ_F is the Fermi potential, N_a is the acceptor doping density (cm^{-3}), k is Boltzmann's constant, T is the temperature and n_i is the intrinsic carrier density which can be calculated by using the equation [12]

$$n_i = 2\left(\frac{2\pi kT}{h^2}\right)^{3/2}\left(m_n^* m_p^*\right)^{3/4} e^{-\frac{E_g}{2kT}} \quad (8)$$

where h is the Planck's constant, E_g is the bandgap energy (= 1.12eV) and m_n^* and m_p^* are the effective electrons and holes masses in nc-Si given as $m_n^* = 0.34\,m_O$ and $m_p^* = 0.55\,m_O$ [11].

Now the gate insulator electric field can be determined by using the following equation

$$E_i = \frac{\varepsilon_{nc-Si}}{\varepsilon_i} E_s \quad (9)$$

where ε_i is the dielectric constant of insulating layer. In this study, we have assumed the insulating layer as silicon nitride.

From equations (2), (6) and (9), we get the gate insulator electric field at threshold as

$$E_{Si-N_X}(inv) = \frac{q\varphi_s}{\varepsilon_i}\sqrt{N_t \times \left[1 + \frac{10.4}{1+\left(\frac{1.88}{D_G \times 10^9}\right)^{1.37}}\right]} \quad (10)$$

The threshold voltage is given as

$$V_T = \varphi_s + V_i(inv) \quad (11)$$

where $V_i(inv)$ is the voltage across the silicon nitride insulator and thus equal to $t_i E_i(inv)$.

Therefore the threshold voltage becomes

$$V_T = \varphi_s\left[1 + \frac{qt_{ox}\sqrt{N_t}}{\varepsilon_{ox}}\sqrt{1 + \frac{10.4}{1+\left(\frac{1.88}{D_G \times 10^7}\right)^{1.37}}}\right] \quad (12)$$

In nc-Si TFT, the effective carrier mobility (μ_{eff}) is affected by the height of potential barrier (Ψ_B) which is present at the grain boundary when the grains are partially depleted of carriers and as in nc-Si TFT the nanocrystalline silicon consist of large number of grains separated by grain boundaries, so the expression for μ_{eff} proposed by N. Gupta [10] can be modified as

$$\mu_{eff} = \frac{\mu_G}{1+M\left[\frac{\mu_G D_{GB}}{\mu_{GB} D_G}\right]exp\left(\frac{q\Psi_B}{kT}\right)} \quad (13)$$

where μ_G is the bulk grain mobility, μ_{GB} is carrier mobility in the grain boundary, D_G is the average grain size, D_G is the average grain boundary size and M is the mobility degradation factor given as M = exp(γ). This mobility degradation factor is required in order to include the effect of carrier scattering due to surface roughness which exponentially decreases the effective carrier mobility with the gate voltages.

For an n-channel TFT, the total carrier concentration (N) in the strong inversion channel is approximately equal to gate induced electron

concentration and is given as[13]

$$N = \frac{C_i (V_G - V_T)}{q t_{si}} \quad (14)$$

where V_G is the gate voltage, t_{si} is the nc-Si inversion layer thickness and C_i is the gate insulator capacitance per unit area.

The potential barrier height within the grains is given as [14] :

$$\Psi_B = \frac{q n_t^{\,2}}{8 N \varepsilon_{nc-Si}} \quad (15)$$

where n_t (cm^{-2}) is the density of charged states at the grain boundaries and can be extracted from a linear fit to $\ln\left(\frac{I_D}{V_{GS}}\right)$ vs $\frac{1}{V_{GS}}$ by using the following equation [15]

$$\frac{I_D}{V_{GS}} = \frac{W}{L} \mu_0 V_{DS} C_i \, exp\left(-\frac{q^3 n_t^{\,2} t_{si}}{8 \varepsilon_i k T C_i} \frac{1}{V_{GS}}\right) \quad (16)$$

where $\frac{W}{L}$ is the channel width to channel length ratio, V_{DS} is the drain-source voltage, μ_0 is the carrier mobility at the equilibrium condition. The drain current (I_{DS}) of nc-Si TFT under the linear region can be given as [13]

$$I_{DS} = \mu_{eff} \frac{W}{L} C_i \left[V_{DS}(V_{GS} - V_T) - \frac{V_{DS}^{\,2}}{2}\right]. \quad (17)$$

III. RESULTS AND DISCUSSION

Table 1 shows the values of the parameters used in the calculations. For the calculation of n_t, the experimental data [16] was used to plot $\ln\left(\frac{I_D}{V_{GS}}\right)$ vs $\frac{1}{V_{GS}}$, which happens to be a straight line. Using MATLAB Linear Regression Analysis, the slope of this straight line was found to be -6.226 as from Equation (16), we get $n_t = 3.5.10^{11}$ cm^{-2}. The value of threshold voltage (V_T) is extracted from equation (12) by using MATLAB and it comes out to be 2.86V which matched well with the experimental value [16].

Figure 2 shows the variation of threshold voltage with gate insulator thickness for different trap density values. It is noticed that the threshold voltage increases with increases in trap density for a given value of gate insulator thickness. This is attributed to the fact that number of free carriers available for the conduction decrease with increase in trap density. It is also observed that as thickness of gate insulator increases, threshold voltage also increases for all values of trap density. This due to the fact that as gate insulator thickness increases, the gate voltage which is required to achieve strong inversion state in the nc-Si channel layer also increases.

Figure 3 shows the threshold voltage variation with the acceptor doping concentration at different value of gate insulator thickness. It is observed that the threshold voltage increases with increase of acceptor doping concentration at a given value of gate insulator thickness. It is also observed that difference in threshold voltage is higher for large values of doping density as compared to that small value of doping density. This is attributed to the fact that the trap density becomes high for larger doping density and these trap states increases the potential barrier across the nc-Si layer and thus degrade the performance of the device.

Table 1: Parameters used in the calculations

Parameters	**Symbols**	**Values**
Channel length	L	50nm
Channel width	W	200nm
Grain size	D_G	25nm
Grain boundary width	D_{GB}	2.5nm
Drain voltage	V_{DS}	1V
nc-Si inversion layer thickness	t_{si}	80nm
Bulk grain mobility	μ_G	203cm^2 Vs^{-1}
Grain boundary mobility	μ_{GB}	0.3cm^2 Vs^{-1}
Mobility degradation factor	M = exp(γ)	γ= 0.7 at V_G< 11V γ= 1 at V_G> 11V

Figure 4 plots the threshold voltage variation with trap density at various values of gate insulator thickness for grain size of 25 nm and moderate

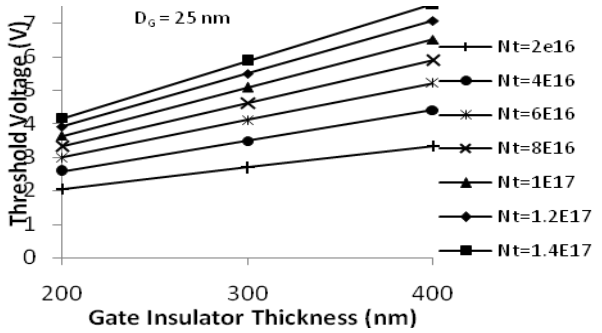

Figure 2: Variation of threshold voltage as a function of gate insulator thickness for different values of trap density.

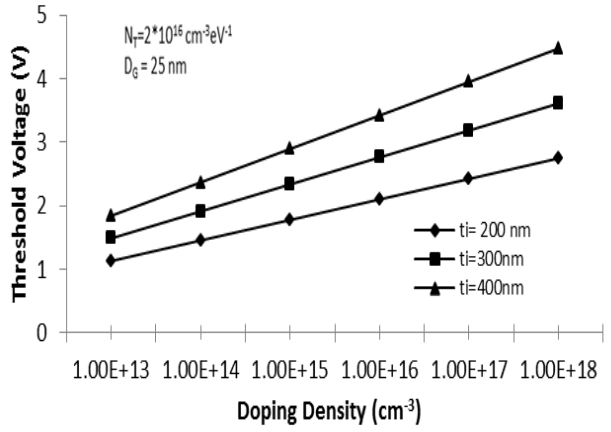

Figure 3: Variation of threshold voltage as a function of acceptor doping concentration for different values of gate insulator thickness.

doping concentration. It is observed that the decrease in gate insulator thickness causes the decrease in trap states exist in gate insulator and thus decreasing the threshold voltage. Figure 5 shows that how threshold voltage varies with trap density at different temperatures. It is seen that as the temperature increases, the carriers available for conduction increases and thus channel formation occur at small gate voltage. This results in the reduction of threshold voltage.

To validate the model, the variation of drain current versus gate voltage of n-channel nc-Si TFT calculated at V_{DS} = 1V for V_T = 2.86Vis shown in figure 6 and is compared with experimental values of Lee et. al.[16]. It can be seen that in the higher gate voltage region (V_G > 8V), the computed variation are in excellent agreement with

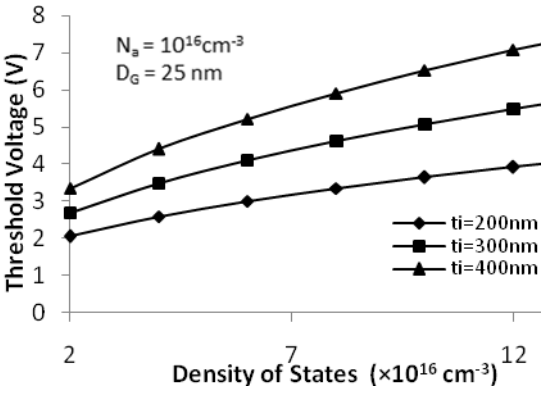

Figure 4: Variation of threshold voltage as a function of trap density for different values of gate insulator thickness

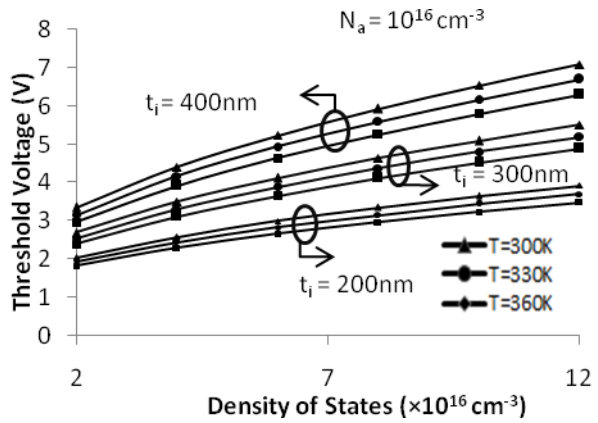

Figure 5: Variation of threshold voltage as a function of trap density for different values of gate insulator thickness at different temperatures.

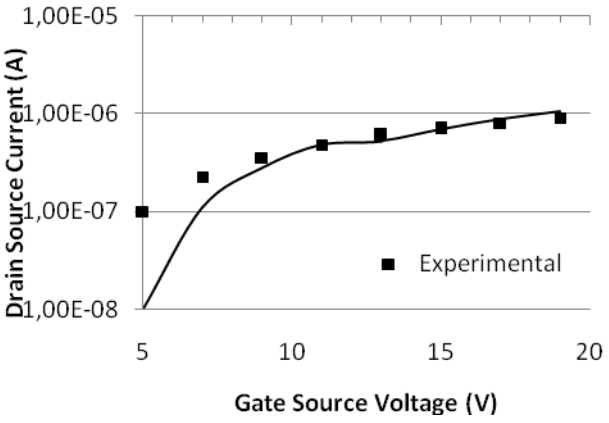

Figure 6: Plot of the transfer characteristics of n-channel nc-Si TFT (W=200nm, L=50nm) calculated at V_D=1V for V_T=2.86V, N_a=1016cm^{-3} and N_t= 2×1016cm^{-3}.Solid dark line shows the result of C.H.Leeet. al.[16]

experimentally observed values, however in the region (V_G< 8V) there is a disagreement between the computed and experimental results. This is because the effect of grain boundaries is more pronounced at low gate voltage and the channel used for experiments may slightly different in terms of purity of nanocrystalline silicon material.

IV. CONCLUSION

In this paper, a model for determining the threshold voltage of nc-Si TFTs including the effect of gate insulator thickness is presented. In this proposed model, it is assumed that the gate insulator and silicon interface traps are uniformly distributed across the interface region. The results demonstrate that the threshold voltage of nc-Si TFT increases with increases in trap density and acceptor doping concentration for a particular value of gate insulator thickness. Numerical calculations also demonstrated that the decrease in gate insulator thickness causes the decrease in the threshold voltage. It is further seen that as the temperature increases, the threshold voltage decreases. The validity of this model was verified through the satisfactory agreement between theoretical and experimental data.

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