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DIFFERENTIALLY GRADED JUNCTIONLESS TRANSISTOR

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ABSTRACT
In this work, we propose a differentially graded double gate junctionless transistor (DGJLT) and compared it with a uniformly doped double Gate junctionless transistor (DGJLT) in respect of on-current, off-current and I_{on}/I_{off} ratio. In our investigation, we found that the differentially graded DGJLT shows significant improvement in device performance and hence it may prove to be a better switching device when compared to uniformly doped DGJLT. In this paper we also show the electron concentration in off and on state for both the devices and find that differentially graded DGJLT has better control over channel.
Keywords: double gate junctionless transistor (DGJLT), uniformly doped, differentially graded.

I. INTRODUCTION

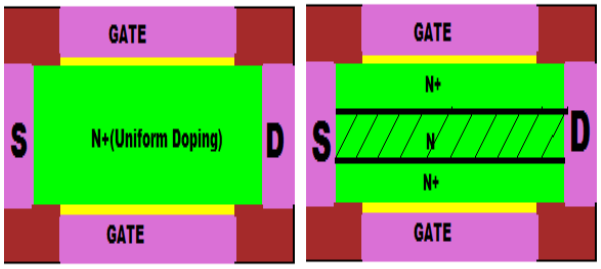
As we scale down the conventional metal-oxide-semiconductor field effect transistor (MOSFET), complex fabrication and device processing problems arise due to shallow junctions. Besides, as we scale down the device in sub-20nm regime, short- channel effects become important which affect device performances. Recently junctionless transistor has been proposed and fabricated successfully [1]. Some of the proposed junctionless transistors are SOI-JLT [2], BPJLT [2], Silicon channel double gate junctionless transistor [3] and nanowire structure with all around gate [4]. Currently junctionless tunnel field effect transistor has been demonstrated [5]. Traditional C-MOS inverter is also designed from the n and p type junctionless transistor [6] and cost evolution of the C-MOS junctionless transistor has also been carried out. The FinFET structure of bulk junctionless transistor has been demonstrated and device performance has been compared with SOI-JNT [7]. Several thin-film structure of junctionless transistor has been demonstrated [8]-[11]. The p type germanium body junctionless transistor has also been demonstrated and it has been shown that the device has better analog performance compared to silicon body JLT [12].

Junctionless transistor is also used for memory design. 6-T SRAM of 20-nm channel junctionless nanowire transistor has been proposed [13] and the static noise margin of 185mV has been achieved. Besides, 1-T DRAM of junctionless transistor has also been demonstrated. Recently junctionless transistor has been fabricated with laser scribing method and it has been found to be a cost efficient fabrication method [14]. Junctionless diode has also been demonstrated [15]. Modeling of drain current for double gate JLT and trigate JLT has been done [16]-[18]. Advantage of JLTs over conventional MOSFETs are, 1) easy fabrication process, 2) cost efficiency and scalability, 3) better analog and digital performance, 4) less short channel effects and 5) less impact ionization effects. Junctionless transistor is a device with a semiconductor layer beneath the gate oxide, where semiconductor layer has no P-N junction. Device is either n+-n+-n+ or p+-p+-p+ and source, drain and channel have same type of doping. For n type of JLT in off-state (at Vg=0V), channel is fully depleted by work-function difference between gate and channel. A very low current flows through the lower part of channel. As we increase gate voltage, charge carriers start to accumulate in the channel and further increase in gate voltage causes accumulation of electrons and a high I_{on} flows through bulk of the device.

In this work we propose the differentially graded DGJLT, which provides better digital performance. In the rest of the paper we demonstrate the device structure and operation of differentially graded DGJLT and compare with uniformly doped DGJLT.

II. DEVICE STRUCTURE AND OPERATION

Fig. 1(a) shows the device structure of uniformly doped DGJLT. The device has n-type of channel with uniform channel doping concentration of 10^{19} cm^{-3} and source, channel and drain have same doping concentration of 10^{19} cm^{-3}. Device parameters used for simulations are listed in table 1. Device channel is stacked by gate oxide of 1nm which has relative permittivity of 3.9. Channel length of device used is 30 nm. Device parameters used here are listed in table 1. Gate work function used is 5.3eV. Fig. 1(b) shows the proposed differential graded DGJLT. Device has the same device aspect ratio as of uniformly doped DGJLT but upper and lower layer of the device are highly doped with doping concentration of 10^{19} cm^{-3} and middle layer of the device is lightly doped with doping concentration of 10^{18} cm^{-3}. Channel is stacked by gate oxide of thickness 1nm and metal gate of work function 5.3 eV from both sides of channel. Doping concentration profiles for both the devices are shown in table 2.



(a) (b)

Fig. 1: (a) Schematic representation of the uniformly doped DGJLT and (b) schematic representation of proposed differential graded DGJLT with L_g =30 nm, T_{si}=10 nm, N_d=10^{19} cm^{-3} , T_{ox}=1nm and Φ_g=5.3 eV.

For both the devices, performances are obtained by 2-D device simulation. Device simulations are performed using the Synopsys Taurus-Medici device simulator. Standard models used are fldmob, prpmob, conmob, consrh, auger and bgn. Mobility models fldmob, prpmob, conmob are electric field, transverse electric field and concentration dependent respectively. Models, such as, Shockley read-hall model (consrh), band gap narrowing model (bgn) and auger recombination model (auger) are included because of high doping concentration.

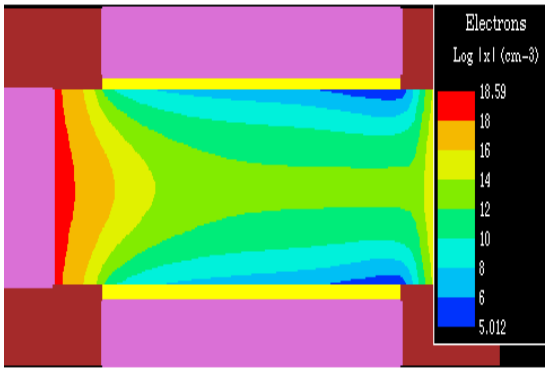
Table 1: Parameters used for device simulation

Parameter	Differentially Graded DGJLT	Uniformly Doped DGJLT
Channel length	30 nm	30 nm
Device layer thickness	12 nm	12 nm
EOT of gate dielectric	1 nm	1 nm
Dielectric constant	3.9	3.9
Gate work function	5.3 eV	5.3 eV
Drain supply voltage	1.0 V	1.0 V

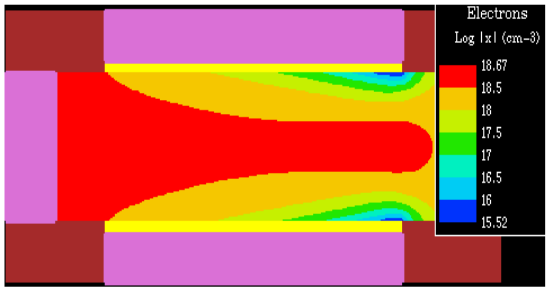
Table 2: Device Doping Variation:

Channel Position From Top (nm)	Nd (Differentially Graded DGJLT) (cm^{-3})	Nd (Uniformly Doped DGJLT) (cm^{-3})
0-4	10^{19}	10^{19}
4-8	10^{16}-10^{19} c	10^{19}
8-12	10^{19}	10^{19}

Fig. 2 shows contour of electron concentration of the uniformly doped DGJLT. Fig. 2(a) shows the contour of electron concentration in off state (at V_g=0V and V_d=1V) condition of uniformly doped DGJLT. For lower off-current channel should be fully depleted. From Fig. 2(a) we observe that middle layer of DGJLT has electron concentration of ~10^{14} cm^{-3}. Gate is unable to deplete center layer of the channel. Fig. 2(b) shows electron concentration in ON-state (at V_g=1V and V_d=1V). The channel has good electron concentration except near the drain region, because of pinch-off. The highest electron concentration in on-state is ~$10^{18.57}$ cm^{-3}. The higher electron concentration makes the channel conducting and provides high ON-state current.



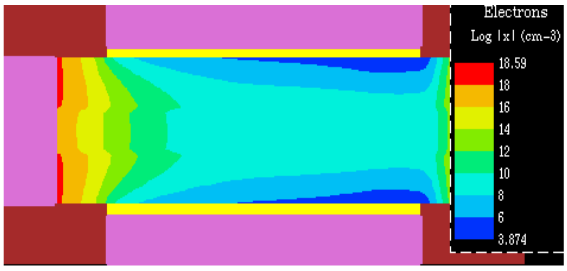
(a)



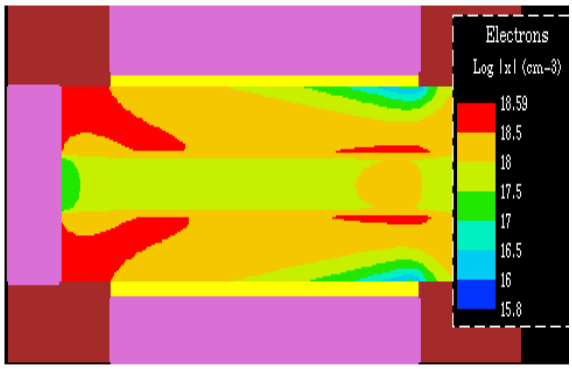
(b)

Fig. 2: Electron concentration in the uniformly doped DGJLT. Fig. 2(a) In off state, V_g=0 V, V_d=1 V; Fig. 2(b) In on state, V_g=1 V and V_d=1 V with L_g=30 nm, T_{si}=12 nm, N_d=10^{19} cm^{-3}, T_{ox}=1 nm.

Fig. 3 shows the electron concentration of differential graded DGJLT. In differential graded DGJLT structure, channel has differential doping concentration in vertical direction. For the structure, upper 4 nm has doping concentration of 10^{19} cm^{-3}, middle 4nm has doping concentration of 10^{17} cm^{-3} and the lower 4 nm has doping concentration of 10^{19} cm^{-3}. Fig. 3(a) shows electron concentration in off-state condition of the differential graded DGJLT. From Fig. 3(a) we observe that the device is better depleted compared to the uniformly doped DGJLT. In the middle-region of device, electron concentration is reduced to ~10^{10} cm^{-3}. From Fig. 3(a) we also observe that near the source region device is better depleted compared to uniformly graded DGJLT. Fig. 3(b) shows the electron concentration of differentially graded DGJLT in on-state. From Fig. 3(a) we observe that the differentially graded DGJLT has similar electron concentration compared to the uniformly doped DGJLT. In the middle region electron concentration has reduced to 10^{18} cm^{-3} from $10^{18.67}$ cm^{-3}. Later in this paper we show that in differentially graded DGJLT off-state current is reduced by several orders with similar order of the on-state current when compared to uniformly doped DGJLT.



(a)



(b)

Fig. 3: Electron concentration of the differential graded DGJLT. Fig. 3(a) In off-state, Vg=0 V, V_d=1 V and Fig. 3(b) In on state, V_g=1 V, V_d=1 V with L_g=30 nm, T_{si}=12 nm, T_{ox}=1 nm.

Fig. 4 shows the I_d-V_g plot of uniformly doped DGJLT and differentially graded DGJLT for different drain voltages. From Fig. 4 we observe that uniformly doped DGJLT has off-state current (V_d=1V and V_g=0V) of order of ~10^{-10} amp/µm and it is reduced to order of ~10^{-13} amp/µm for the differentially graded DGJLT. Similarly at V_d=0.05 V uniformly doped DGJLT has off-state current (V_d=0.05V and V_g=0V) of ~10^{-14} amp/µm and for differentially graded DGJLT off-state (V_d=0.05V and V_g=0V) current is reduced to ~10^{-11} amp/µm. I_{off} is reduced approximately by 3 orders in differentially graded DGJLT when compared to uniformly doped DGJLT. Uniformly doped DGJLT has on-current (V_d=1V and V_g=1V) of ~4.07X10^{-4} amp/µm and differentially graded DGJLT has on-current of ~3.07X10^{-4} amp/µm. Similarly at V_d=0.05V uniformly doped DGJLT has on-current (V_d=0.05V and V_g=1V) of ~9.53X10^{-5} amp/µm and differentially graded DGJLT has on-current of ~8.62X10^{-5} amp/µm. From the given data we observe that on-state current is

similar with a large reduction in the off-state current, hence improving I_{on}/I_{off} ratio.

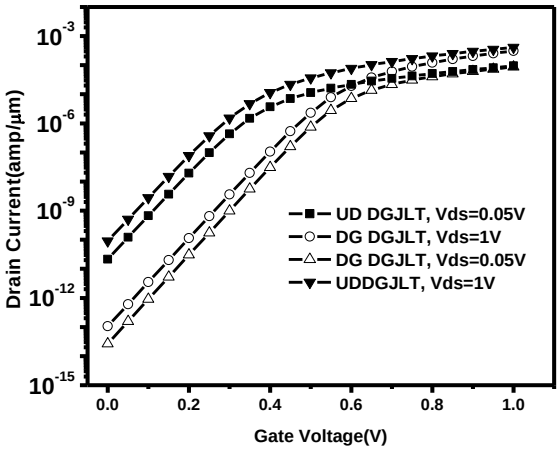


Fig. 4: Id-Vg plot of uniformly doped DGJLT (UD DGJLT) and differentially graded DGJLT (DG DGJLT) at different drain voltages of V_d= 0.05V and V_d=1 V, N_d=10^{19} cm^{-3}, Lg=30 nm, T_{si}=12 nm, T_{ox}=1 nm, T_{mid}=4 nm, N_{mid}=10^{18} cm^{-3}.

Fig. 5 shows the off-state current with varied channel length. From Fig. 5 we observe that I_{off} decreases with increasing channel length for both uniformly doped DGJLT and Differentially Graded DGJLT. Fig. 5 shows that differentially graded DGJLT has lower I_{off}. For channel length of 60nm differentially graded and uniformly doped DGJLT have I_{off} of ~2.91X10^{-15} and ~1.84X10^{-12} amp/μm respectively. Similarly for channel length of 30nm differentially graded and uniformly doped DGJLT have I_{off} of ~1.737X10^{-11}amp/μm and ~1.0223X10^{-8} amp/μm respectively. I_{off} is reduced by ~3 orders in differentially graded DGJLT. Fig.6 shows the I_{on} of differentially graded DGJLT and uniformly doped DGJLT with varying channel length. From Fig.6 we observe that both have similar on current. From Fig. 5 and Fig. 6 we observe that in differentially graded DGJLT I_{on}/I_{off} ratio is improved to ~2.90X10^{9} from ~4.50X10^{6}, for uniformly doped DGJLT of 30 nm channel length.

Schematic diagram of the devices are shown in Fig. 1. We have increased device thickness to 20 nm to show the effect of device thickness on performance. Device parameters used for simulations are listed in table 3. Both the devices have same device parameters except doping concentration. Doping concentration profiles for both the devices are shown in table 4.

Table 3: Parameters used for device simulation

Parameter	Differentially Graded DGJLT	Uniformly Doped DGJLT
Channel length	60 nm	60 nm
Device layer thickness	20 nm	20 nm
EOT of gate dielectric	1 nm	1 nm
Dielectric constant	3.9	3.9
Gate work function	5.3 eV	5.3 eV
Drain supply voltage	1.0 V	1.0 V

Table 4: Device doping variation

Channel Position From Top (nm)	Nd (Differentially Graded DGJLT) (cm^{-3})	Nd (Uniformly Doped DGJLT) (cm^{-3})
0-6	10^{19}	10^{19}
6-14	10^{18}	10^{19}
14-20	10^{19}	10^{19}

In this section we have taken thicker channel structure. In thicker channel uniformly DGJLT, problems are severe. Uniformly doped DGJLT is not turned off in off-state. As we have explained earlier, in uniformly doped DGJLT, the extent of channel depletion decreases with the distance from gate. For thicker channel structure, in the center of channel, distance from the gate is increased, which causes reduction in channel depletion. The center layer of channel remains non-depleted in off-state, i.e., at zero gate bias, gate work function is unable to deplete the center of channel, which causes large off-state current from the bulk of device and hence the device is not turned off in off-state. In proposed device structure of differentially graded DGJLT, center layer of channel contains low doping concentration of 10^{18} cm^{-3}. Top and bottom gates deplete the highly doped top and bottom layers of DGJLT and due to low doping concentration in the center it is easily depleted with the help of both gates and very low off-state current flows through entire channel. Fig. 7 shows the I_d–V_g characteristics of the uniformly doped DGJLT and differentially graded DGJLT with 60 nm gate length and 20 nm thick

channel. In case of uniformly doped DGJLT, I_{off} is $1.117X10^{-5}$ amp/μm and I_{on} is $6.03X10^{-4}$ amp/μm. It can be seen that uniformly doped DGJLT has very modest I_{on}/I_{off} of 45. Poor I_{on}/I_{off} of uniformly doped DGJLT is because of huge off-state current flow through center of the channel. In the differentially graded DGJLT, I_{off} is $1.492X10^{-12}$ amp/μm and I_{on} is $2.84X10^{-4}$ amp/μm. It can be seen that differentially graded DGJLT has improved I_{on}/I_{off} of $2X10^{8}$ because in case of differentially graded DGJLT channel is fully depleted in off-state.

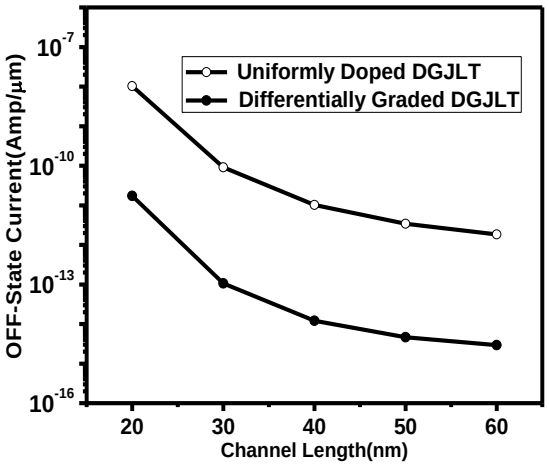


Fig. 5: I_{off} of uniformly doped DGJLT and differentially graded DGJLT with varying channel length with V_d=1 V, $N_d=10^{19}$ cm^{-3}, Lg=30 nm, T_{si}=12 nm, T_{ox}=1 nm, T_{mid}=4 nm, $N_{mid}=10^{18}cm^{-3}$.

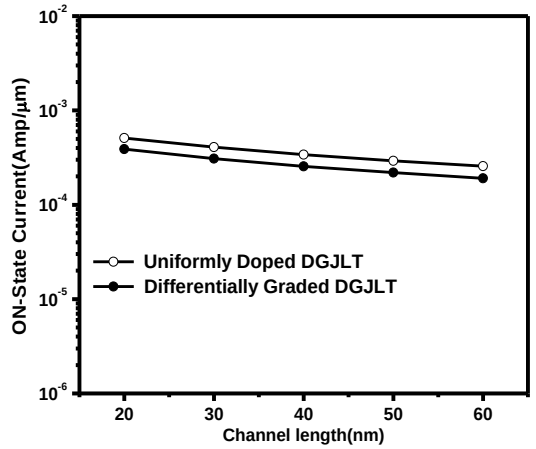


Fig. 6: On-state current of uniformly doped DGJLT and differentially graded DGJLT with varying channel length with V_d=1 V, $N_d=10^{19}$ cm^{-3}, Lg=30 nm, T_{si}=12 nm, T_{ox}=1 nm, T_{mid}=4 nm, $N_{mid}=10^{18}$ cm^{-3}

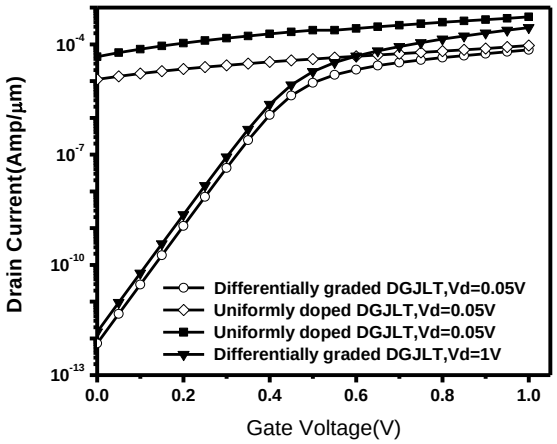


Fig. 7: Id-Vg plot of uniformly doped DGJLT (UD DGJLT) and differentially graded DGJLT (DG DGJLT) at different drain voltages of V_{DD}=0.05 V and V_{DD}=1 V, $N_d=10^{19}$ cm^{-3}, Lg=60 nm, T_{si}=30 nm, T_{ox}=1 nm.

III. CONCLUSION

In this work, we proposed a differentially graded DGJLT and the results are compared with its uniformly doped DGJLT. Differentially graded DGJLT offers better I_{on}/I_{off} ratio and has better switching characteristics. Further improvement in the device performance can be obtained by using III-V compound materials and strained silicon.

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