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ULTRA THIN IMPACT IONIZATION MOSFET (UTIMOS) FOR REDUCED OPERATING VOLTAGES

Ankit Dixit, Sangeeta Singh, P. N. Kondekar

Department of Electronics and Communication Engineering, PDPM-IIITDM, Jabalpur, MP, India
ankit.dixit@iiitdmj.ac.in

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ABSTRACT

Impact Ionization MOSFET (IMOS), is a device that has led to the revolution in super steep sub threshold slope devices. It has resolved one of the most critical and fundamental problem of sub-threshold slope (SS) which cannot be lower than 60 mV/decade at room temperature for conventional MOSFET. An IMOS device working is based on the avalanche breakdown mechanism. In this paper, we have proposed ultra thin impact ionization MOSFET (UTIMOS) as an improved structural variant of the lateral impact ionization MOSFET (LIMOS). UTIMOS is having very much lower breakdown voltage hence its operating voltage is reduced to a great extent. Simulation results claims that ultra thin impact ionization MOSFET has much better device performance parameters as compared with the lateral impact ionization MOSFET. The intensified electric field in vertical direction due to smaller thickness of device silicon layer T_{Si} is the key feature of the UTIMOS. Simulation results show the sub-threshold slope SS to be 1.37 mV/dec for proposed UTIMOS. It shows considerable improvement in other device performance parameters also.

Keywords: Impact Ionization, avalanche breakdown, drain induced current enhancement (DICE), gate induced barrier lowering (GIBL).

I. INTRODUCTION

For past few decades CMOS technology has headed towards the path of aggressive down scaling as it showed excellent performance and scaling properties. But since last decade semiconductor industry faces many challenges related to scaling, such as alarming exponential trend in sub-threshold power dissipation. This exponential increase in the static leakage power is associated with the sub threshold slope. The sub threshold slope of a conventional MOSFET is defined as inverse derivative of the log of drain current with respect to the gate voltage in low current regime. Theoretically the minimum value of SS for a conventional MOSFET is limited by its thermodynamic diffusion limit (kT/q)(ln10) = 60mV/dec at 300 K. In order to deal with this problem many novel devices have been proposed to replace or complement CMOS whose device operation are not diffusion limited. Here, we will focus on the Impact Ionization MOSFET (IMOS) device [1], [2] and [3]. The unique feature of the IMOS device is that it has a super steep sub-threshold swing less than 60 mV/dec at room temperature. In MOSFETs gate controls the thermally injected carriers by a channel potential barrier. Whereas, IMOS devices have no channel potential barrier, it uses the potential difference between the source and the channel to determine whether breakdown occurs or not. Since the carriers of I-MOS devices are injected by avalanche breakdown process instead of thermal injection, the sub threshold swing can be reduced even below 60 mV/dec at room temperature. Researchers has explored the various aspects of the IMOS operation and fabrication process flow [4], biasing [5], circuit level implementation, sensor applications [6] and memory implementations [7]. They have reported the analytical and compact mathematical modeling also for IMOS [8] and [9], its reliability issue [10] and h-spice model [11] and [12]. But still there is a crucial literature gap in relating the operating breakdown voltage V_{br} with the thickness of the device silicon layer T_{Si}. In this paper, we have related the breakdown voltage V_{br} with the thickness of the device silicon layer T_{Si} and hence proposed ultra-thin impact ionization MOSFET (UTIMOS) as a improved structural variant of the Lateral impact ionization MOSFET (LIMOS). UTIMOS is having very much lower breakdown voltage hence its operating voltage is reduced to a great extent. Simulation results claims that ultra thin impact ionization MOSFET has much better device performance parameters as compared with the lateral impact ionization MOSFET.

This paper is structured as follows. In Section II, the device structure of UTIMOS and simulation parameters for studying the device characteristics and device operation are introduced, Section III device performance parameters are studied. Finally, Section IV concludes the device characteristics of UTIMOS.

II. DEVICE STRUCTURE AND SIMULATION

Fig. 1 shows the n-channel ultra thin impact ionization MOSFET UTIMOS architecture used for the simulation modeling and analysis with silicon-on-insulator (SOI) implementation. Conceptually, the UTIMOS transistor is also combination of a p-i-n diode and a MOS transistor. The first constitutes the intrinsic area of the IMOS, and second part is the MOS part. Similar to the IMOS, in n-channel UTIMOS device also, the p^+ is the source and the n^+ is the drain because the p-i-n diode is always reverse biased. Conceptually, in UTIMOS the vertical gate induced field and the MOS surface carrier concentration affect the breakdown voltage of the diode and the surface concentration of carriers in the 'ON' state of the IMOS transistor depends on the number of carriers injected by the avalanche breakdown

mechanism in the diode. Hence, the smaller thickness of the device silicon layer T_{Si} leads to more. Intense electric field in vertical direction and hence break down voltage V_{br} reduces. This intensified vertical electric field due to reduced thickness of device silicon layer T_{Si} is the key feature of the UTIMOS.

Various device performance parameters such as drain current I_d, on-current I_{on}, off-current I_{off}, on-current to off current ratio I_{on}/I_{off} , DICE, GIBL, sub-threshold slope (SS), and transconductance g_m for the UTIMOS are investigated using Synopsys TCAD Sentaurus simulator version vG-2012.06 [13] and [14]. To obtain accurate device simulations for impact ionization device, simulations included all models used to describe common device behavior including both *VanOverstraetendeMan* impact-ionization and the band-to-band tunneling model, along with the band gap narrowing model, and Shockley-Read-Hall and Auger recombination at 300K and it is assumed that the avalanche coefficients of carriers near the surface are the same as the values in the bulk of the material. For mobility, doping as well as transverse-field models are considered. Table. I. enlists the various device parameters used during UTIMOS device simulations.

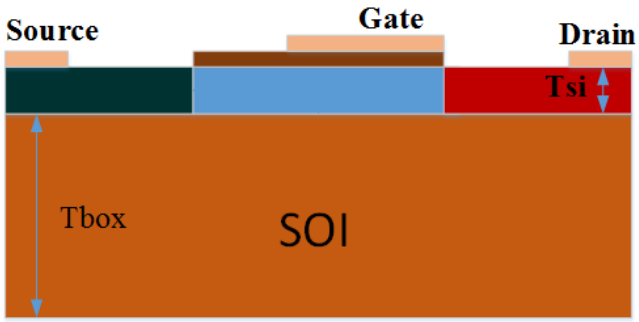

Fig.1: Structure of stimulated UTIMOS

Table 1: Parameters used for the UTIMOS simulation

Parameters	UTIMOS structure
Channel length (L_{ch})	100 nm
Gate length (L_g)	60 nm
Silicon thickness (T_{Si})	15 nm
Intrinsic length (L_{in})	40 nm
Doping N_d	10^{19} cm^{-3}
Doping N_a	10^{19} cm^{-3}
Gate thickness (t_{ox})	3 nm
Gate work-function	4.17 eV
Gate bias	0 V to 2 V

III. SIMULATION RESULTS AND DISCUSSION

III.1 n-type UTIMOS

For better analysis of UTIMOS various device performance parameters are evaluated. The biasing technique of IMOS is different from the conventional CMOS. In IMOS voltages are applied with respect to the drain.

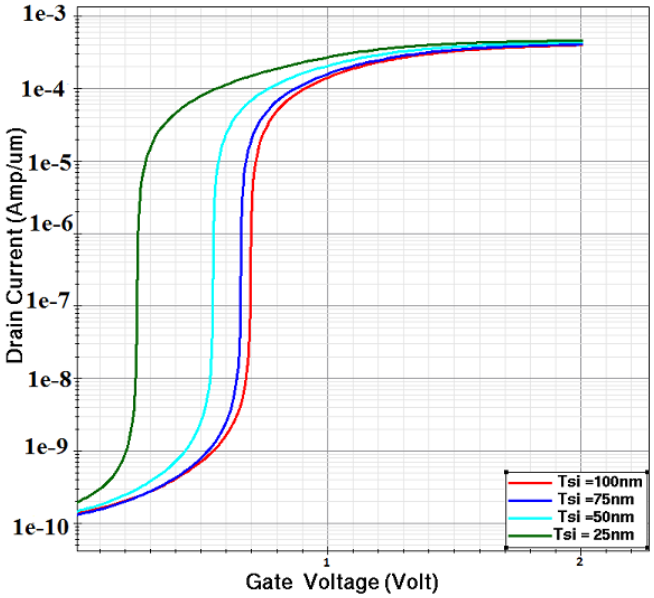

Fig. 2: I_d-V_{gd} characteristics for n-channel LIMOS as a function of the gate voltage with drain voltage V_{SD}= -7.5 V for different $T_{Si.}$

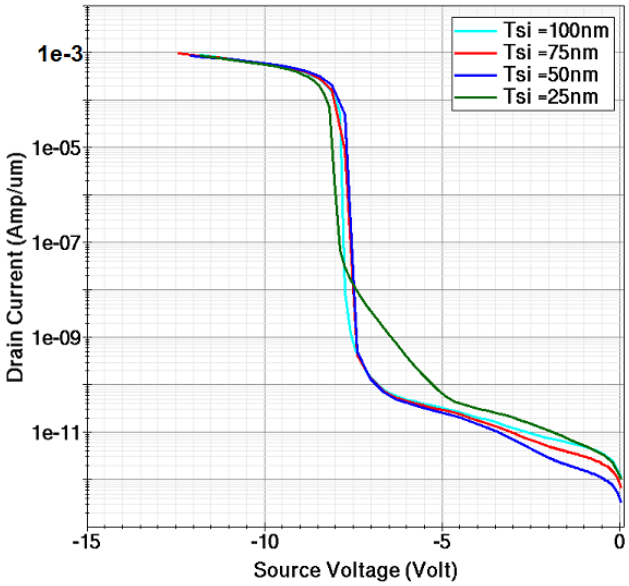

Fig. 3: I_d-V_{sd} characteristics for n-channel UTIMOS at different $T_{Si.}$

Fig. 2 shows the plot for drain current for n-channel UTIMOS as a function of the gate voltage with drain voltage V_{sd} = -7.5V for different T_{Si}. It is clearly inferred

that as the thickness of the device silicon layer T_{Si} is reduced electric field is enhanced in vertical direction and hence break down voltage V_{br} reduces for UTIMOS. In similar way, Fig. 3 shows the plot. I_d-V_{sd} characteristics for n-channel UTIMOS at different T_{Si}. It shows that the threshold voltage V_{th} reduced with the T_{Si}.

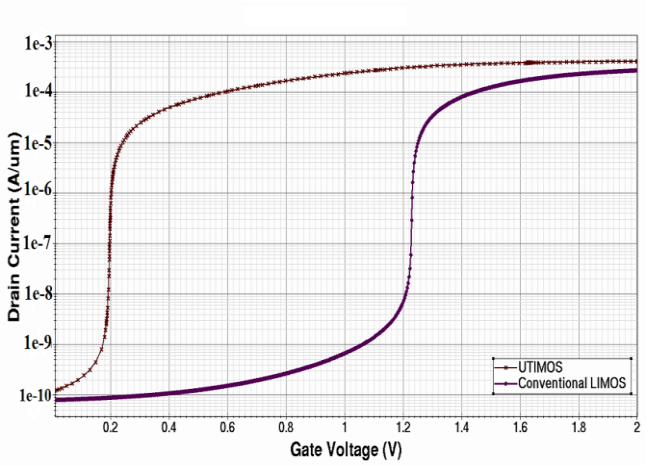

Fig. 4: I_d v/s V_{gd} characteristics for n-channel UTIMOS and conventional LIMOS.

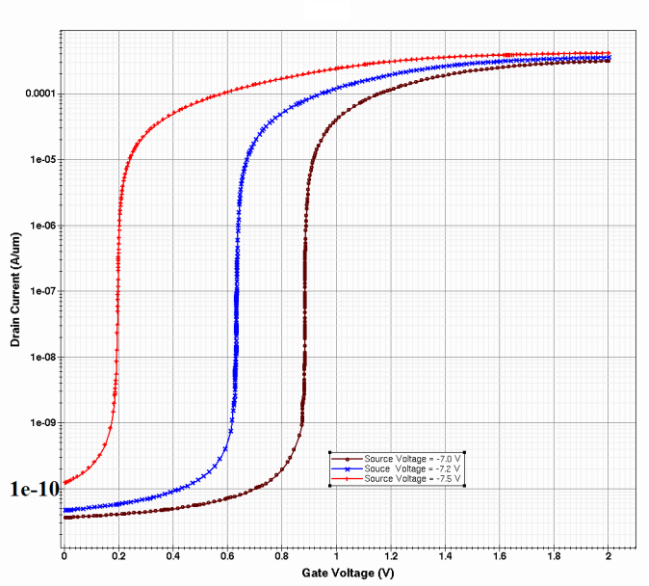

Fig. 5::I_d v/s V_{gd} characteristics for n-channel UTIMOS for different V_{sd}.

Fig 4 shows the I_d v/s V_{gs} characteristics for n-channel UTIMOS and conventional LIMOS and Fig. 5 depicts the I_d v/s V_{gs} characteristics for n-channel UTIMOS for different V_{ds}. To give in-depth analysis of the impact ionization mechanism going inside the UTIMOS various parameters as, electrostatic potential, electric field, impact ionization rate in different regions of the device, e-alpha avalanche, band-gap narrowing and current density are studied for proposed UTIMOS. As the impact ionization rate depends on the electric field in the drain side intrinsic zone. Rising the drain source voltage increases the impact ionization rate exponentially. Fig. 6 shows the electrostatic potential variation in different regions of UTIMOS and Fig. 5 shows the electrostatic potential variation with respect to the x-axis

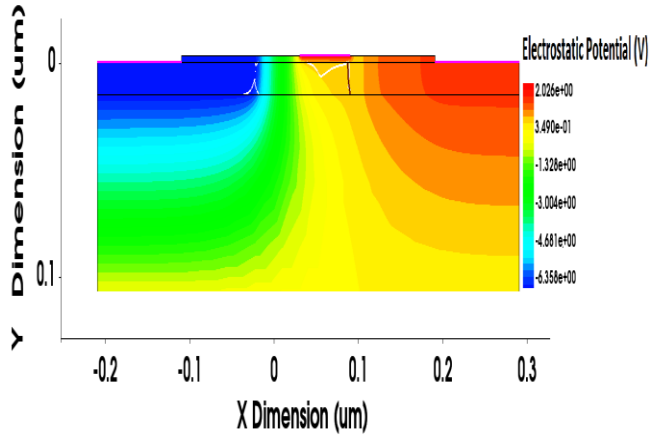

Fig. 6: Electrostatic potential variation in different regions of UTIMOS.

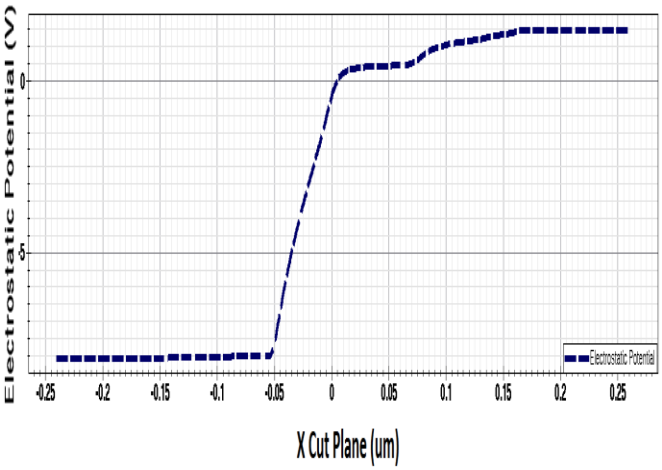

Fig. 7: Electrostatic potential variation with respect to the x-axis cut plane.

cut-plane. Both Fig. 6 and Fig. 7 illustrate that the electrostatic potential is maximum in the intrinsic region without gate overlapping area. Fig. 8 shows the electric field variation in different regions of UTIMOS. Fig 9. shows the electric field variation with respect to the x-axis cut plane. The maximum electric field occurs at x = 0, i.e., at the edge of the gate towards intrinsic side and its value is $1.0 \times 10^7 V/cm$. The potential difference between drain and source gives rise to the electric field in the drain sided intrinsic region.

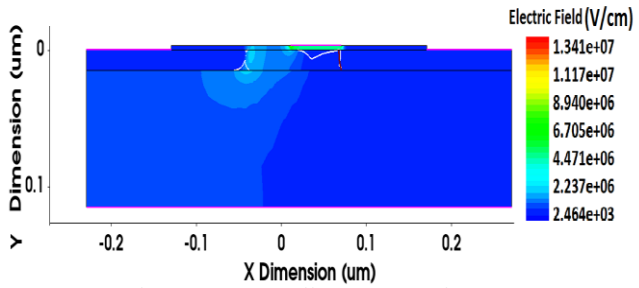

Fig. 8: Electric field variation in different regions of UTIMOS.

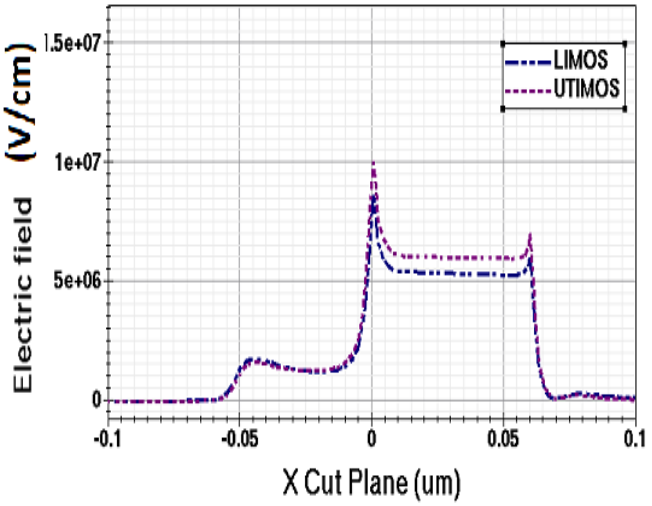

Fig. 9: lectric field variation with respect to the x-axis cut plane for LIMOS and UTIMOS.

As the drain-to-source voltage increases, this electric field can be increased until a significant impact ionization rate occurs in the drain side intrinsic zone. At this point, the electrical behavior changes to impact ionization mode and hence current is injected because of impact ionization not because of drift and diffusion.

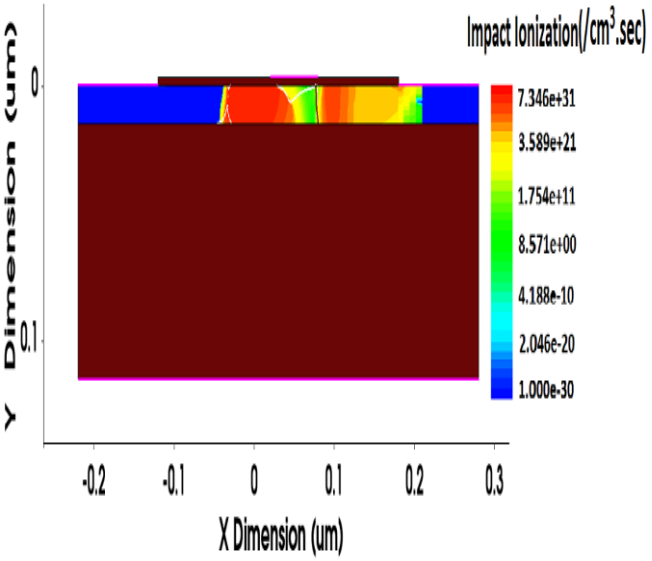

Fig. 10: Impact ionization rates in different regions of UTIMOS.

Fig. 10 shows simulated impact ionization rates in different regions of UTIMOS and it is maximum in the intrinsic region. Fig. 11 shows simulated impact ionization rates with respect to the x axis cut plane for LIMOS and UTIMOS.

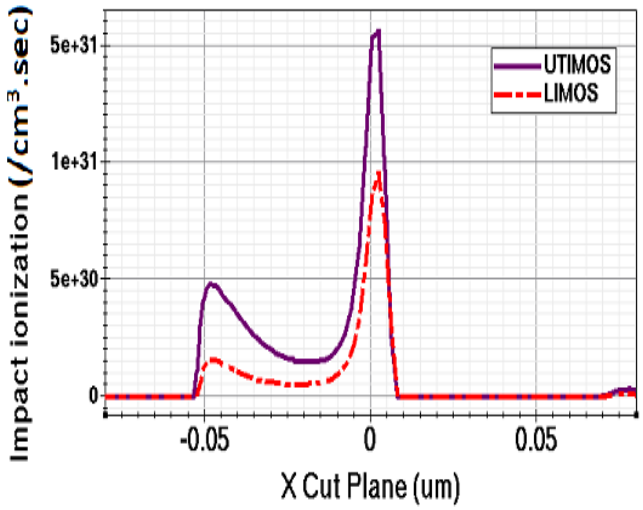

Fig. 11: Impact ionization rates with respect to the x axis cut plane for LIMOS and UTIMOS.

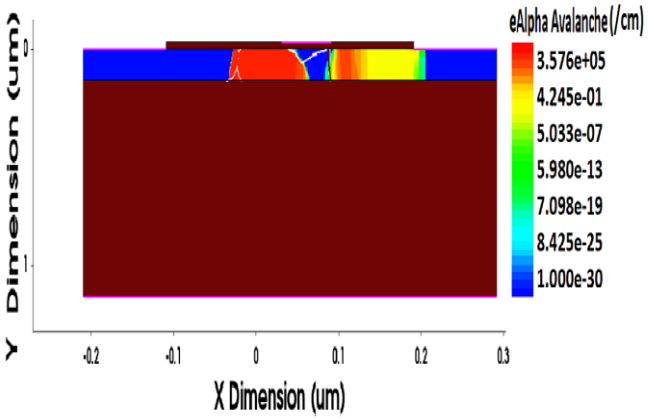

Fig. 12: E-alpha avalanche in different regions of UTIMOS.

It shows maximum value as $1.5x10^{31}cm^{-3}/s$ for UTIMOS. Fig. 12 shows e-alpha avalanche in different regions of UTIMOS and Fig. 13 illustrates the same with respect to the x axis cut plane for LIMOS and UTIMOS. E-alpha avalanche for UTIMOS is of the order of $3x10^{5}cm^{-1}$ for UTIMOS and $2.4x10^{5}cm^{-1}$ for LIMOS. Band gap narrowing in the device for UTIMOS is shown in Fig.14 and it is maximum in source and the drain regions and Fig 15. demonstrates the band gap narrowing with x-axis cut plane for both UTIMOS and LIMOS. Current density in the device for UTIMOS is shown in Fig.16 and Fig 17.demonstrate the same with x-axis cut plane for both UTIMOS and LIMOS.

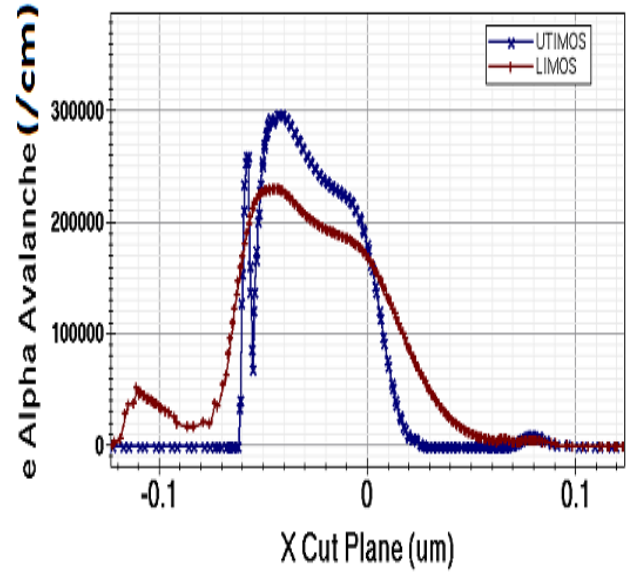

Fig. 13: E-alpha avalanche with respect to the x axis cut plane for UTIMOS
and LIMOS.

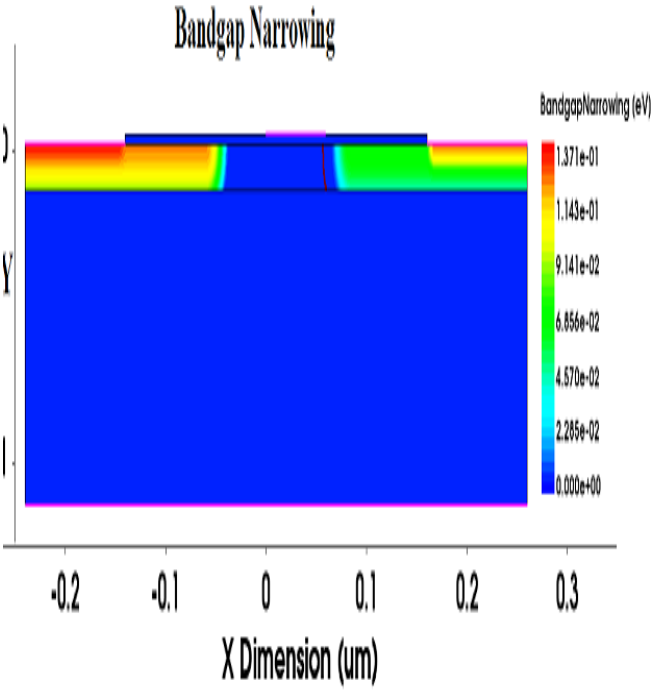

Fig. 14: Band gap narrowing in the device for UTIMOS.

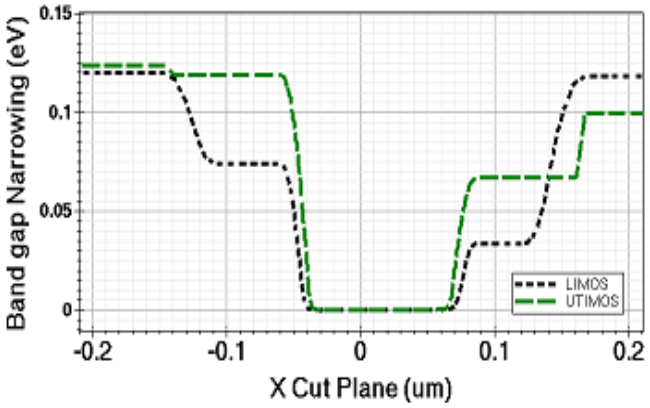

Fig. 15: Band gap narrowing with respect to the x- axis cut plane for UTIMOS and LIMOS.

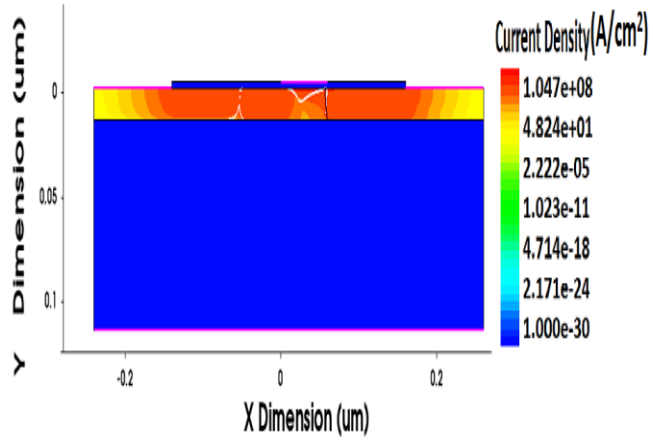

Fig. 16: Current density in the device for UTIMOS.

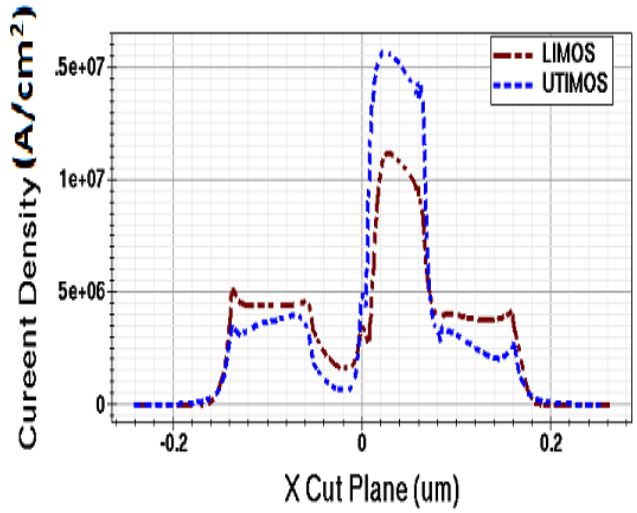

Fig. 17: Current density in the device for both UTIMOS and LIMOS

Table 2: Device performance parameters of LIMOS for T_{Si} variations

Parameters	T_{Si} =100 nm	T_{Si} =75 nm	T_{Si} =50 nm	T_{Si} =25 nm
SS (mV/dec)	3.063	3.53	2.66	2.51
V_{br} (V)	-7.75024	-7.40399	-7.4006	-7.12
DICE (mV/V)	135.5	106	74.4	51.77
GIBL (mV/V)	750	900	974	1044
V_{th}(V)	0.6768	0.6401	0.5371	0.240
I_{on}(A/µm)	$2.41x\ 10^{-4}$	$2.76x10^{-4}$	$2.95x10^{-4}$	$4.0x10^{-4}$
I_{off}(A/µm)	$1.43x10^{-10}$	$1.45x10^{-10}$	$1.50x10^{-10}$	$1.96x10^{-10}$
I_{on}/I_{off}	$1.69x10^{6}$	$1.90x10^{6}$	$1.97x10^{6}$	$2.04x10^{5}$
g_m(A/V)	$4.99x10^{-04}$	$4.95x10^{-04}$	$4.83x10^{-04}$	$4.20x10^{-04}$

III. 2 p-type UTIMOS

Structurally, one of the crucial features of IMOS is that simply the placement of the gate region with respect to the n^+ and p^+ regions changes the polarity of the device. As a result of this p-IMOS and n-IMOS can be fabricated in one run itself. Here, p-type UTIMOS simulation results have been presented. Fig. 18 shows the schematic cross-sectional view of p-type UTIMOS and Fig. 19 shows I_d v/s V_{gs} characteristics for p-channel UTIMOS. Table. III. illustrates various device performance parameters of both n-type and p-type UTIMOS.

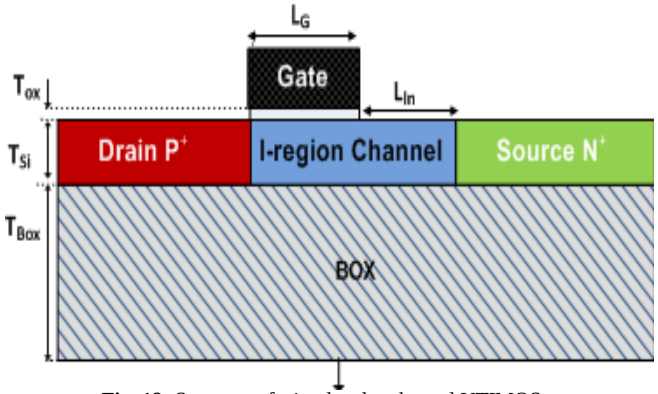

Fig. 18: Structure of stimulated p-channel UTIMOS

As there is no drain induced barrier lowering DIBL concept for the IMOS similar device parameter, i.e., drain induced current enhancement DICE is used to study this behaviour of the UTIMOS. Hence, DICE of UTIMOS corresponds to DIBL concept of conventional MOSFET. Table II Enlists various device performance parameters of UTIMOS.

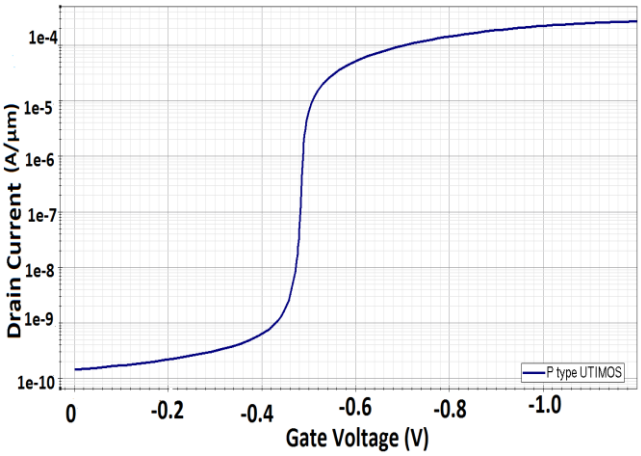

Fig. 19: I_d v/s V_{gs} characteristics for p-channel UTIMOS

Table 3: Comparison of device performance parameters between UTIMOS and LIMOS

Parameters	*n*-type UTIMOS	*p*-type UTIMOS	LIMOS
V_{br} (V)	-6.955	7.003	-7.549
V_{th} (V)	0.237	-0.472	0.692
SS (mV/dec)	1.37	2.3	3.23
I_{on}(A/µm)	$4.13x10^{-4}$	$2.55x10^{-4}$	$2.76x10^{-4}$
I_{off} (A/µm)	$1.24x10^{-10}$	$1.47x10^{-10}$	$1.64x10^{-10}$
I_{on}=I_{off}	$3.34x10^{6}$	$1.73x10^{6}$	$1.68x\ 10^{6}$
g_m (A/V)	$3.62x10^{-4}$	$4.71x10^{-4}$	$4.99x10^{-4}$
DICE (mV/V)	74.01	72.9	74.4
GIBL (mV/V)	902	913	974

IV. CONCLUSION

In this paper, we have proposed ultra-thin impact ionization MOSFET (UTIMOS) as an improved structural variant of the lateral impact ionization MOSFET. UTIMOS is having very much lower breakdown voltage hence its operating voltage is reduced to a great extent, Simulation results claimed that ultra-thin impact ionization MOSFET has much better device performance parameters as compared with the LIMOS. The smaller thickness of the device silicon layer T_{Si} leads to more intense electric field in vertical direction and hence break down voltage V_{br} reduces. This intensified vertical electric field due to reduced thickness of device silicon layer T_{Si} is the key feature of the UTIMOS. Simulation results show the sub-threshold slope SS to be 1.37mV/dec for proposed UTIMOS. It shows considerable improvement in other device performance parameters namely I_{on}, I_{off} , I_{on}/I_{off} ratio, threshold voltage V_{th}, breakdown voltage V_{br}, drain induced current enhancement DICE, and gate induced barrier lowering GIBL.

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