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DESIGN OF 20 nm FinFET STRUCTURE WITH ROUND FIN CORNERS USING SIDE SURFACE SLOPE VARIATION

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ABSTRACT

FinFET transistors have emerged as novel devices having superior controls over short channel effects (SCE) than the conventional MOS transistor devices. However, FinFET exhibit certain undesirable characteristics such as corner effects, quantum effects, tunneling etc. Usually, the corner effect deteriorates the performance by increasing the leakage current. In this work, the corner effect of Tri-gate bulk FinFETs are investigated by 3D Process and device simulation and their electrical characteristics are compared for different bias conditions. Finally the optimum design of bulk FinFETs are achieved with 3-D device simulation under changing slope of Fin.

Keywords: Short channel effect**(**SCE), narrow width effect(NWE), Corner effect, Tri gate-FinFET, Premature inversion, Quantum Effect, round and tapered shaped Fin structure, DIBL, GIDL.

I. INTRODUCTION

As CMOS technology is continually scaling, a transition from conventional planar MOSFETs to FinFET structure [1] is designed for 22 nm and 14 nm technology nodes with improved subthreshold performances. In the Tri-Gates Vth and I_{OFF} are affected by overlapping Top and Side Gate electric fields at the Tri-Gate corner. The presence of charge sharing effect between two adjacent gates causes the premature inversion in the corners (Fig.1). The corners present leads to the formation of independent channels with different threshold voltages. This phenomenon is known as corner effect and it needs to be suppressed by additional corner implantation and/or corner rounding [2-3]. Corner implantation uses the fin formation hard mask and allows a retarget of Tri-Gate threshold voltage independent of the halo implantation shared with the planar MOSFETs. The radius of curvature of the corners has a significant impact on the device electrical characteristics and can decide whether or not a different threshold voltage will be measured at the corners and at the planar interfaces of the device [1]. So, Corner rounding erases electric field overlapping of Top- and Side-Gate and permits a homogenous transition between Top- and Side-Channel [3].

To consider the electric field focusing in the corner region, we introduced a corner factor α_c to take into account the effect in the $V_{th,c}$ model[4]. The value of α_c normally 0.25 and had no dependence on the corner shape, body geometry, and body doping. After the correction, α_c is extracted to 0.4 regardless of the corner shape. We can express $V_{th,c}$ of bulk FinFET with corner correction factor α_c [4]as follows:

$$V_{th,c} = V_{FB} + 2\psi'_B + \frac{q x_{dep} N_b \alpha_c}{C_{ox}} \left(1 - \frac{2x_h}{3L_c}\right) . \qquad (1)$$

where V_{FB} and $2\psi'_B$ are the flat-band voltage and effective surface potential(including SCE, NWE and 3-D Charge sharing effect), respectively. N_b, x_{dep}, and C_{ox} are the body doping, channel depletion width under the gate, and gate capacitance, respectively. x_h is a fitting parameter to represent the charge-sharing length at the source-side (or drain-side) and is used to reflect the SCE.

Several techniques are used to optimize FinFET structures to improve I_{on}/I_{off} performances [5-6]. Here, Corner rounding also allows to suppress corner leakage path with improve I_{on}-I_{off} performance and reduces the side wall area with reduced the gate capacitance leading to the reduction in intrinsic delay. The DC and transient analysis of

CMOS inverter using Conventional(C)- SOI FinFET and Partially Cylindrical (PC)-FinFET have been done which shows that PC-FinFET inverter has reduced propagation delay as compared to C-FinFET [7]
The three-dimensional simulation for 20 nm NMOS and PMOS FinFETs have major focus on rounded fin corners, tapered fin shape with several different slopes, impact of fin shape on FinFET channel stress and I–V characteristics (Fig 2). The FinFET structure with a 5 nm top width and 15 nm bottom width is also presented in [8]. A 22 nm node FinFET technology for mass production has been demonstrated in [9], which exhibits higher performance than planar MOSFETs, especially in terms of the tight gate control (improved short-channel effects and steep subthreshold slopes). This type of structure can further optimize the performances of Bulk FinFET which are comparable to the performance of SOI FinFET proposed in different researches [10].

II. DEVICE STRUCTURE AND DIMENSIONS

The Bulk and SOI FinFET structures have been made with 3-D Sentaurus structure editor [11-12]. The tri-gate FinFET designed is of 20nm channel length with source/drain doping is $2.0X10^{20}$ cm^{-3} (n type) and Channel doping $2.0X10^{18}$ cm^{-3}. Metal is used as gate contact material with work function of metal is kept 4.62eV. The Physical thickness of the gate insulator(Tox) is 0.0023 μm(Hfo2 thickness = 0.0017 μm, interlayer oxide thickness = 0.0006 μm). The FinFET is designed with 10nm spacer length and 32nm gate thickness.

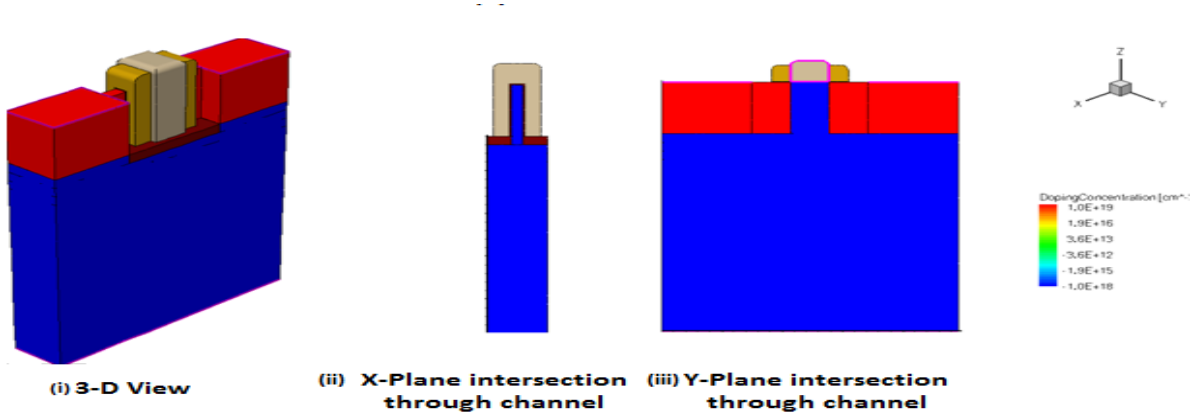


Fig.1: 3-D Conventional bulk FinFET Structure(without corner rounding)

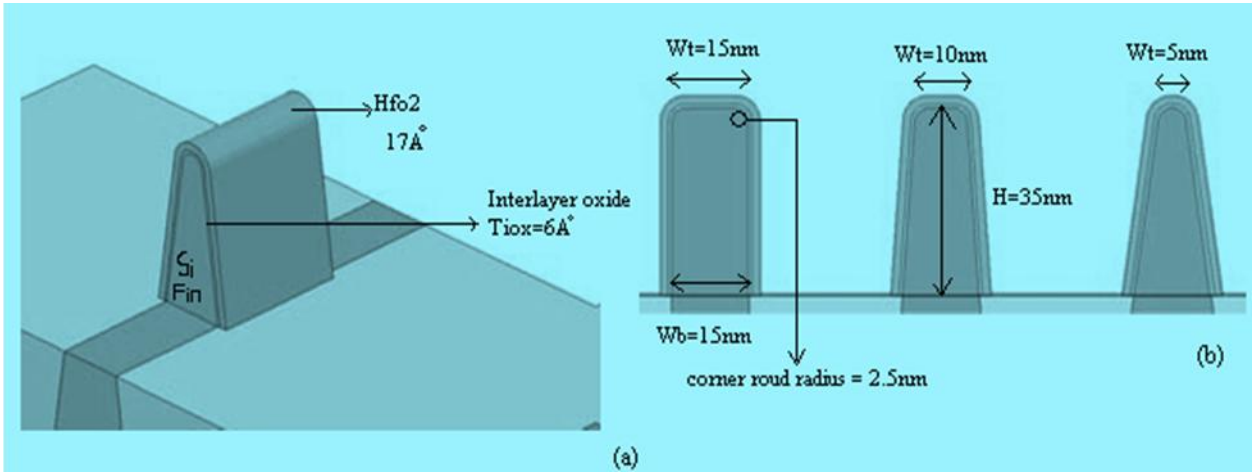


Fig.2: (a) Cross-sectional view of rounded corner FinFET structure for 3-D device simulation (b) Fin structure showing the variation in top fin width (W_{top})

The 3-D simulation of FinFET structure is performed for 20nm channel length with 0.035 μm Fin height, 20nm bottom Fin width and top Fin width varied over range between 5 nm to 15 nm. All the dimensions are same for both NFinFET and PFinFET.

III. SIMULATION RESULTS

Figure 3 shows the I–V simulation results of the FinFET with a 5 nm top width, where the work function of the metal gate is assumed to be 4.62 eV (midgap workfunction). It is shown that the drain-induced barrier lowering (DIBL) of the NFinFET is larger than that of the PFinFET. GIDL (Gate induced drain lowering) currents are observed in both the PFinFET and NFinFET. Band-to band tunneling generation due to GIDL is shown to be dominant at the fin top. Gate leakage currents are suppressed by the high-k dielectric.
Fig. 4 shows the results of the subthreshold slope as a function of the top fin width for the PFinFET and NFinFET. The subthreshold slopes of the NFinFETs are larger than those of the PFinFETs, in agreement with the DIBL results. The main reason for the NMOS DIBL being higher than the PMOS DIBL is that the quantum separation of the NFinFET is larger than that of the PFinFET which reduces gate control and, therefore, increases DIBL.

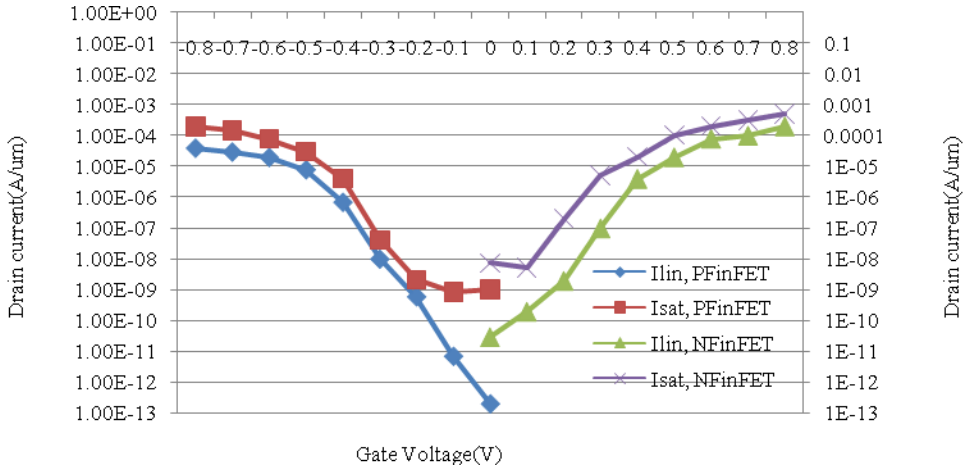


Fig.3: Id–Vg characteristics for NFinFET and PFinFET (Top Fin Width = 5nm)

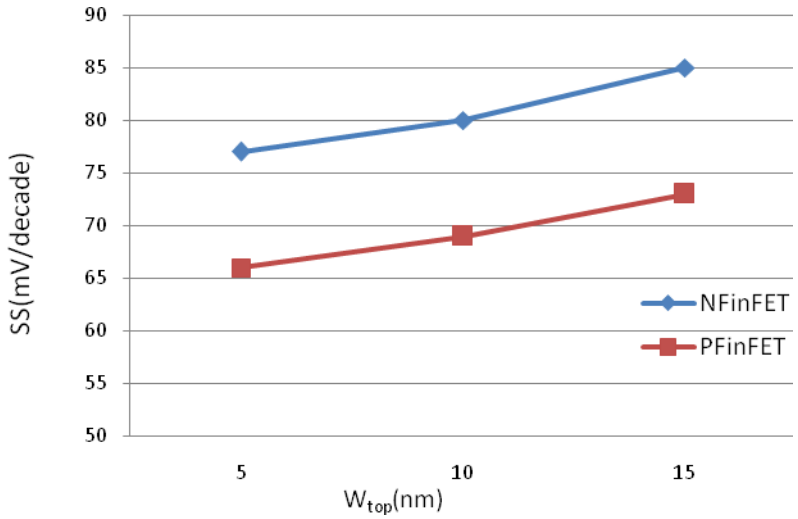
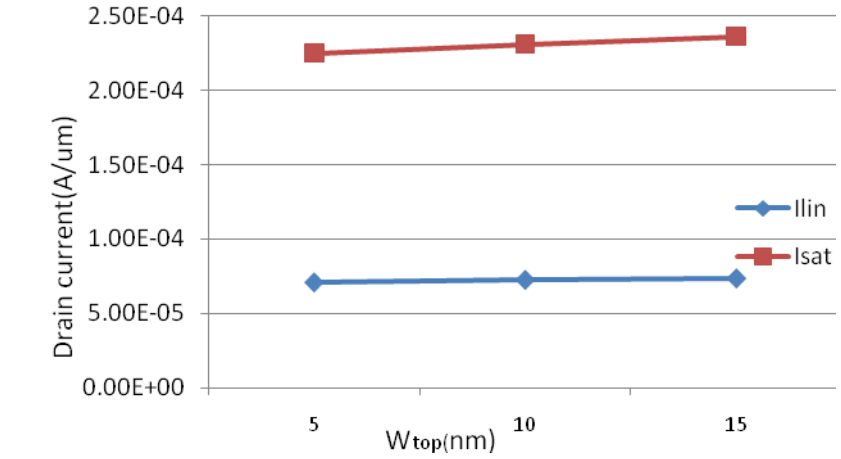
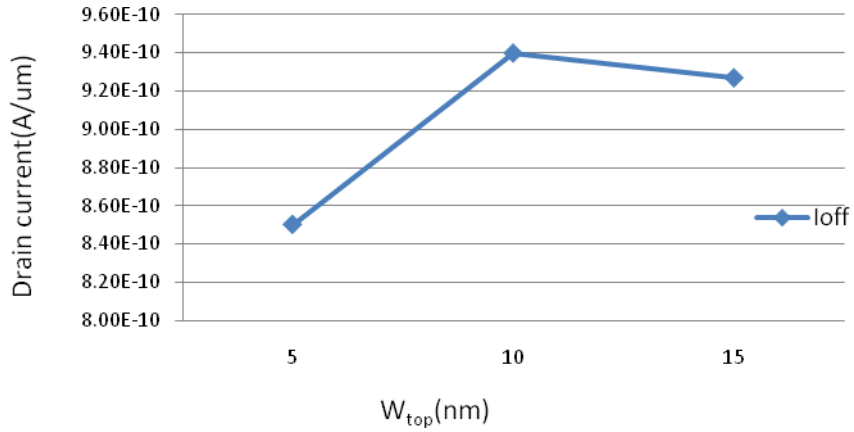


Fig.4: Side-surface slope impacts subthreshold slope

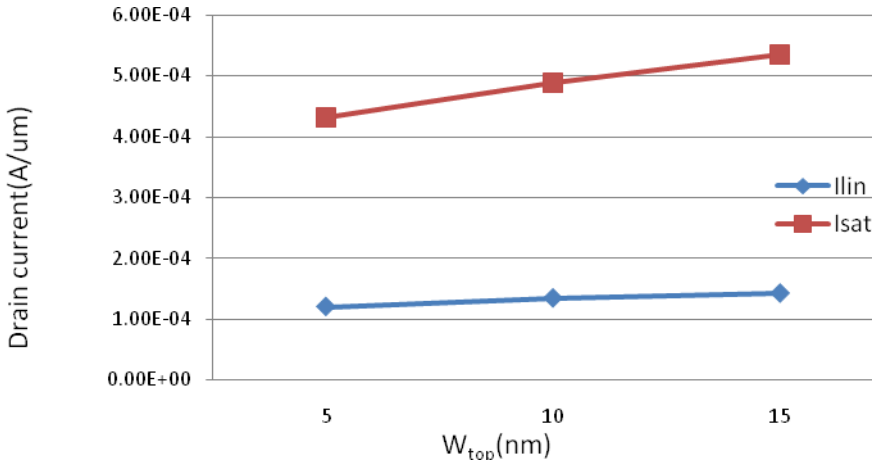


(a)

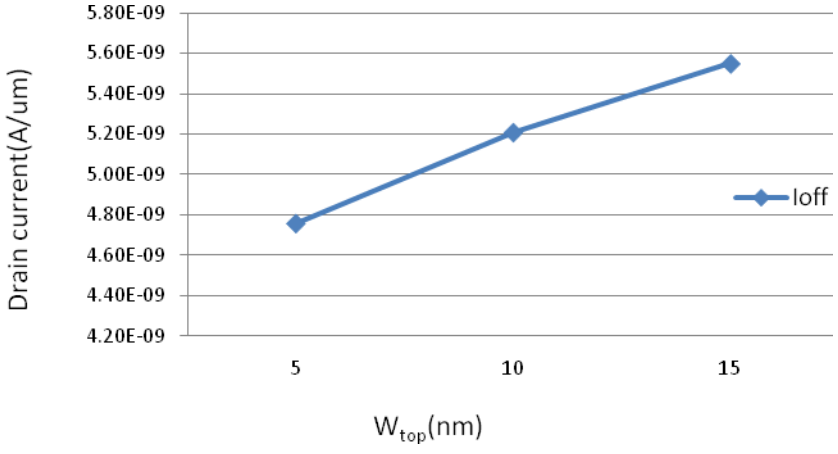


(b)

Fig. 5 Side-surface slope impacts I–V performance of NFinFET **(a)** I_{lin}/I_{sat}, **(b)** I_{off} for different W_{top}



(a)



(b)

Fig. 6: Side-surface slope impacts I–V performance of PFinFET **(a)** I_{lin}/I_{sat} **(b)** I_{off} for different W_{top}

Fig. 5 and Fig. 6 show the results of the on-current, linear current, and off-current as a function of the top fin width for the NFinFET and PFinFET. In both FinFETs, as the top fin width becomes wider, the on-current becomes higher due to the increased fin area. For the NFinFET, the larger subthreshold-slope variation leads to the larger on-current variation.

Further the simulations are done, keeping different work functions of NFinFET and PFinFET for a particular off current. The on current of the PFinFET is 66μmA/um and the on-current of the NFinFET is 1.02 mA/μm. after normalizing the off current to a fixed value 100nA/μm by the workfunction adjustment for NFinFET and PFinFET 4.32 eV and 4.93 eV respectively. The subthreshold slope (SS) is 74 mV/decade for NFinFET and 67 mV/decade for PFinFET by normalizing off current which is nearer to the ideal values with top fin width 5 nm.

IV. CONCLUSIONS

The mobile carrier density of tri gate FinFET is higher in the corner than the other portions of the channels. Also, now the corner regions are comparable with the planar surface channel region in small dimension devices. A larger part of the current is carried by the corners, so, the corners are in a position to switch on the device. As dimensions are decreasing the effect of corner role on on-state current is increasing and also we have observed that the electron density distributions at the corners are higher compared to the other portion of the channel. For the same channel length we can optimize the top fin size for desirable on and off sate performance with the change in shape of Fin from round shape corner to tapered shape Fin. This shows that the scalability of FinFET can be enhanced under desirable on and off state performance with proposed FinFET structures.

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