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ANALYTICAL MODELING OF VOLUME INVERSION AND CHANNEL LENGTH MODULATION IN FULLY DEPLETED DOUBLE GATE NANOSCALE SOI MOSFETs

Rajiv Sharma

Department of Electronics and Communication Engineering, Vaish College of Engineering, Rohtak, Haryana, India.
rsap70@rediffmail.com

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ABSTRACT

In this paper, surface potential sensitivity to channel length scaling for Fully Depleted Double Gate Nanoscale SOI MOSFETs is comprehensively investigated. Analytical expression for centre potential is then obtained whereby the key effect of volume inversion taking place for the modeled device leading to increase in mobility is illustrated. Variation of drain current with variation in process parameters like width and temperature and variation of tranconductance with temperature as a parameter is investigated. This work also includes modeling of transit time, which is one of the main figures of merits for analog/rf performance for Double Gate Fully Depleted Nanoscale SOI MOSFETs. Lastly, behavior of the modeled device in terms of mobility is investigated by varying the thickness of silicon film and gate oxide thickness through simulation carried out on 2D ATLAS device simulator.

Keywords: Fully depleted, DG-SOI MOSFET, Green’s function, Volume Inversion, ATLAS Simulator.

I. INTRODUCTION

Double Gate MOSFET is one of the most promising architecture for scaling CMOS devices down to nano scale regime [1], since they allow significant reduction of short channel effects such as threshold voltage roll off, drain induced barrier lowering (DIBL) and subthreshold slope degradation compared to planar single gate MOSFETs [2-4]. As compared to bulk silicon, the architecture of DG SOI MOSFET is more flexible because more parameters such as thickness of Si film, front and back gate oxide thickness, substrate doping, drain to source voltage can be used for optimization. It is well known that short channel effects are reduced in ultra thin SOI films. A direct application of these extremely thin films is DG MOSFET, which make use of volume inversion concept formulated [5]. A number of compact and analytical models for DG MOSFETs that account for quantum, volume inversion, short-channel and non static effects have been proposed [6-7]. Due to excellent control of potential, it is admitted that DG MOSFETs will presumably represent the final stages of Si microelectronic devices [8-10].

Starting from base formulation, our work in this paper is focused on investigation of front and back surface potential sensitivity to channel length. Recently, authors have developed a 2D analytical drain current model for symmetric double gate fully depleted nanoscale SOI MOSFETs [11]. In this paper, device performance parameters such as drain current, transconductance and transit time are investigated with respect to variation in process parameters

such as temperature, channel width, channel doping and gate oxide thickness. Finally, this work is concluded by showing the benefits of volume inversion evaluated in terms of effective mobility.

II. MODEL FORMULATION

The structure of Double Gate Fully Depleted Nanoscale SOI MOSFET used for our analysis and simulation is shown in Fig. 1.

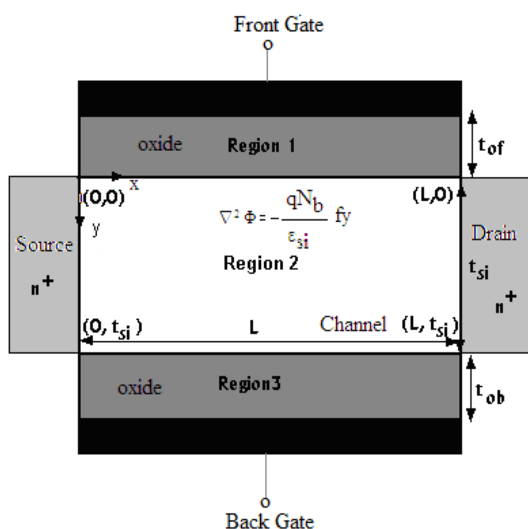

Fig. 1: Schematic Diagram of a Fully Depleted Double Gate Nano Scale SOI MOSFET

where L is channel length, N_b is doping in the silicon film, q is the electronic charge, ε_{si} is dielectric permittivity of silicon, t_{si} is thickness of silicon film and t_{of}/t_{ob} is front/back gate oxide thickness.

The two dimensional Poisson's equation is given as:

$$\nabla^2\phi(x,y) = \frac{\partial^2\phi(x,y)}{\partial x^2} + \frac{\partial^2\phi(x,y)}{\partial y^2} = -\frac{\rho(x,y)}{\varepsilon} \quad (1)$$

where $\phi(x,y)$ is the 2D potential distribution, ρ is 2D space charge density distribution and ε is the dielectric permittivity. In recently developed model by authors for Double Gate Fully Depleted Nanoscale SOI MOSFET device , Green's function solution technique has been adopted to solve 2D Poisson's equation using Dirichlet's and Newman's boundary condition at silicon-silicon di-oxide interface [12]. Substituting the Green's function solution into the Green's theorem, 2D potential distribution in region 2 [12] is

$$\phi_S(x,y) = \frac{-qN_b}{\varepsilon_{si}} x(L-x) + V_{bi} + \frac{x}{L}V_{ds} - \sum_{m=1}^{\infty} \frac{\sin\left(\frac{m\pi}{L}x\right)}{\varepsilon_{si}\left(\frac{m\pi}{L}\right)\sinh\left(\frac{m\pi}{L}t_{si}\right)} \times \left[D_{sf}\cosh\left[\frac{m\pi}{L}(t_{si}-y)\right] - D_{sb}\cosh\left(\frac{m\pi}{L}y\right)\right] \quad (2)$$

where V_{ds} is drain to source voltage, V_{bi} is built in potential. D_{sf} is Fourier coefficient of electric displacement at front interface and D_{sb} is Fourier coefficient of electric displacement at back interface [12]

Surface potential distribution at front interface $\phi_{S1}(x)$ is obtained by replacing y = 0 in eq. (2)

$$\phi_{S1}(x,y) = \frac{-qN_b}{\varepsilon_{si}} x(L-x) + V_{bi} + \frac{x}{L}V_{ds} - \sum_{m=1}^{\infty} \frac{\sin\left(\frac{m\pi}{L}x\right)}{\varepsilon_{si}\left(\frac{m\pi}{L}\right)\sinh\left(\frac{m\pi}{L}t_{si}\right)} \times \left[D_{sf}\cosh\left[\frac{m\pi}{L}(t_{si})\right] - D_{sb}\right]. \quad (3)$$

Similarly, the surface potential distribution

at back interface $\phi_{S2}(x)$ is obtained by replacing y = t_{si} in eq. (2)

$$\phi_{S2}(x,y)=\frac{-qN_b}{\varepsilon_{si}}x(L-x)+V_{bi}+\frac{x}{L}V_{ds}-\sum_{m=1}^{\infty}\frac{\sin\left(\frac{m\pi}{L}x\right)}{\varepsilon_{si}\left(\frac{m\pi}{L}\right)\sinh\left(\frac{m\pi}{L}t_{si}\right)}\times\left[D_{sf}-D_{sb}\cosh\left(\frac{m\pi}{L}t_{si}\right)\right] \quad (4)$$

DG MOSFETs operate in two distinct modes, namely surface inversion (exactly in case of bulk MOSFETs) and volume inversion. In volume inversion front and back channel merge in to occupying whole Si region. When charge is close to the centre of silicon layer, electrons are less affected for scattering mechanisms like roughness scattering, remote scattering (both remote roughness scattering and coulomb scattering) [12,13]. Thus in this mode of operation, carrier no. and mobility are increased and as a result performance improves significantly.

Relation between potential at surface $\phi_S(x)$ and at the centre $\phi_c(x)$ of SOI film [15] is given as

$$\phi_s(x)=\frac{1}{1+H}(\phi_c(x)+HV'_{gs}) \quad (5)$$

where $H=\varepsilon_{ox}t_{si}/4\varepsilon_{si}t_{ox}$

and $V'_{gs}=V_{gs}-V_{fb,f}$

V_{gs} is gate to source voltage, $V_{fb,f}$ is flat band voltage of the front gate, ε_{ox} is dielectric permittivity of oxide and t_{si} is thickness of silicon film. From equation (5), potential at centre of channel $\phi_c(x)$ in terms of front surface potential $\phi_{S1}(x)$ is given by

$$\phi_c(x)=(H+1)\phi_{S1}(x)-HV'_{gs}\ . \quad (6)$$

Substituting for front surface potential $\phi_{S1}(x)$ from eq. (3) in eq. (6), we have

$$\phi_c(x)=(H+1)\left(\begin{array}{l}\frac{-qN_b}{\varepsilon_{si}}x(L-x)+V_{bi}+\frac{x}{L}V_{ds}\\ -\sum_{m=1}^{\infty}\frac{\sin\left(\frac{m\pi}{L}x\right)}{\varepsilon_{si}\left(\frac{m\pi}{L}\right)\sinh\left(\frac{m\pi}{L}t_{si}\right)}\\ \times\left[D_{sf}\cosh\left[\frac{m\pi}{L}t_{si}\right]-D_{sb}\right]\end{array}\right)-HV'_{gs} \quad (7)$$

$$=(H+1)\left(a-b\times c\right)-HV'_{gs}\ . \quad (8)$$

Similarly, using eq. (5), relation between potential at centre of channel $\phi_c(x)$ and back surface potential $\phi_{S2}(x)$ is given by

$$\phi_c(x)=(H+1)\phi_{S2}(x)-HV'_{gs}\ . \quad (9)$$

Substituting for $\phi_{S2}(x)$ from eq. (4) in eq. (9), we have

$$\phi_c(x)=(H+1)\left(\begin{array}{l}\frac{-qN_b}{\varepsilon_{si}}x(L-x)+V_{bi}+\frac{x}{L}V_{ds}\\ -\sum_{m=1}^{\infty}\frac{\sin\left(\frac{m\pi}{L}x\right)}{\varepsilon_{si}\left(\frac{m\pi}{L}\right)\sinh\left(\frac{m\pi}{L}t_{si}\right)}\\ \times\left[D_{sf}-D_{sb}\cosh\left(\frac{m\pi}{L}t_{si}\right)\right]\end{array}\right)-HV'_{gs} \quad (10)$$

$$= (H+1)(a - b \times d) - HV'_{gs} \quad (11)$$

with $a = \frac{-q.N_b}{(\varepsilon_{si})} x(L-x) + V_{bi} + \frac{x}{L} V_{ds}$,

$$b = \sum_{m=1}^{\infty} \frac{\sin\left(\frac{m.\pi}{L} x\right)}{\varepsilon_{si}\left(\frac{m\pi}{L}\right)\sinh\left(\frac{m\pi}{L} t_{si}\right)} ,$$

$$c = D_{sf} \cosh\left(\frac{m\pi}{L} t_{si}\right) - D_{sb}$$

and $d = D_{sf} - D_{sb} \cosh\left(\frac{m\pi}{L} t_{si}\right)$.

The mobility of electrons $\mu_n(x)$ is given as

$$\mu_n(x) = \frac{\mu_{no}}{\left[1 + \left(\frac{E(x)}{E_c}\right)^2\right]^{1/2}} \quad (12)$$

where μ_{no} is low field mobility [16]

E_c is critical field given by

$$E_c = 6.01 \times 10^2 T^{3/2} \quad (13)$$

$E(x)$ is the longitudinal field given by

$$E(x) = \frac{C_{ox}\left(V_{fb,f} - V_{gs} + \phi_c(x)\right)}{\varepsilon_{si}} \quad (14)$$

where C_{ox} is oxide layer capacitance and is given by $C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$.

Substituting for V'_{gs} and $\phi_c(x)$ in eq. (14), we have

$$E(x) = \frac{C_{ox}\left(-V'_{gs} + \{\phi_s(x)(1+H) - HV'_{gs}\}\right)}{\varepsilon_{si}}$$

$$= \frac{C_{ox}(H+1)\left(\phi_s(x) - V'_{gs}\right)}{\varepsilon_{si}} \quad . \quad (15)$$

Substituting for $E(x)$ from eq. (15) in eq. (12), the mobility of electrons at front surface $\mu_{n1}(x)$ is given as

$$\mu_{n1}(x) = \frac{\mu_{no}}{\left[1 + \left(\frac{E_c(C_{ox}(H+1)\phi_{s1}(x) - V'_{gs})}{\varepsilon_{si}}\right)^2\right]^{1/2}} \quad (16)$$

Similarly, the mobility of electrons at back Si-SiO$_2$ interface $\mu_{n2}(x)$ is obtained as

$$\mu_{n2}(x) = \frac{\mu_{no}}{\left[1 + \left(\frac{E_c(C_{ox}(H+1)\phi_{s2}(x) - V'_{gs})}{\varepsilon_{si}}\right)^2\right]^{1/2}} \quad (17)$$

The expression for drain current for the modeled device [11] is

$$I_{DS} = \int \frac{T3 \cdot [T4\left(\phi_S(x) - V'_{gs}\right) - T1 \cdot \sqrt{\phi_s(x)}]}{\left[1 + T2 \cdot \left(\phi_S(x) - V'_{gs}\right)^2\right]^{1/2}} \cdot d\phi_S(x) \quad (18)$$

where I_{DS} is current in the channel $0 \le x \le L$, $\phi_S(x)$ is surface potential and T1, T2, T3 and T4 are defined elsewhere [11] and are rewritten as

$T1 = \sqrt{2 \cdot q \cdot N_b \cdot \varepsilon_{si}}$, $T2 = \frac{C_{ox}{}^2 (1+H)^2}{\varepsilon_{si}{}^2 \cdot E_c{}^2}$

$$T3 = \frac{2 \cdot W \cdot \mu_{no} \cdot (1+H)}{L}$$

and $T4 = C_{ox} \cdot (1+H)$.

Recently, authors have carried out analytical analysis of cut-off frequency for symmetric Double Gate Fully Depleted Nanoscale SOI MOSFET [11]. Cut off frequency (f_T) is calculated using the relation

$$f_T = \frac{g_m}{2 \cdot \pi \cdot L \cdot W \cdot C_T} \quad (19)$$

where g_m is transconductance, L is channel length, W is channel width and C_T is device capacitance [11].

Cut-off frequency f_T is one of the important figures of merit of low-voltage and high speed devices. The expression for Cut off frequency (f_T) for the modeled device [11] is rewritten as

$$f_T = -\frac{T3\cdot T4}{\sqrt{T2}}\left[\frac{\sec\theta_2\cdot\tan\theta_2\cdot\left(\sqrt{T2}\right)}{[1+T2\cdot\left(V_{bi}+V_{ds}-V'_{gs}\right)^2]} - \frac{\sec\theta_1\cdot\tan\theta_1\cdot\left(\sqrt{T2}\right)}{[1+T2\cdot\left(V_{bi}-V'_{gs}\right)^2]}\right]$$
$$+\frac{T1\cdot T3}{T2}\cdot\left(-\sqrt{T2}\right) \times\left[\frac{\sec\theta_2\cdot\tan\theta_2}{\left(1+T2\cdot\left(V_{bi}+V_{ds}-V'_{gs}\right)^2\right)} - \frac{\sec\theta_1\cdot\tan\theta_1}{\left(1+T2\cdot\left(V_{bi}-V'_{gs}\right)^2\right)}\right]$$
$$+\frac{T1\cdot T3}{\sqrt{T2}}\left[\begin{array}{l}\ln(\sec\theta_2+\tan\theta_2)\\ -\ln(\sec\theta_1+\tan\theta_1)\end{array}\right]$$
$$+\frac{T1\cdot T3}{\sqrt{T2}}\cdot V'_{gs}\cdot\left(-T2\right)\left[\frac{\sec\theta_2}{\left(1+T2\cdot\left(V_{bi}+V_{ds}-V'_{gs}\right)^2\right)} - \frac{\sec\theta_1}{\left(1+T2\cdot\left(V_{bi}+V_{ds}-V'_{gs}\right)^2\right)}\right]$$
$$\times\frac{1}{2\cdot\pi\cdot L\cdot W\cdot C_T} \quad . \tag{20}$$

In this paper, work is extended to model transit time (τ). The transit time is the device static parameter to measure speed of the device. There are two limits in the speed of a double-gate SOI-MOSFET. First, a basic limit is set by the time for charge transport along the channel. Secondly, the charging of capacitances in the device imposes a limit on the minimum transit time. The transit time (τ) of a double gate SOI-MOSFET is inverse of cut-off frequency (f_T) and can be written as

$$\tau = \frac{1}{f_T} \quad . \tag{21}$$

III. RESULTS AND DISCUSSION

The simulated device structure is a symmetric double gate fully depleted SOI MOSFET with source/drain regions doped at 10^{20} m^{-3}, a lightly doped p-type channel with doping levels of SOI layer equal to 10^{17} m^{-3}. The channel length is 65nm, channel width is 130nm, source/drain lengths are 10nm, the top and bottom gate oxide thickness are $t_{of} = t_{ob} = t_{ox} = 1.5nm$. The silicon layer thickness t_{si} of the simulated double gate SOI MOSFET device is 10nm. The metal gate work function is 4.25 eV. Same gate voltage V_{gs} is applied to both the gates. Low field mobility (μ_{no}) is $750 cm^2/Vs$ and unless specified, all simulations has been done at room temperature i.e. at T=300 K.

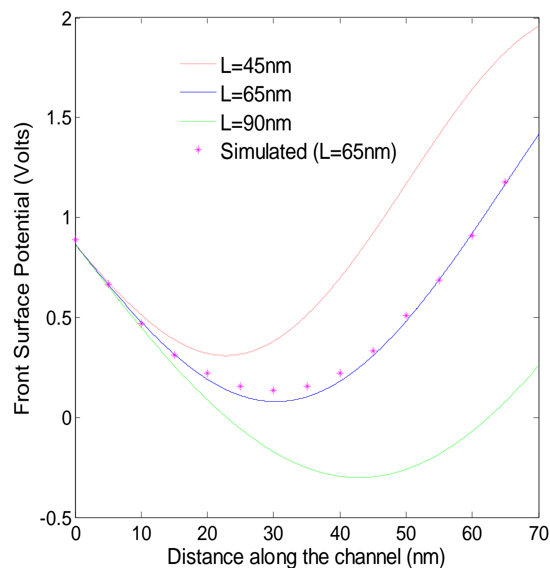

Fig. 2: Variation of front surface potential along channel of a symmetric double gate fully depleted nanoscale SOI MOSFET with different values of channel length. N_b = $1\text{x}10^{17}m^{-3}$, $t_{of} = t_{ob} = 1.5$nm, $t_{si} = 10nm$, V_{ds} = 0.3V, V_{gs} = 0.3V, $V_{fb,f}$ = $V_{fb,b}$= -0.26V, V_{bi} = 0.868V.

Figure 2 shows the variation of front surface potential as a function of distance along the channel with channel length as a parameter. The expansion of space charge region around the source and drain junctions depends strongly on device dimensions. Contribution of the space charge regions around the source and drain junctions becomes significant in short channel devices. As channel length decreases, depletion regions in the channel due to gate overlap with the depletion regions due to source/drain junctions. Due to overlapping of the fields, the effective gate controlled charge becomes smaller. In other words, charge sharing results in a decrease in effective area of device to be depleted which can be seen as rise in channel potential. Rise in channel potential due to shortening of channel is due to channel length modulation.

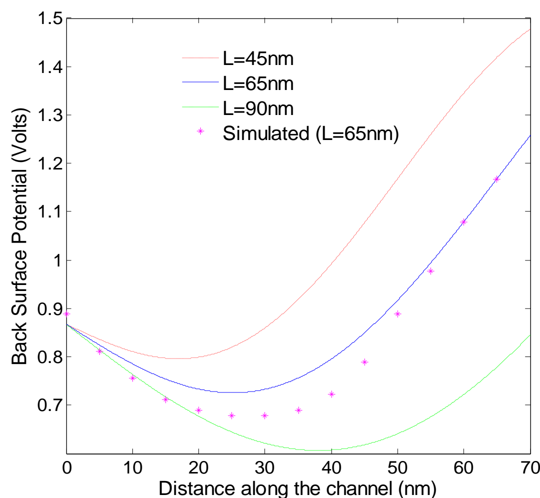

Fig. 3: Variation of back surface potential along channel of a symmetric double gate fully depleted nanoscale SOI MOSFET with different values of channel length. N_b = 1x10^{17}m^{-3}, $t_{of} = t_{ob} =$1.5nm, $t_{si} = 10nm$, V_{ds} = 0.3V, V_{gs} = 0.3V, ,$V_{fb,f}$ = $V_{fb,b}$= -0.26V, V_{bi} = 0.868V.

The variation of back surface potential as a function of distance along the channel with channel length as a parameter is shown in Fig. 3. The expansion of space charge region around the source and drain junctions depends strongly on channel length. As channel length decreases, contribution of the space charge regions becomes significant. In nanoscale devices, a significant portion of total depletion charge under the gate is actually due to source and drain junction depletion, rather than bulk depletion charge induced by gate voltage. This results in lowering of potential barrier and drop in threshold voltage is observed. It can therefore be concluded that decrease in channel length results in a decrease in effective area of device to be depleted leading to rise in channel potential. Rise in channel potential due to shortening of channel is due to channel length modulation.

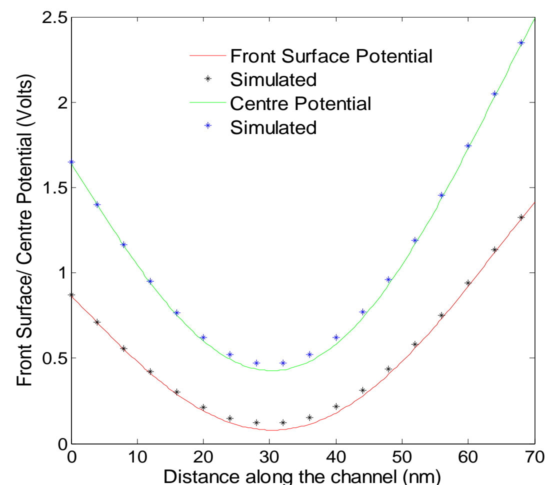

Fig. 4: Front surface potential $\phi_{s1}(x)$ and Centre potential $\phi_c(x)$ profiles of symmetric double gate fully depleted nanoscale SOI MOSFET ($\phi_c(x) > \phi_{s1}(x)$). L=65nm, N_b = 1x10^{17}m^{-3}, $t_{of} = t_{ob} =$1.5nm, $t_{si} = 10nm$, V_{ds} = 0.3V, V_{gs} = 0.3V, $V_{fb,f}$ = $V_{fb,b}$= -0.26V, V_{bi} = 0.868V.

Figure 4 shows the comparison between potentials at the centre and front surface. Figure 5 shows the comparison between potentials at the centre and back surface. For a single gate SOI NMOSFET, application of positive gate bias greater than threshold voltage, i.e V_{gs} > V_{th}, number of minority charge carriers at the

surface is sufficient leading to formation of channel between source and drain and this phenomenon is called surface inversion. However in case of double gate SOI NMOSFET, with application of positive gate bias minority charge carriers at the front $Si-SiO_2$ interface as well as at the back $Si-SiO_2$ interface are not confined to two surfaces. The double-gate control of silicon-on-insulator (SOI) transistors forces the whole silicon film (volume) in strong inversion. Carrier profile is qualitatively modified i.e. most of carriers flow in the middle of film. Increase in concentration of charge carriers at centre of film compared to concentration at $Si-SiO_2$ interfaces justifies volume inversion taking place in double gate SOI MOSFET. Therefore potential at the centre of silicon film is greater than the potential at the front $Si-SiO_2$ interface as well as at the back $Si-SiO_2$ interface.

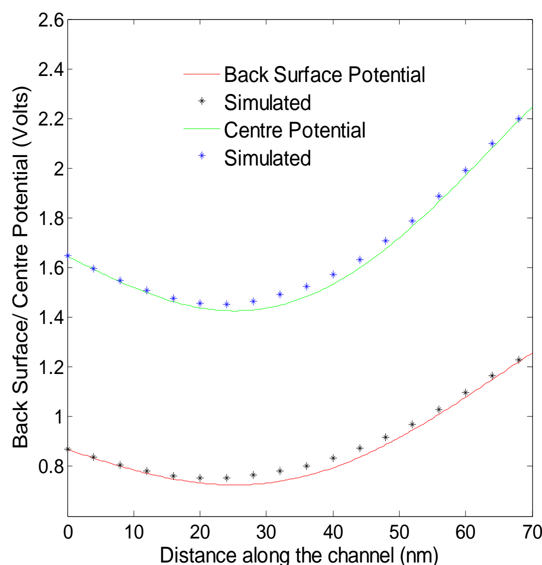

Fig. 5: Back surface potential $\phi_{s2}(x)$ and Centre potential $\phi_c(x)$ profiles of symmetric double gate fully depleted nanoscale SOI MOSFET ($\phi_c(x)$ > $\phi_{s2}(x)$). L=65nm, N_b=1x10^{17}m^{-3}, $t_{of} = t_{ob} = 1.5$nm, $t_{si} = 10nm$, V_{ds} = 0.3V, V_{gs} = 0.3V, $V_{fb,f}$ = $V_{fb,b}$ = -0.26V, V_{bi} = 0.868V.

Variation of drain current with drain voltage for different values of channel width and temperature are shown in Figs. 6 and 7 respectively. As channel width increases, current driving capability increases, hence drain current increases. The drain current in SOI MOSFET varies considerably with temperature. The current-voltage characteristics (Fig. 7) exhibits anomalous trend for increasing temperature.Transcondustance dependence on gate to source voltage for different values of temperature is shown in Fig. 8. Drain current and thus transconductance increases with increase in temperature owing to gradual reduction of phonon scattering. Figure 9 shows variation of transit time with channel length. Increase in channel length increases the transit time. Hence for better speed of the device, the channel length should be very small. Also increase in oxide thickness decreases the transit time.

Recently authors have carried out simulation based study of Double Gate Fully Depleted Decananometer (Channel length, L=10nm) SOI MOSFET [17]. In this paper, behavior of the modeled device in terms of mobility is investigated by varying the thickness of silicon film and gate oxide thickness through simulation carried out on 2D ATLAS device simulator [18].

Figure 10 shows mobility of simulated device measured at the centre of silicon film with thickness of front/back gate taken as 3nm. Figure 11 shows mobility of simulated device measured at the centre of silicon film with thickness of front/back gate taken as 1.5nm whereas all other parameters for device remain same. Density of defects increase during thinning, hence mobility decreases in the film and at both interfaces. Thinning process degrades the film and generates new scattering centers. Mobility decreases as oxide thickness decreases due to stronger surface induced scattering.

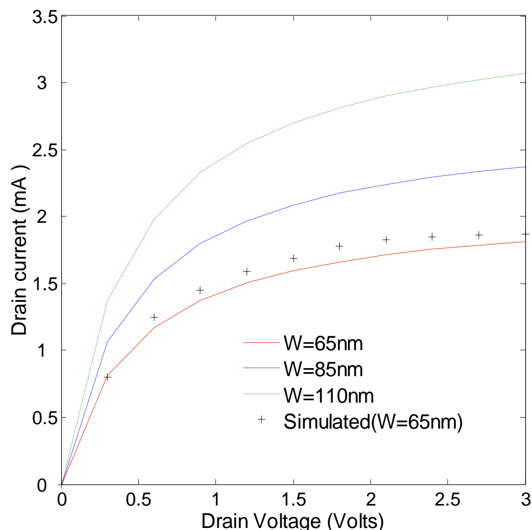

Fig. 6: Drain current versus drain voltage of a symmetric double gate fully depleted nanoscale SOI MOSFET with different values of channel width. L=65nm, N_b = $1x10^{17}m^{-3}$, $t_{of} = t_{ob} = 1.5$nm, $t_{si} = 10nm$, V_{gs} = 0.3V, V_{bi} = 0.868V ,$V_{fb,f}$ = $V_{fb,b}$= -0.26V.

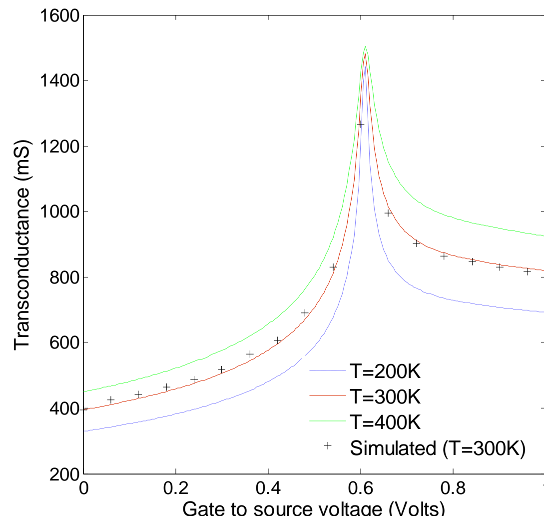

Fig. 8: Transconductance as function of gate to source voltage of a double gate fully depleted nanoscale SOI MOSFET with different values of temperature. L=65nm, W=130nm, N_b = $1x10^{17}m^{-3}$, $t_{of} = t_{ob} = 1.5$nm, $t_{si} = 10nm$, V_{ds} = 0.3V, V_{bi} = 0.868V ,$V_{fb,f}$ = $V_{fb,b}$= -0.26V.

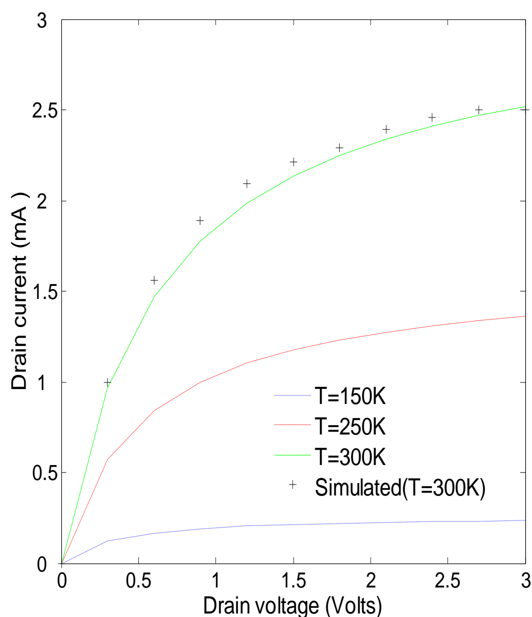

Fig. 7: Drain current versus drain voltage of a symmetric double gate fully depleted nanoscale SOI MOSFET with different values of temperature. L=65nm, N_b = $1x10^{17}m^{-3}$, $t_{of} = t_{ob} = 1.5$nm, $t_{si} = 10nm$, V_{gs} = 0.3V, V_{bi} = 0.868V ,$V_{fb,f}$ = $V_{fb,b}$= -0.26V.

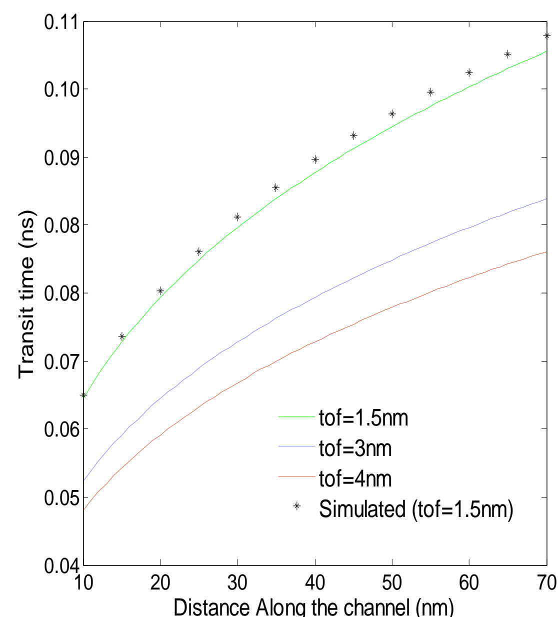

Fig. 9: Transit time of a symmetric double gate fully depleted nanoscale SOI MOSFET with different values of gate oxide thickness. N_b=$1x10^{17}m^{-3}$, $t_{si} = 10nm$, V_{ds} = 1V, V_{gs} = 0.3V, V_{bi} = 0.868V ,$V_{fb,f}$ = $V_{fb,b}$= -0.26V.

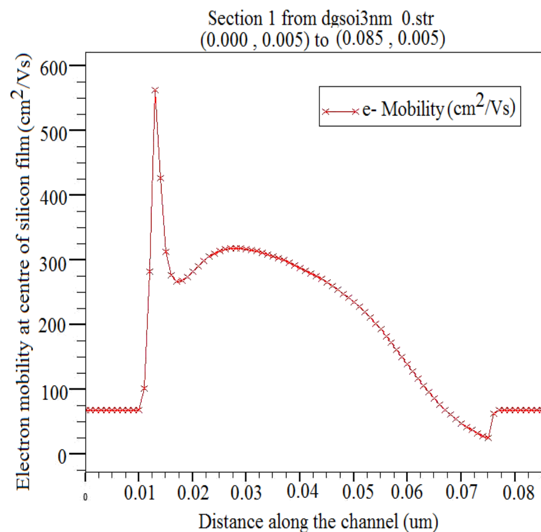

Fig. 10: The simulated output on ATLAS device simulator for modeled device showing mobility along the channel at the centre of silicon film. Channel length L = 65nm, source-drain doping is $1x10^{20}m^{-3}$, Al gates, with work function of 4.10 eV, gate oxide thickness $t_{oxf} = t_{oxb} = 3$nm, $N_b =$ $1x10^{17}m^{-3}$ and $t_{si} = 10nm$.

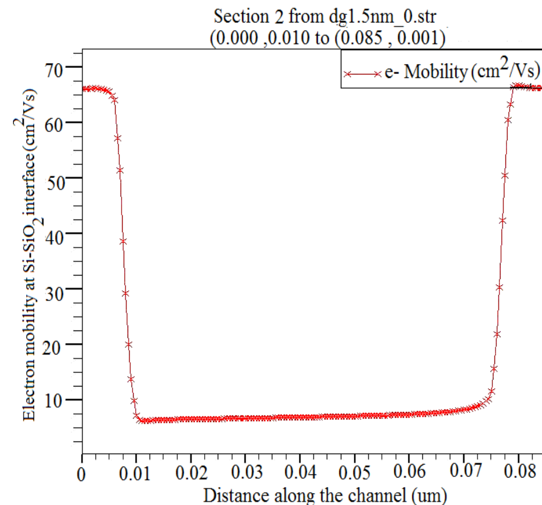

Fig. 12: The simulated output on ATLAS device simulator for modeled device showing mobility along the channel at the Si-SiO_2 Interface. Channel length L = 65nm, source-drain doping is $1x10^{20}m^{-3}$, Al gates with work function of 4.10 eV, gate oxide thickness $t_{of} = t_{ob} = 1.5nm$, $N_b = 1x10^{17}m^{-3}$ and $t_{si} = 10nm$.

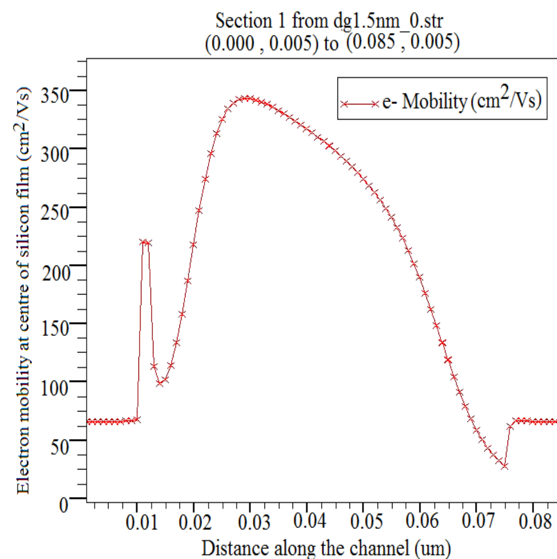

Fig. 11: The simulated output on ATLAS device simulator for modeled device showing mobility along the channel at the centre of silicon film. Channel length L = 65nm, source-drain doping is $1x10^{20}m^{-3}$, Al gates with work function of 4.10 eV, gate oxide thickness $t_{of} = t_{ob} = 1.5$nm, $N_b = 1x10^{17}m^{-3}$ and $t_{si} = 10nm$.

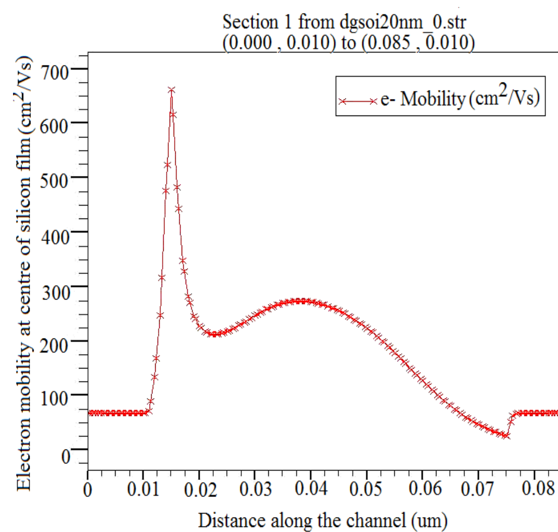

Fig. 13: The simulated output on ATLAS device simulator for modeled device showing mobility along the channel at the centre of silicon film. Channel length L = 65nm, source/drain doping is $1x10^{20}m^{-3}$, Al gates with work function of 4.10 eV, gate oxide thickness $t_{of} = t_{ob} = 1.5nm$, $N_b =$ $1x10^{17}m^{-3}$ and $t_{si} = 20$nm.

Figure 12 shows mobility of simulated device measured at the $Si-SiO_2$ interface of silicon film. The electric field is negligible in the middle of double gate SOI MOSFET where most of inversion charge is located. As electron-phonon scattering strongly depends upon field, the mobility increases in the centre of film. Thus increase in mobility at centre of film (Fig. 11) compared to mobility at $Si-SiO_2$ interface (Fig. 12) is due to effect of volume inversion taking place in double gate SOI MOSFET.

Figure 13 shows mobility of simulated device measured at the centre of silicon film with thickness of silicon film taken as 20 nm whereas all other parameters for device are kept same as in Fig. 11. Key effect influencing electron transport in double gate SOI inversion layers is phenomenon of phonon scattering. Comparing the performance of the device on the basis of silicon film thickness, it is seen that mobility of the simulated device with 20nm silicon film thickness (Fig. 13) is higher than mobility of device having silicon film thickness of 10 nm (Fig. 11). Increase in silicon film thickness reduces scattering of charge carriers thereby improving mobility and thus the performance of the device.

IV. CONCLUSION

Based on 2D model for potential distribution for double gate fully depleted nanoscale SOI MOSFET recently developed by authors, surface potential sensitivity to channel length scaling has been investigated to explore short channel effects. Surface potential increases as the channel length decreases due to channel length modulation. Analytical expression for centre potential in terms of surface potential is then obtained. Analytical results show that the potential at the centre is greater than the potential at the front surface as well as at the back surface. This indicates that the carrier profile is qualitatively modified: most of carriers flow in the middle of film, not at the two interfaces (front $Si-SiO_2$ interface and back $Si-SiO_2$ interface). Increase in concentration of charge carriers at centre of film compared to concentration a $Si-SiO_2$ t interface is due to effect of volume inversion taking place in double gate SOI MOSFET. Device simulation is done using 2D ATLAS device simulator [18] and results obtained are compared with analytical results. The modeled results are found to be in good agreement with simulated data. Device performance parameters such as drain current, transconductance and transit time are investigated with respect to variation in process parameters such as temperature, channel width, channel doping and gate oxide thickness. Lastly, effect of volume inversion taking place for the modeled device leading to increase in mobility is also justified through simulation results done on 2D ATLAS device simulator. Simulation results show that reduction of gate oxide thickness and silicon film thickness results in decrease in mobility due to stronger surface induced scattering.

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