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DESIGN OF A HALF-ADDER USING SILICON QUANTUM DOT-BASED SINGLE-ELECTRON TRANSISTOR OPERATING AT ROOM TEMPERATURE

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ABSTRACT

In this paper, for the first time, we have proposed a half-adder using single-electron transistors (SETs) operating at room temperature. The proposed circuit has been designed based on SET logic, and multi-gate SETs based on silicon quantum dots with 2 nm diameters operating at room temperature have been used as switching transistors. In logic used for the design, '0' and '1' bits of information are represented by low and high voltage levels, respectively. We have chosen 0.0Volt and 2.9Volt, respectively, for low and high levels of input voltages. The logic operation of the half-adder has been verified using SIMON simulator. Simulation results show that the designed circuit performs the expected operation correctly, and low and high levels of output voltages are approximately 0.0Volt and 0.1Volt, respectively.

Keywords: Half-adder, logic gate, single-electron transistor (SET), SET logic, silicon quantum dot (Si-QD).

I. INTRODUCTION

Single-electron transistor [1,2] is one of the best candidates for future logic VLSI circuits because of its high packing density and ultra-low power dissipation. The structure of a usual SET consists of three metallic electrodes of source, drain, and gate as well as a metallic or semiconductor island. This device utilizing the coulomb blockade of electron tunneling or single-electron charging effect [2,3] can be used to implement logic circuits in which one or a few electrons are manipulated to perform logic operations.

So far, several SET-based logic circuits have been proposed and analyzed [4-10]. SETs with silicon islands (Si-SETs) are more promising than the metallic ones because of their better performance at room temperature. Thus, recently, attentions have been attracted more to Si-SETs and circuits implemented using them [11-14].

In this work, design, simulation, and analysis of a half-adder based on 2nm diameter Si-QD-based SET operating at room temperature is presented. The operation of this transistor, considering the Pauli's exclusion principle and effects of energy-levels quantization and broadening in Si-QD, has been studied in [15,16]. The paper is organized as follows: in section 2, design concept based on SET is discussed. In sections 3 and 4, binary addition of two bits is described and accordingly the half-adder circuit is designed. In section 5, the logic operation of the half-adder is simulated using SIMON [17] to verify the correct function of the circuit. Summary and some remarkable results of the paper are presented in section 6.

II. BASIC LOGIC OF DESIGN

SET logic [2,18,19] is one of the usual approaches for implementing single-electron circuits. This logic utilizes SETs as switching transistors, in a manner similar to conventional MOS transistors, to implement logic gates and circuits. In this logic, high and low voltage levels define the '1' and '0' bits, respectively. Because of SET's capability of complementary operation [8,20], the SET logic-based circuits can be easily conceptualized from CMOS circuits and thus have two important advantages. First, most of logic functions, which are performed

by CMOS, can be implemented by them. Second, coupling to other devices can be easily carried out since outputs are represented by the charging voltages of output capacitors.

For the design, we have used this logic and employed multi-gate SETs based on Si-QDs with 2 nm diameters operating at room temperature as switching transistors. Fig. 1 shows the equivalent circuit of a double-gate SET based on Si-QD. In this figure, V_{IN}, V_C, and V_{dd} are the input-gate voltage, control-gate voltage, and bias voltage applied to drain, respectively. The input-gate and control-gate capacitances have been set to the same values and denoted by C_{IN}. The parameters of this transistor have been listed in Table I.

Fig. 2 illustrates the drain current versus input-gate voltage characteristic of this transistor. In Fig. 1, one of the gates has been used as a control gate. By applying a constant dc voltage of V_C=2.9V, the characteristic is shifted by 180º for the first three peaks (red curve). In other words, the SET works as a P-type transistor. Thus, the control gate enables the complementary use of the SET (as the N- or P-type transistor). In Fig. 2, points "1" to "3", open circles in blue curve, are operating points for the transistor, depending on the sum of V_{IN} and V_C. As can be seen, the SET is ON when this summation is equal to 2.9V, and the SET is OFF when this value is equal to 0 or 5.8 V.

TABLE I: Parameters used in SIMON

Parameter	Value
C_S, Source tunnel junction capacitance	$1.25*10^{-19}$ F
C_d, Drain tunnel junction capacitance	$1.25*10^{-19}$ F
C_{IN}, Gate capacitance	$0.92*10^{-19}$ F
C_Σ, Island total capacitance	$4.34*10^{-19}$ F
R_T, Tunneling resistance (R_s=R_d=R_T)	$1.3*10^6$ Ω
H, Height multiplication factor	$1eV^2$
ΔE, Energy-levels spacing	0.43eV
W_1, First energy-state broadening	0.0005eV
W_2, Second energy-state broadening	0.005eV
W_3, Third energy-state broadening	0.08eV
W_4, Fourth energy-state broadening	0.11eV
V_{dd}, Drain bias voltage	0.1V
Temperature	300 °K

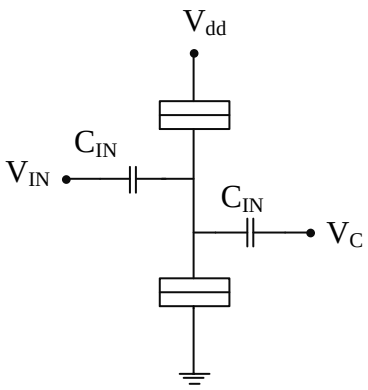

Fig. 1: Equivalent circuit of the double-gate SET based on Si-QD.

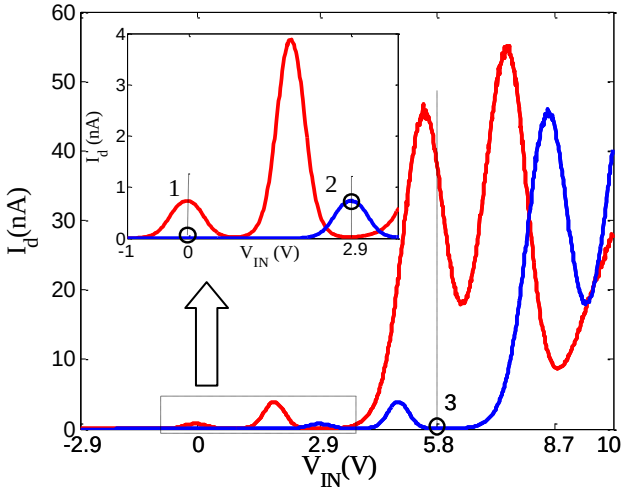

Fig. 2: Drain current, I_d, of the SET shown in Fig. 1 as a function of input-gate voltage (V_{IN}) with the bias voltage V_{dd}=0.1V. The blue and red curves are drain current for V_C= 0 and V_C=2.9V, respectively.

III. TWO BITS BINARY ADDITION

As we know, when two bits, for example A and B, are added, a one-bit sum and a one-bit carry are produced. A half-adder is used for this purpose. The sum bit is '1' only when one of the addend bits is '1', otherwise it is '0'. This result is identical to an XOR operation. Thus, the sum bit is implementable using an XOR logic gate with two inputs of A and B. The carry bit will be '1' if both of A and B are '1', otherwise it will be '0'. This effect is the same as an AND operation. Therefore, the carry bit can be performed using an AND logic gate with two inputs of A and B. Thus, a half-adder circuit can be implemented by employing an XOR logic gate and an AND logic gate. In following sections, we concentrate on design of these two gates as well as explanation of their operation.

III.1. AND Logic Gate

Fig. 3 illustrates the proposed elemental circuits for design of AND logic gate. The circuit is composed of two double-gate SETs shown in Fig. 1. These two SETs have a common gate as input (A). The remaining gate in the double-gate SET is a control gate by which we can change type of the SET. Therefore, the two SETs in the elemental circuit can be used in a complementary manner where SET_1 and SET_2 work as N- and p-type transistors, respectively. The control-gate voltage has been set zero for N-SET and V_C=2.9V for P-SET, also the input logic levels '0' and '1' have been set to zero and V_{IN-H}=2.9V, respectively. When the input is logic '1', SET_1 is ON and SET_2 is OFF, and when the input is logic '0', SET_1 and SET_2 are OFF and ON, respectively. The circuit outputs V_O=A.V_1 with V_1 of the bias voltage and A of the input signal.

Fig. 4 shows the equivalent circuit of the proposed 2-input AND logic gate. In this figure, A and B are two arbitrary input signals. This circuit is constructed by sequential connection of the elemental circuit shown in Fig. 3. It is impossible to use the input voltage directly for bias pin because SETs can only use a low source-drain voltage. In other words, in order to maintain the coulomb blockade condition, it is needed that $V_{DS}<e/C_{\Sigma}$, so the BUFFER have been used in the structure of AND gate.

III.2. XOR Logic Gate

Fig. 5 shows the equivalent circuit of the proposed XOR logic gate. The circuit is composed of two three-gate SETs. For these transistors, source and drain tunnel junction capacitances are the same and are $C_S=C_d=0.79*10^{-19}$ F, and their other parameters are identical to the double-gate transistor illustrated in Fig. 1. For this circuit, the output is HIGH (logic '1') if solely one of the inputs, A or B, is HIGH (logic '1'), and the output is LOW (logic '0') when neither or both inputs are HIGH.

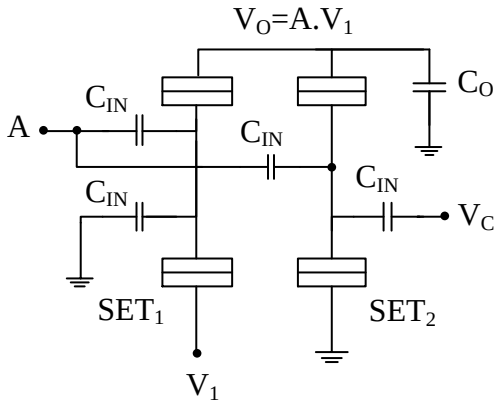

Fig. 3: Elemental circuit for implementation of AND logic gate.

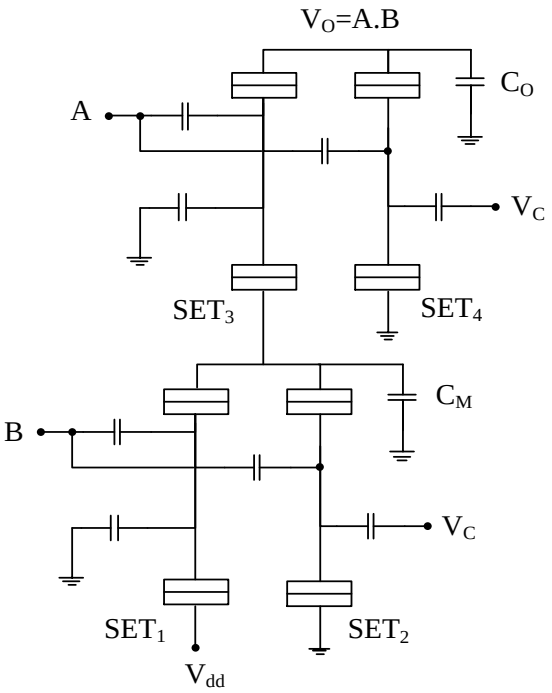

Fig. 4: Equivalent circuit of the proposed 2-input AND logic gate.

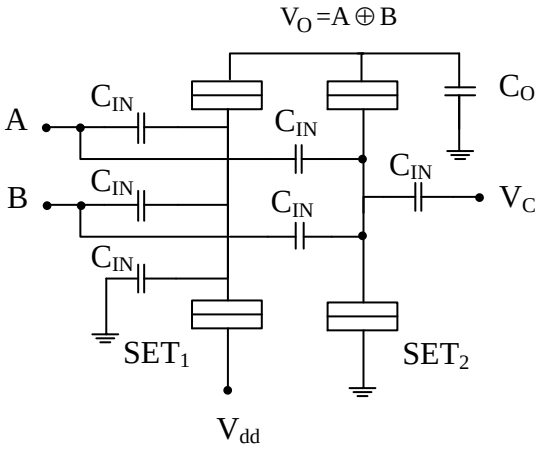

Fig. 5: Equivalent circuit of the proposed XOR logic gate.

IV. HALF-ADDER

Fig. 6 shows the equivalent circuit of the proposed half-adder. The carry and the sum blocks are the circuits shown in Figs. 4 and 5, respectively. In Fig. 6, A and B are the addends, C_O is the output node capacitance, and C_M is the inter-SET-node capacitance which has been used to suppress the high voltage fluctuations. One can see that the half-adder operation, i.e., calculation of one-bit sum and carry, can be performed using only six transistors. The operation validity of the designed circuit is investigated in the next section.

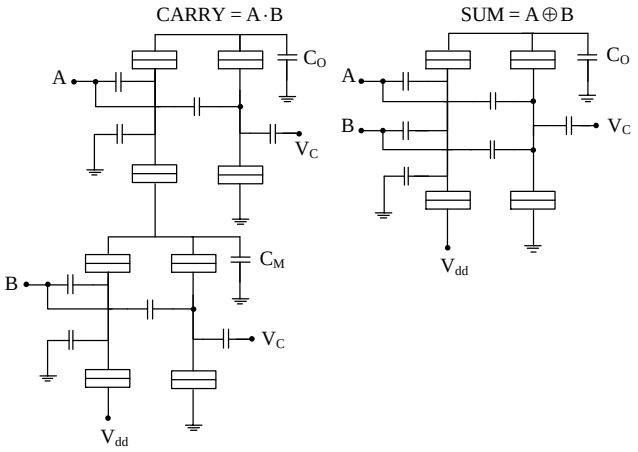

Fig. 6: Equivalent circuit of the half-adder.

V. SIMULATION RESULTS AND DISCUSSION

In this paper, simulations are performed by using SIMON which is a Monte Carlo simulator for single-electron devices and circuits. What we have simulated is the change in the voltage of the sum and carry output nodes. It is noted that we have set the output node and inter-SET-node capacitances to 50aF and 10aF, respectively. Fig. 7 shows the logic operation of the half-adder. In this figure, A and B are the inputs of the half-adder and can take only two values; 0.0Volt which corresponds to logic '0', and 2.9Volt which corresponds to logic '1'. The inputs are piecewise constant and apply all possible combinations of logic '0' and '1' to the circuit. As can be seen, the low and high voltage levels at the sum and carry output nodes are approximately 0.0Volt and 0.1Volt, respectively. The simulations clearly confirm the correct performance of the proposed half-adder.

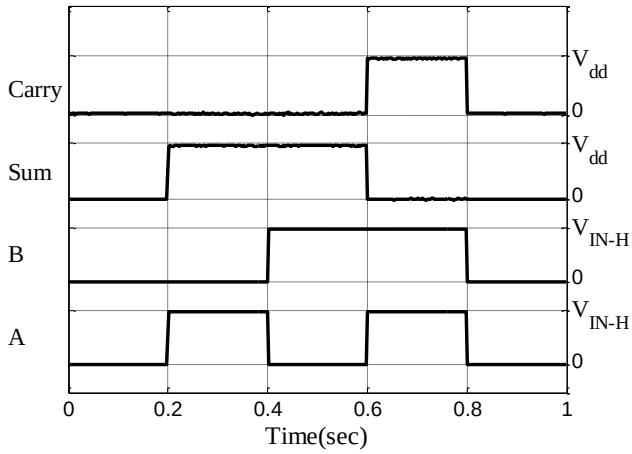

Fig. 7: Logic operation of the half-adder, time variations of input voltages (A and B) and output nodes voltages (sum and carry).

VI. CONCLUSION

The design and simulation of a SET-based half-adder was presented in this paper. The design is based on SET logic and uses multi-gate SETs based on Si-QDs with 2 nm diameters operating at room temperature as switching transistors. The circuit adds two bits and produces their sum and carry. The circuit comprises six transistors. The inputs '0' and '1' logic levels of the half-adder are corresponding to voltages of 0.0Volt and 2.9Volt, respectively. The results of simulations provided by SIMON simulator, show that the low and high levels of output voltages, sum and carry, are approximately 0.0Volt and 0.1Volt, respectively. These results also indicate that the presented half-adder operates correctly.

References

[1] T. A. Fulton and G. D. Doran, "Observation of single-electron charging effects in small tunnel junctions", Phys. Rev. Lett. **59**, 109 (1987).

[2] K.K. Likharev, "Single-electron devices and their applications", Proc. IEEE **87**, 606 (1999).

[3] H. Grabert and M. H. Devoret, "Single Charge Tunneling: Coulomb Blockade Phenomena in Nanostructures", NATO Adv. Sci. Inst. Ser. B, Plenum Press, New York (1992).

[4] B. Pruvost, K. Uchida, H. Mizuta, and S. Oda, "Design of New Logic Architectures Utilizing Optimized Suspended-Gate Single-Electron Transistors", IEEE Trans. Nanotechnol. **9**, 504 (2010).

[5] Y. Miyoshi, F. Nakajima, J. Motohisa, and T. Fukui, "A 1 bit binary-decision-diagram adder circuit using single-electron transistors made by selective-area metalorganic vapor-phase epitaxy", Appl. Phys. Lett. **87**, 33501 (2005).

[6] J. He, Z.A.K. Durrani, and H. Ahmed, "Universal three-way few-electron switch using silicon single-electron transistors", Appl. Phys. Lett. **85**, 308 (2004).

[7] Y. Ono, H. Inokawa, and Y. Takahashi, "Binary adders of multigate single-electron transistors: Specific design using pass-transistor logic", IEEE Trans. Nanotechnol. **1**, 93 (2002).

[8] Y. Ono, Y. Takahashi, K. Yamazaki, M. Nagase, H. Namatsu, K. Kurihara, and K. Murase, "Si complementary single-electron inverter with voltage gain", Appl. Phys. Lett. **76**, 3121 (2000).

[9] Y. Takahashi, A. Fujiwara, K. Yamazaki, H. Namatsu, K. Kurihara, and K. Murase, "Multigate single-electron transistors and their application to an exclusive-OR gate", Appl. Phys. Lett. **76**, 637 (2000).

[10] M. Y. Jeong, Y. H. Jeong, S. W. Hwang, and D. M. Kim, "Performance of single-electron transistor logic composed of multigate single-electron transistors", Jpn. Appl. Phys. **36**, 6706 (1997).

[11] Y. Sun, Rusli, and N. Singh, "Effect of Oxidation-Induced Tensile Strain on Gate-All-Around Silicon-Nanowire-Based Single-Electron Transistor Fabricated Using Deep-UV Lithography", IEEE Trans. Nanotechnol. **10**, 1214 (2011).

[12] Y. Sun, Rusli, and N. Singh, "Room-temperature operation of silicon single-electron transistor fabricated using optical lithography", IEEE Trans. Nanotechnol. **10**, 96 (2011).

[13] S. J. Shin, C. S. Jung, B. J. Park, T. K. Yoon, J. J. Lee, S. J. Kim, J. B. Choi, Y. Takahashi, and D. G. Hasko, "Si-based ultrasmall multiswitching single-electron transistor operating at room-temperature", Appl. Phys. Lett. **97**, 103101 (2010).

[14] Y. C. Jung, K. H. Cho, B. H. Hong, S. H. Son, D. S. Kim, D. Whang, S. W. Hwang, Y. S. Yu, and D. Ahn, "Fabrication and characterization of sidewall defined silicon-on-insulator single-electron transistor", IEEE Trans. Nanotechnol. **7**, 544 (2008).

[15] M. Miralaie, M. Leilaeioun, K. Abbasian, and M. Hasani, "Modeling and analysis of Room-Temperature Silicon Quantum Dot-Based SET Logic gates", J. Comput. Theor. Nanosci. (2012), in press.

[16] M. Miralaie, M. Leilaeioun, and K. Abbasian, "Modeling of a Room-Temperature Silicon Quantum Dot-Based Single-Electron Transistor and the Effect of Energy-Level Broadening on Its Performance", J. Electron. Mater. (2012).

[17] C. Wasshuber, H. Kosina, S. Selberherr, "SIMON a simulator for single-electron tunnel devices and circuits", IEEE Trans. Comput. Aided Des. Integr. Circuits Syst. **16**, 937 (1997).

[18] A. N. Korotkov, R. H. Chen, and K. K. Likharev, "Possible performance of capacitively coupled single-electron transistors in digital circuits", J. Appl. Phys. **78**, 2520 (1995).

[19] R. H. Chen, A. N. Korotkov, and K. K. Likharev, "Single-electron transistor logic", Appl. Phys. Lett. **68**, 1954 (1996).

[20] J. R. Tucker, "Complementary digital logic based on the Coulomb blockade", J. Appl. Phys. **72**, 4399 (1992).