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Corner effects sensitivity to Fin geometry variations in Tri-gate SOI-FinFET

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ABSTRACT

SOI-FinFET transistors have emerged as novel devices having superior controls over short channel effects (SCE) and higher current drive than the conventional MOS transistor devices.

In Tri-gate SOI-FinFET where the channel is controlled by gate from three sides of the Si thin film known as fin, deducing fin geometry have great influence on undesirable characteristics such the corner effects,

In this work, the corner effect of Tri-gate SOI-FinFETs is investigated by 3D Process and device simulation and their electrical characteristics are compared for different fin geometry.

It has been observed that the increase in fin height H_{fin} is a solution to neglect the corner effect because this increase will decrease the part of the corners compared to the all silicon film.. An enhancement in the on state current and sub-threshold performance have been observed.

Index Terms: FinFET, Silicon-On-Insulator, Fin geometry, corner effect

I. INTRODUCTION

The intensive and fast downscaling of CMOS transistors has been the leading cause behind the growth of the semiconductor industry for the last years. However, short channel effects (SCE) coming into picture such as V_T roll-off, hot carrier effects, drain induced barrier lowering (DIBL), increase in sub-threshold swing and leakage currents, etc, make difficult for the industry to follow the Moore's Law with bulk devices. The Solution to contain these effects is to require performance boosters, like use of novel materials and non-classical device structures to continue further scaling. These includes partially depleted SOI (PDSOI) MOSFETs, fully depleted SOI (FDSOI) MOSFETs and multi-gate MOSFETs which are being investigated [1] to continue improving the device performance and to follow the International Technology Roadmap for Semiconductor (ITRS) [2]. The main feature [3] of these multi-gate transistors is the improving the gate control over the channel by geometrically placing the gate close to the channel and providing tighter gate coupling for a better control over the channel and to avoid short channel effects.

The tri-gate SOI-FinFET [4] is one of the promising structures in nano scale regime where the channel is controlled by gate from three sides of the Silicon film. Since the gate control is increased, the requirements on the Silicon film thickness are relaxed as compared to single gate or DG-FinFET.

In Tri-gate FinFET due to proximity of two adjacent gates in corners we get premature inversion [5]. The presence of charge sharing effect between two adjacent gates causes the premature inversion in the corners. The corners present gives rise to the formation of independent channels with different threshold voltages. This phenomenon is known as corner effect. The potential curve is changed in these corners of silicon, this change results in a leakage current in corners which is not under control of gates [6]-[7]. In this area, the threshold voltage is smaller than elsewhere, thus before the transistor is activated, it exists already a sum of current of corner called "leakage current".

In this paper, a device simulations and 3D process was presented for an increased sight of the source and drain area in tri-gate SOI-FinFET. The role of corners in nano-scale dimensions below 50nm has been investigated. For the larger devices, the conduction along the planar side of the devices dominates the current conduction. Whereas in small dimension devices a larger part of the current is carried by the corners, since the surface of the corners is comparable to the inversion channel along the planar surface. The corners are inverted in threshold regime, so it does not deteriorate the performance.

II. DEVICE STRUCTURE

The device structure for the Tri-gate SOI-FinFET is shown in Fig.1 schematically. The gate electrode wraps around the fin and separated from it by the gate oxide (in black), and S/D regions are formed on two ends of

the fin. With the gate on the top and two sides of the channel, the voltage applied to the gate has more effect on the channel than in the conventional FET, which has the gate only on the top surface of the channel.

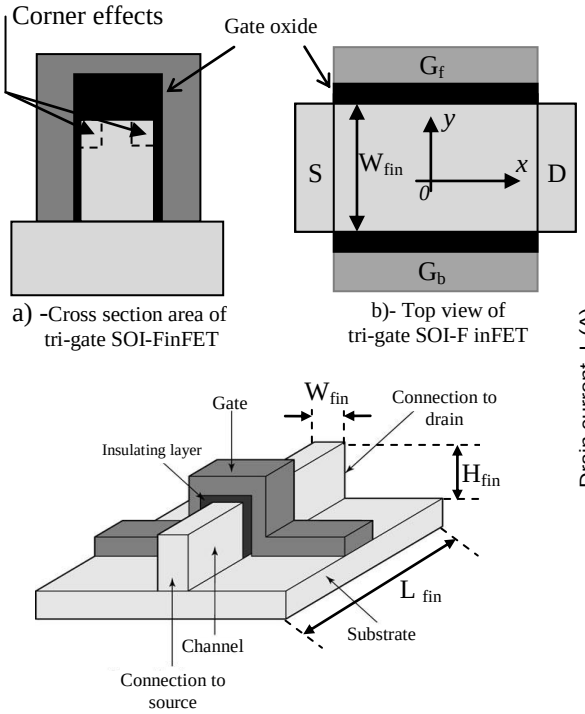

Fig. 1: Dimensional schematic view of tri-gate FinFET.

This schematic of tri-gate SOI-FinFET (Fig.1) shows the important geometrical parameters of the fin which are width (W_{Fin}), height (H_{Fin}) and channel length (L).

Channel length (L):

In order to manufacture a circuit which functions quickly as possible and which consumes less energy with the smallest possible surface, it is necessary to decrease the channel length of the transistor.
By reducing the channel length, the surface occupied by the transistor is thus reduced and resistance series is decreased allowing to have a more important current. At the same time, the transcapacity (Cgg) is reduced and then the speed of the circuit is increased.

Fin width (or thickness) W_{fin}:

To depleting all the thickness of the silicon film, in the case where the doping of the substrate is weak or intrinsic, W_{fin} must be small. According to the simple scaling theory, the natural length l is decreased as the fin width decreased. The reduction in W_{fin} does not have only beneficial consequences; it will also imply the appearance of the effects of quantum mechanics. That made deviate the carriers of the interface Si-SiO_2 towards the fin center by increasing the effective *band-gap*, the threshold voltage will thus increase and the capacity of the oxide of gate will be reduced. In addition, when W_{fin} is reduced without considering the quantum effects, the section of silicon film is smaller, which increases resistance series and reduces the current.

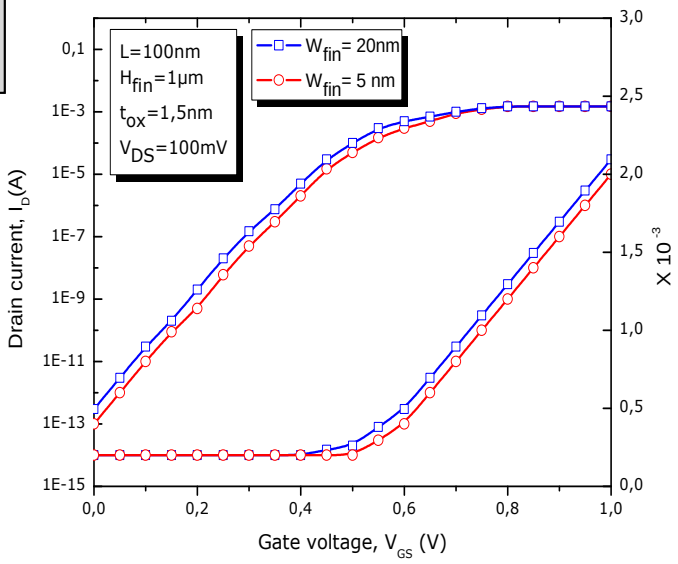

Fig. 2: Influence of the W_{fin} parameter in 3D simulations

Fig 2 shows the simulated results for the Id (Vg)-characteristics with two different fin widths, 20nm and 5nm. When W_{fin}=20nm, the lateral electric field varies more rapidly at the W_{fin}=5nm. The rapid spatial variation in electric field prevents carriers from reaching a steady-state equilibrium with the local electric field, and the electron temperature of the narrowed W_{fin} is reduced. Although the maximum electric field on the drain side is increased as W_{fin} is reduced, witch result reduction in drain current with decreasing fin width.

Fin height H_{fin}:

The fin height can be comparable to the channel width in the case of MOSFET bulk. But in this case, in strong inversion, the width W_{fin} can be estimated at twice the height H_{fin}. In order to have an important current, the height H_{fin} must be largest as possible. That limits also the corners effects and the effects of quantum mechanics in vertical direction. However, because of the difficulty of manufacture, H_{fin} cannot always be increased as it is wished. When H_{fin} is very large, to maintain the uniformity of the fin width throughout the vertical direction will be a challenge. Consequently, to

amplify the current, we can multiply the silicon films in parallel witch gave the idea of the development of technology MOSFET to nanofil.

III. PROCESS AND DEVICE SIMULATION

As the 3D structures of FinFETs are complex [8] and also, beyond 50 nm gate length, the channel profile needs critical adjustment for setting the threshold voltage, we use Silvaco simulator from TCAD which is a privately owned provider of electronic design automation (EDA) software [9]. This simulator has many facilities and the following modules are used in this study:

- Structure and Mesh Editor **DevEdit**: Can be used to either create a device from scratch or to remesh or edit an existing device, and can be also used directly within DeckBuild. In command mode DevEdit structures can be parameterized and varied automatically by DeckBuild or Virtual Wafer Fab (VWF) [10].
- Device Simulation Framework **Atlas:** Is a 2D and 3D Device Simulation Framework which enables device technology engineers to simulate the electrical, thermal and optical behavior of semiconductor devices. ATLAS solves the fundamental physical equations describing the dynamics of carriers in semiconductor devices for arbitrary device structures and also predicts terminal characteristics of semiconductor devices for steady state, transient and small signal AC stimuli.
- 3D Interactive Visualization Tool **TonyPlot3D**: Is a 3D graphics viewer, capable of displaying 3D TCAD data generated by Silvaco TCAD process or device simulators.

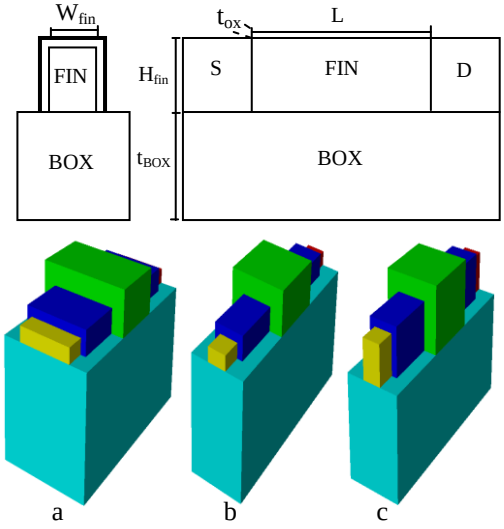

Fig. 3-a: The 3-D device structure generated from DevEdit3D and TonyPlot3D: *a) H_{fin}=50nm, W_{fin}=150nm. b) H_{fin}=50nm, W_{fin}=50nm. c) H_{fin}=150, W_{fin}=50nm*

The 3D view of the simulated device with fin geometry variation is shown in Fig.3-a and the cross sectional view is shown in Fig.3-b.

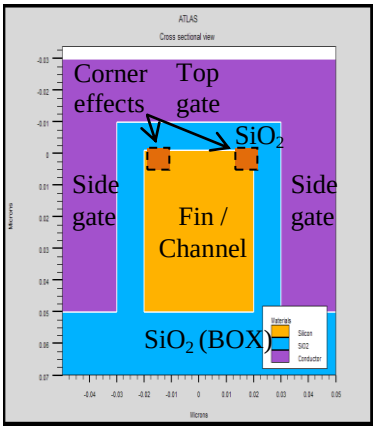

Fig. 3-b: Cross sectional view of tri-gate SOI-FinFET.

The 3D SILVACO simulation suite including, DevEdit3D and TonyPlot3D is performed in this article, in order to validate the basic principles and to uncover several important aspects: evaluation of the width and fin height effects on corner effects in tri-gate SOI-FinFETs. For this purpose each and one parameter was varied to study its effect independently of the others.

The solution to remove the effects of the corner is proposed in [5]. If the doping of silicon is very weak or intrinsic, the corner effects are generally negligible; another solution is to round the corner. This is why the GAA does not have corner effects [6]

To neglect these corner effects we will try to minimize the part of corners compared to the all silicon film by increasing sufficiently the fin height (H_{fin}).

IV. 3D DEVICE SIMULATION AND RESULTS

According to a comparison of the potential in the oxide and the silicon in the section perpendicular to the flow of the current for various heights and widths of fin simulated with the simulator of the device Atlas of Silvaco, we see that for a very high fin H_{fin} = 1µm, the potential in silicon is nearly identical in the vertical direction (Fig.4). There is only one small portion of the potential which is not identical in the vertical direction near to the interfaces between the silicon and the gate above silicon and oxide of the substrate, this last result from the penetration of the influences of side gates through oxide above the silicon and oxide of substrate. Because oxide above silicon (t_{ox_top}) is very thick

(t_{ox_top}=50nm), the gate above silicon has a very weak influence on the silicon and can be neglected compared to the side gates.

When the fin height decreases until 50nm, if the fin width is sufficiently small (W_{fin}=20nm or less); the potential in the vertical direction is still nearly identical. The parts of the potential which are not identical in the vertical direction are neglected compared to the part of identical potential thanks to the good control of the transverse gates. When the fin height is very small (H_{fin}=20nm), we cannot any more consider that the potential is identical in the vertical direction whatever the value of W_{fin} .Contours of the potential are rounded.

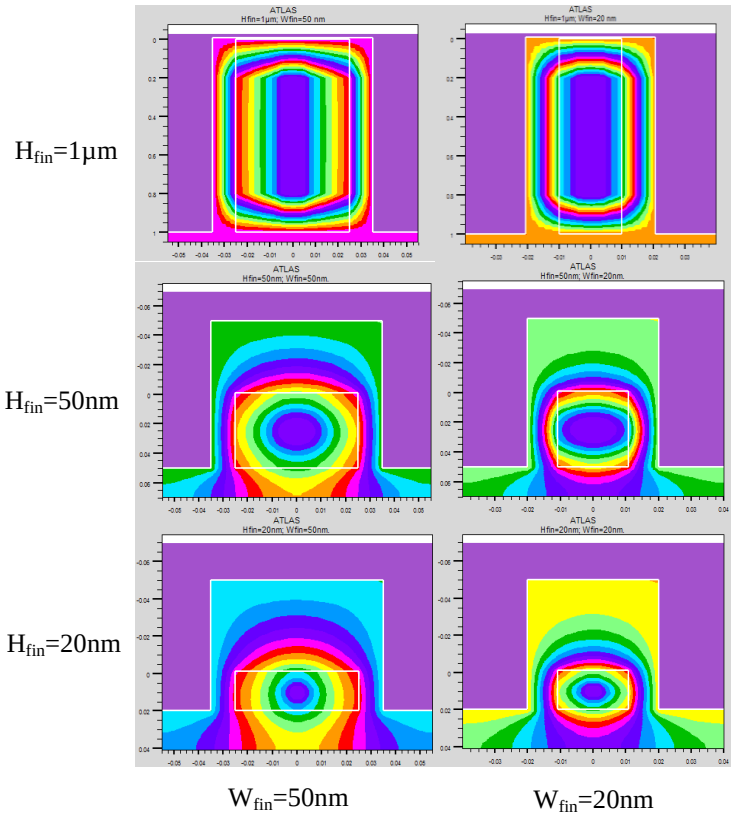

Fig. 4: Potential in the oxide and the silicon in the section y-z for a channel length of 1µm and a V_{gs} = 0.3V

V. CONCLUSION

The 3D structure of SOI-FinFET introduces new undesirable effects like the corner effect which can be well eliminated by a very weak doping of silicon or an intrinsic silicon. In this work a study of the influence of fin geometry on corner effects in Tri-gate SOI-FinFET performances has been reported to present a new solution which will allow to eliminate this undesirable effect. This solution is the minimization of the corner part with increasing the fin height.

We spoke about the effects of corners located in the two higher corners. In fact, they can also exist in the two lower corners [11], [12], the electric lines coming from the grids cross oxide in bottom and arrive at silicon film, and they influence the potential in bottom of silicon, this effect is called also the BOX effect and has an influence similar to the corners effect and it can be limited by reducing the fin width W_{fin} and It will be next course of study.

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