Journal of Electron Devices, Vol. 18, 2013, pp. 1582-1586

© JED [ISSN: 1682 -3427]

Journal of Electron Devices
www.jeldev.org

SUITABILITY OF HIGH-k GATE DIELECTRICS ON THE DEVICE PERFORMANCE AND SCALABILITY OF NANOSCALE DOUBLE GATE FINFETS WITH QUANTUM MODELING: A SIMULATION STUDY

Subha Subramaniam[1], Sangeeta M.Joshi[2], R.N. Awale[1]

[1]Department of Electrical Engineering, Veeramata Jijabai, Technological Institute, Mumbai, India
[2]Department of Electronics Engineering, Vidyalankar Institute of Technology, Mumbai, India

Received 11-10-2013, revised 24-10-2013, online 25-10-3013

ABSTRACT

The impact of a high-*k* dielectrics and the effect of downscaling on the device performance of nanoscale DG-FinFET is studied using the device simulation tool PADRE. Simulations were performed for a wide range of dielectric permittivity *k* and scaling limits of DG-FinFET structure is studied for different gate lengths varying from 45nm to 10nm. Simulations were performed for the proposed technology nodes with specifications matching the ITRS requirements with proportionate device dimensions. Matlab is used to calculate the equivalent oxide thickness of high-k gate materials. As we scale down below 22 nm gate lengths with the new device architectures, introduction of high-k gate dielectric becomes imminent to alleviate the problems associated with short channel effects. The simulation results show an exponential increase in threshold voltage, transconductance, and drive current and an exponential decrease of leakage current with increasing dielectric constants for all gate lengths. The effect of scaling and high-k gate materials on the fringing capacitance is also modeled using matlab. However linear increase in the parasitic fringing capacitance with high-k dielectrics is observed. This leads to increase in the electric field and degrades the performance of DG-FinFETs. This degradation can be controlled by using high k as spacers. Our results prove that DG-FinFET has a scalable structure upto 10nm and $La_2O_3/LaAlO_3$ (k=30) as a promising scope of gate material for 22nm and below gate lengths up to 10nm.

Keywords: FinFETs, high-k gate dielectric, DIBL, Subthreshold Swing, On current, Leakage Current, transconductance.

I. INTRODUCTION

Scaling of device dimensions has been the primary factor for the rapid growth of the semiconductor industry [1,3]. Due to limitations in gate-oxide thickness and source/drain(S/D) junction depth, scaling of conventional bulk MOSFET devices has become difficult. FinFETs emerged as one of the most promising novel device structures to solve the problems associated with short channel effects owing to the simultaneous control of the channel by more than one gate. The FinFET consists of a channel formed in a vertical Si fin controlled by a self aligned double-gate. In the FinFET structure the silicon resembles the dorsal fin of a fish. The silicon body has been rotated on its edge into a vertical orientation such that only the source and drain regions are placed horizontally about the body, as a conventional planar FET [4]. With decreasing oxide thickness below 1.5nm gate oxide leakage due to direct tunnelling becomes more significant.

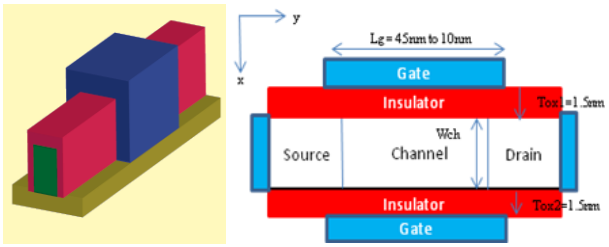

Fig.1.Two dimensional cross section of the DG-FinFET Device Structure used for device simulations

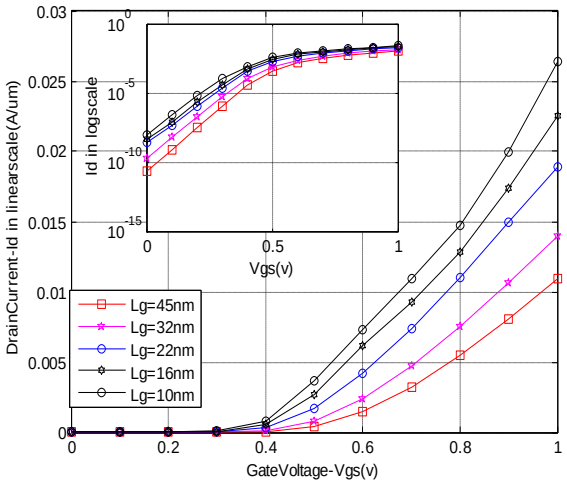

Fig.2: Plot showing the I_d-V_g characteristics for various gate lengths. Inset shows the plot of I_d-V_g in logscale.

The obvious remedy is to replace silicon dioxide with an insulator that has significantly higher dielectric constant than 3.9.This will allow the device to operate using the same capacitance, but with a higher physical thickness that suppresses direct current leakage, and hence, lower power consumption [1].

The new oxides must satisfy six conditions to be acceptable as gate dielectrics, a high enough *K* value, thermal stability, kinetic stability, band offsets, good interface quality with Si, and low bulk defect density. On this basis the dielectrics with k values 3.9, 7, 10, 11, 12, 15, 25 and 30 for this work. These dielectric constants

correspond to SiO_2 (k=3.9), Si_3N_4 (k=7), Al_2O_3 (k=10), $HfSiO_4$ (k=11), Gd_2O_3 (k=12), Y2O3 (k=15), HfO_2/ZrO_2 (k=25), and La_2O_3/a-$LaAlO_3$ (k=30) respectively. In order to examine the scalability of DG-FinFET structure various gate lengths from 45nm, 32nm, 22nm, 16nm and 10nm are chosen for this work. In this paper, we present the scalability aspects of DG-FinFET structures at different gate lengths. We also report a suitable high-k gate oxide material by examining the effect of wide range of high-k dielectrics on the DG-FinFET device parameters & SCEs using extensive 3-D device simulations by PADRE.

Table 1: Dimensions used for DG-FinFET simulations

Gate length-L_g(nm)	45nm	32nm	22nm	16nm	10nm
Fin Width-W_{fin}(nm)	15	11	8	7	5
Gate Oxide thickness-T_{ox}(nm)	1.5	1.2	1.1	1	1
Work function(ev)	4.6	4.6	4.6	4.6	4.6
V_{dd}(v)	1	1	1	1	1
FinHeight-H_{fin}(nm)	30	30	30	30	30

Simulations were performed for the proposed technology nodes with specifications matching the ITRS requirements.

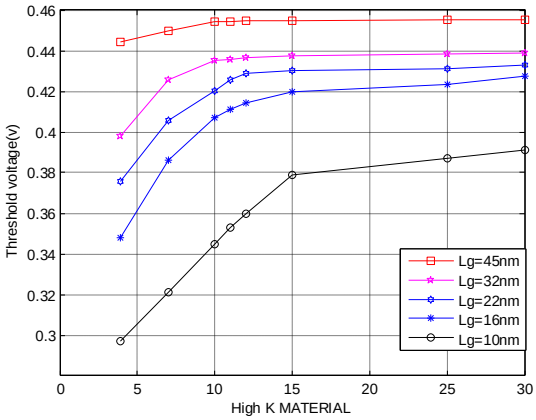

Fig.2: Plot showing effect on threshold voltage -Vth with increasing dielectric constant value K for various gate lengths

II. DEVICE STRUCTURE

The 3-D perspective view and the two dimensional cross section view of DG-FinFET structure are shown in fig.1. To meet the requirements of International Technology Roadmap for Semiconductors (ITRS), simulations have been performed for a wide range of proposed technology nodes (see Table-I) with proportionate device dimensions**.** Source and drain extension lengths are fixed to 30nm. The doping levels used in the channel and heavily doped source/drain regions were 1e+16/cm^3 and 1e+19/cm^3 respectively. The device structures correspond to the profile of Id-Vg characteristics as shown in fig.2.

III. DETAILS OF SIMULATION SETUP

Quantum-mechanical effects are taken care of in the simulation by including the nonlinear drift velocity model and Lombardi's transverse field dependent mobility model which includes the effect of Band to Band Tunneling (BBT), Band Gap Narrowing (BGN), Carrier-Carrier Scattering (CCS). To obtain accurate results for DG-FinFET simulation we need to account for the mobility degradation

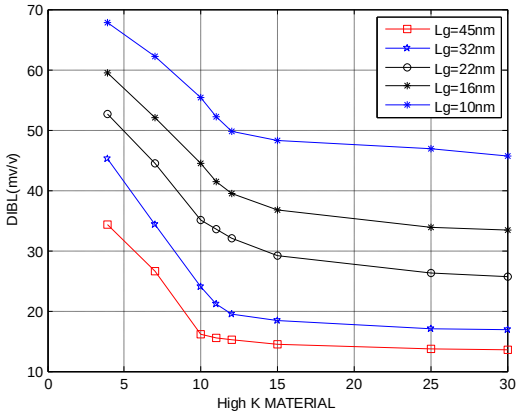

Fig.3: Plot showing effect on Drain Induced Barrier Lowering-DIBL with increasing dielectric constant value K for various gate lengths.

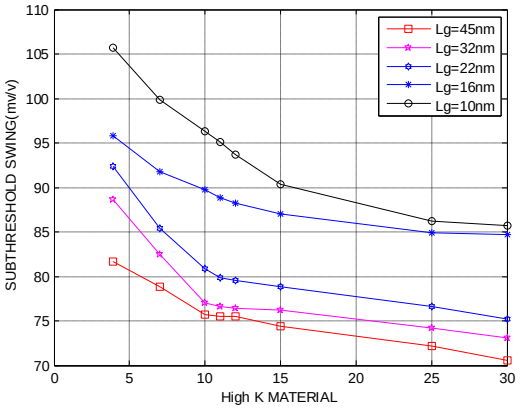

Fig.4: Plot showing effect on Subthreshold Swing-SS with increasing dielectric constant value K for various gate lengths.

that occurs inside inversion layers. The degradation normally occurs as a result of higher surface scattering near the semiconductor to insulator interface. The bulk mobility is computed through the model of Lombardi *et al.* X. Huang et al., IEDM, 1999 had shown the calibration of PADRE [9] with the experimental results. PADRE simulates quantum transport at the nanoscale, which is close to the atomistic dimension.

IV. EFFECT OF HIGH-K DIELECTRICS AS GATE OXIDE MATERIALS ON DG-FINFET DEVICE PARAMETERS

Simulations were performed for a wide range of proposed gate dielectric k values of 3.9, 7, 10, 11, 12, 15, 25 and 30. These dielectric constants correspond to SiO_2, Si_3N_4, Al_2O_3, $HfSiO_4$, $Gd2O_3$, Y_2O_3, HfO_2 and $LaAlO_3$ respectively.[6] In each simulation, the physical gate oxide thickness was proportionately

scaled such that Electrical oxide thickness (EOT) remains the same for particular gate length [1,2]. This analysis was carried out for 45nm to 10nm gate lengths of DG-FinFET Device and the impact of high-K on device performance is studied by extracting various device parameters.

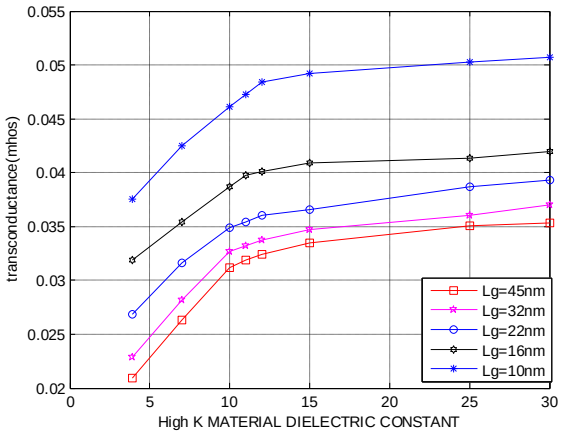

Fig.5: Plot showing effect on Transconductance-gm with increasing dielectric constant value K for various gate lengths.

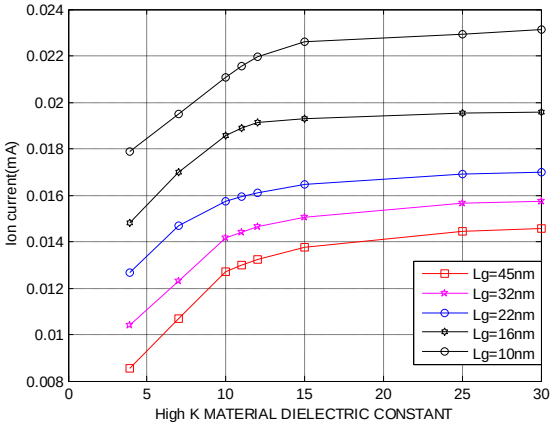

Fig.6: Plot showing effect on On Current-Ion with increasing dielectric constant value k for various gate lengths

The well known effect of "Threshold voltage roll-off" is examined for shrinking down DG-FinFETs from 45nm to 10nm with various high-k gate materials. Since the channel potential in short channel DG-FinFET is controlled by drain electric field, contribution of the gate potential required for channel inversion for attaining V_{th} reduces. Fig.2 depicts the fact that down scaling leads to threshold voltage degradation. Table II shows the impact of scalability and effects of DG-FinFET device parameters from 45nm to 10nm. It also shows a linear increase in threshold voltage with increasing k values for all the gate lengths. $LaAlO_3$ with k=30 as a gate material shows a low percentage increase for 45nm to 22nm, but shows around 66% increase for 10nm gate length in comparison with SiO_2. The simulation results proves that with 25<k<30 DG-FinFET shows a controlled performance in V_{th} at nanoscale gate lengths 22nm, 16nm and 10nm. Fig.3 and fig.4 depicts the major short channel effects DIBL and SS for various gate lengths with increasing dielectric constants. As the gate length shrinks from 45nm to 10nm DIBL and SS increases rapidly. DIBL and SS show an exponential decrease with increasing dielectric constants. Though SiO_2 (k=3.9) & Si_3N_4 (k=7) shows higher DIBL value in

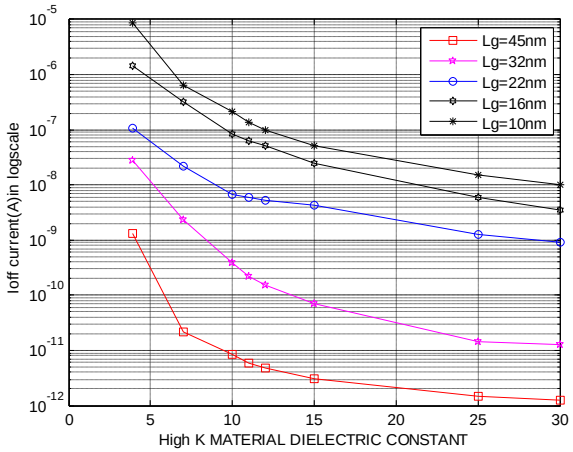

Fig.7: Plot showing effect on Off-state leakage current-Ioff with increasing dielectric constant value K for various gate lengths

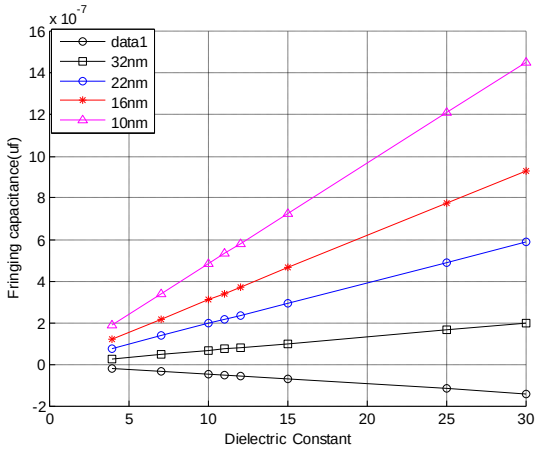

Fig.8: Plot showing effect on fringing capacitance with increasing dielectric constant value K for various gate lengths

Table 2: Impact of scalability and Parameter improvement/degradation from 45nm to 10nm in terms of Percentage for DG-FinFET device

Parameters	Effects	Improvement/Degradation from 45nm to 10nm in terms of Percentage
Vth	Decreases	33%
SS	Increases	30%
DIBL	Increases	146%
Ion	Increases	98%
Ioff	Increases	60%
Gm	Increases	71%
Cfr	Increases	45%

all gate lengths, a sufficient reduction up to 30mv/v is achieved in the range 7<k<15. A further reduction of 5mv/v can be achieved by $LaAlO_3$ (k=30) at all gate lengths. Similarly $LaAlO_3$ (k=30) yields a reduction of 15mv/dec in subthreshold swing for DG-FinFETs at 45nm to 16nm gate lengths as compared to SiO_2. At 10nm gate length it reduces subthreshold swing by 20mv/dec as compared to SiO_2. Materials with dielectric constants greater than

20 have shown a reduction in DIBL & subthreshold swing for better performance of DG-FinFETs.

Subha Subramaniam et al., Journal of Electron Devices **18**, 1582-1586 (2013)

Table 3: Improvement/Degradation of DG-FinFET parameters for various ranges of dielectric constants in comparison with SiO_2 (k=3.9) for all gate lengths in percentage

Parameters	Improvement / Degradation	Length: 45nm		Length: 32nm		Length: 22nm		Length: 16nm		Length: 10nm	
		3.9<k< 15	15<k< 30	3.9<k< 15	15<k< 30	3.9<k< 15	15<k< 30	3.9<k< 15	15<k< 30	3.9<k< 15	15<k< 30
Vth	Increases	2	2.5	12	15	28.7	30.2	20	22	53	66
SS	Decreases	7.6	8.3	14	17	25	28	8	11	8	30
DIBL	Decreases	58	61	61	65	68	71	38	43	22	35
Ion	Increases	61	69	44	50	29	34	30	33	8	10
Ioff	Decreases	90	99	85	99	80	98.9	75	99	70	99
Gm	Increases	60	67	47	61	33	55	36	42	37	46
Cfr	Increases	20	30	10	20	20	30	22	33	25	35

It is well known that the channel length with constant drain voltage, leads to increase in electric field in the channel. This situation leads to velocity saturation of carriers which limits the current and hence the transconductance. Transconductance should be always high enough to obtain a high current handling capability with low gate drive voltage. Fig.5 shows an exponential increase in gm values with increasing k values at gate lengths from 45nm to 10nm. SiO_2 shows degradation in gm value for all gate lengths. For 45nm and 32nm gate lengths better improvement in gm was achieved in the range 7<k<15. But the same amount of increase can be achieved in shorter gate lengths at 22nm to 10nm by using the range 25<k<30. Fig.6 proves the attribution that scaling down DG-FinFETs achieves higher On-current. It depicts an exponential growth of on-current with increasing k values. The greater capacitive coupling between gate and the channel in DG-FinFETs yields higher on-current and $LaAlO_3$ (k=30) as a gate material can yield an increase in on-current with suitable threshold and less leakage. The stand-by power of a chip is determined by the combined $I_{off\ of}$ all the transistors, and as such it must be minimized to integrate millions of transistors together. From Table III 60% increase in I_{off} is significant device degradation at 45nm gate length. Therefore, it is essential to incorporate high-k dielectrics for devices below 22nm gate lengths [8]. The result proves that $LaAlO_3$ (k=30) yields a minimal leakage. The magnitude of the fringing electric field depends upon the dielectric constant of the medium in which it is getting leaked. The fringing Electric field in a DG-FinFET depends upon the capacitance [7] which further depends upon the device doping, oxide thickness, dielectric constant of the oxide used, under lap length used for the device. The fringing field depends upon the dielectric of the medium in which the field is getting leaked, so the dielectric material used for the spacer decides the magnitude of the fringing field. Fig.8. shows the linear increase in fringing capacitance with increasing high k values [7]. As the fringing electric field also increases linearly with fringing capacitance, the degradation can be controlled by using HfO_2/$LaAlO_3$ as spacers which will reduce the fringing field effects [10,11].

IV. CONCLUSION

This paper proves that the Double Gate FinFET structure is scalable up to 10nm gate length. It has been shown that the dominating short channel effects due to down scaling in DG-FinFET devices significantly degrade their performance.

Integration of high-k gate material with high value of dielectric constant than SiO_2 helps to compensate this degradation. The simulation results prove that the degradation in the short channel performance can be improved by using high-k gate dielectric with k>25. So that HfO_2/ZrO_2 (k=25) and $LaAlO_3$ (k=30) can be chosen as a high-k gate material for improved performance in DG-FinFET devices below 22nm gate length. Zr and Hf are both from column I table. It was subsequently found that ZrO_2 is actually slightly unstable and can react with Si to form the silicide, $ZrSi_2$. For this reason, HfO_2 is presently the preferred high *K* oxide over ZrO_2. $LaAlO_3$ is closely lattice matched to Silicon and its oxides are stable next to Silicon. They have low oxygen diffusion coefficients, and it has a conduction band offset of about 1.8 eV. Lanthanides have the lowest leakage and have the highest figure of merit, so they could be the second generation high *K* oxides with lowest leakage for DG-FinFET devices below 22 nm. The simulation results proves that DG-FinFET structure can be scalable up to 10 nm by integrating high-k gate material ($k \geq 25$) with minimal short channel effects.

References

1. C. R. Manoj and V. Ramgopal Rao, "Impact of High-*k* Gate Dielectrics on the Device and Circuit Performance of Nanoscale FinFETs", IEEE Electron Device Letter **28**, 295-297 (2007).
2. Shishir Agrawal and Jerry G. Fossum, "On the Suitability of a High-*k* Gate Dielectric in Nanoscale FinFET CMOS Technology", IEEE Trans. on Electron Devices, **7**, 1714-1719 (2008).
3. H.S.P.Wong, "Beyond the conventional transistors", IBM J. Research and Development, **46**,133-168 (2002).
4. Kranti and G. A. Armstrong, "Performance assessment of nanoscale double- and triple-gate FinFETs," Semicond. Sci. Technol., **21**, 409-421 (2006).
5. Rakesh Vahid, Meenakshi Chandel, "Effect of Gate Length scaling on various performance parameters in DG-FinFETs: A simulation study", J. Nano Electronics and Physics, **4**, 1-6 (2012).
6. J. Robertson, "High dielectric constant oxides"**,** Eur. Phys. J. Appl. Phys. **28**, 265-291 (2004).
7. Bansal, B. C. Paul, and K. Roy, "Modeling and optimization of fringe capacitance of nanoscale DGMOS devices," IEEE Trans. Electron Devices, **52**, 255-262 (2005).

8. X. B. Lu, H. B. Lu, Z. H. Chen, "Field-effect transistors with $LaAlO_3$ and $LaAlO_xN_y$ gate dielectrics deposited by laser molecular-beam epitaxy", Appl. Phys. Lett. **85**, 35-43 (2004).
9. M.Mustafa, Tawseef Bhat, Beigh, "Threshold Voltage Sensitivity To Meatl Gate Work-Function Based Performance Evaluation of Double-gate N-FinFET Structures For LSTP Technology", World Journal of Nano Science and Engineering, **3**,17-22 (2013).
10. Zhao, H., Yee-Chia Yeo, Rustagi, S.C., Samudra, G.S., "Analysis of the Effects of Fringing Electric Field on FinFET Device Performance and Structural Optimization Using 3-D Simulation, "IEEE Transactions on Electron Devices, **55**, 1177-1184 (2008).
11. S L Tripathi, Ramanuj Mishra, R A Mishra, "Multi-gate MOSFET structure with high-k dielectric materials", Journal of Electron Devices, **16**, 1388-1394 (2012).