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# PERFORMANCE IMPROVEMENT OF FINFET USING SPACER WITH HIGH K DIELECTRIC

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**ABSTRACT**
This paper considers the performance improvement of FinFET using dual or triple material spacers and different combinations of the two or three dielectrics in a single spacer. The parameters measured are on/off currents DIBL and sub-threshold slope. The parameters are compared for dual and triple material spacers with high K material gate. All the simulations are performed on TCAD device simulator.
**Keywords*:*** FinFET, Fringing electric field, DIBL, Sub-threshold Slope, High K dielectric material, spacer

## I. INTRODUCTION

The use of high K materials in spacers [1,2] results in to the increase in on state current while off state current, sub-threshold slope and DIBL decreases, enhancing the FinFET performance due to the fringing electric field [3]. The magnitude of the fringing electric field depends upon the dielectric constant of the medium in which it is getting leaked. The fringing field increases with the use of high k dielectric material for spacer. The fringing Electric field in a FinFET depends upon the capacitance [4] which further depends upon the device doping, oxide thickness, dielectric constant of the oxide used, underlap length used for the device, etc. The fringing capacitance for the double gate FinFET is given by equation (1):

$$C_{fr} = k\varepsilon_{di} W \ln \pi W \frac{e^{-\left|\frac{L_{un}-T_{ox}}{L_{un}+T_{ox}}\right|}}{\sqrt{L_{un}^2+T_{ox}^2}} \quad (1)$$

where $\varepsilon_{di}$ is dielectric constant of the gate oxide, $W$ is width of the device, $L_{un}$ is underlap length and $T_{ox}$ is gate thickness.

As seen previously, the fringing field depends upon the dielectric of the medium in which the field is getting leaked, so the dielectric material used for the spacer is important in deciding the magnitude of the fringing field [5,6]. The use of high K dielectric materials such as $Si_3N_4$, $HfO_2$ improves the strength of the fringing electric field resulting in an increase of the on state current while the off state current, the sub-threshold slope and the drain induced barrier of the FinFET are decreased, thus resulting in improvements of the device [7,8]. In this paper the use of two or three different high K dielectrics in a single spacer is analyzed which has lead to further improvements in performances of FinFET structure.

## II. DEVICE DESIGN AND SIMULATION RESULTS

A FinFET with 20 nm channel length is used for the analysis. The channel of the FinFET is lightly doped with the concentration of $10^{15}$ $cm^{-1}$. The doping level in source and drain region is $10^{20}$ $cm^{-1}$. Gaussian doping is used in extension regions. The gate electrode thickness used is 40 nm while the spacer width is kept at 15 nm. The fin thickness used for the FinFET is 10 nm. The threshold voltage of the device is 0.2 V. All the simulations used in this paper are performed using the Sentaurus TCAD tools [9,10]. The FinFET structure is designed and simulated with single, dual and triple dielectric material spacers and their performances are compared for Ion/Ioff , DIBL and sub-threshold slope.

### II.1 Dual Material Spacer

The spacer with two different dielectrics is called as a dual material spacer. The different materials used here are Silicon Oxide and Silicon Nitride or Silicon Nitride and Hafnium Oxide or Hafnium Oxide and Silicon Oxide. The relative position of each material with respect to gate is varied and the performance is analyzed. The widths of each spacer material are 5 nm or 10 nm. FinFETs with dual material spacer for all these combinations are simulated and on state current, off state current, sub-threshold slope and DIBL are analyzed. Fig.1 shows the example of dual material spacer with dielectrics Silicon Nitride and Hafnium Oxide. For convenience the spacer is named as N10H5 where H5 indicates Hafnium Oxide of thickness 5 nm which is used close to the gate side while N10 indicates Silicon Nitride of thickness 10 nm used after the Hafnium Oxide dielectric material. Similarly, for S5H10 spacer H10 indicates Hafnium Oxide of thickness 10 nm being used close to the gate side while N10 means Silicon Nitride of thickness 10 nm and is used after the Hafnium Oxide dielectric material. The same rule is followed for other combinations such as N5H10, S5H10, etc. FinFETs performances with the dual material spacers are considered with respect to the on state current, off state current, sub threshold slope and DIBL. Values are tabulated in table I.

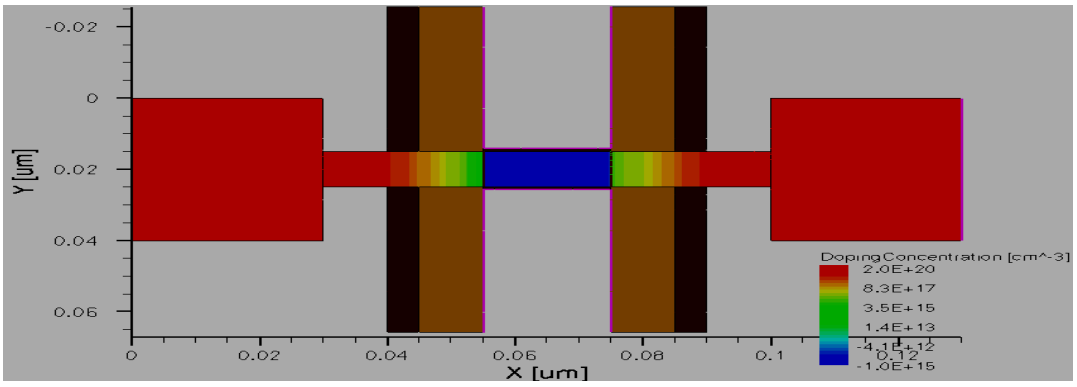


**Fig.1:** Dual material spacer of S5H10

Here, if we specifically consider Silicon Oxide and Silicon Nitride, or Silicon Nitride and Hafnium Oxide, or Silicon Oxide and Hafnium Oxide it can be seen that if we use higher K material (out of two dielectric materials used) immediate to the gate then the performance of dual spacer FinFET is comparatively better than when lower k

material used immediate to the gate. The performance of the dual material spacer of N10H5 is better than single material spacer of $SiO_2$ and $Si_3N_4$ described in previous section while it is not as good as single material spacer of HfO2. The off state current value obtained for S5H10 is lower than the single material spacers of Silicon Oxide, Silicon Nitride and Hafnium Oxide.

### II.2 Triple material spacer

The spacer with three different dielectrics in a single spacer is called as a triple material spacer. The use of triple material spacer is illustrated in the Fig.2 wherein $SiO_2$, $Si_3N_4$ and $HfO_2$ are used with the width of 5 nm each. Relative position of all the three dielectrics is changed and the performance is analyzed and tabulated in table II. Similar to the dual material spacer condition, S, N and H indicate $SiO_2$, $Si_3N_4$ and $HfO_2$ respectively. Thus, S5N5H5 mean, spacer material immediate to the gate is $HfO_2$, then $Si_3N_4$ and outermost is $SiO_2$ with the width of each material equal to 5 nm.

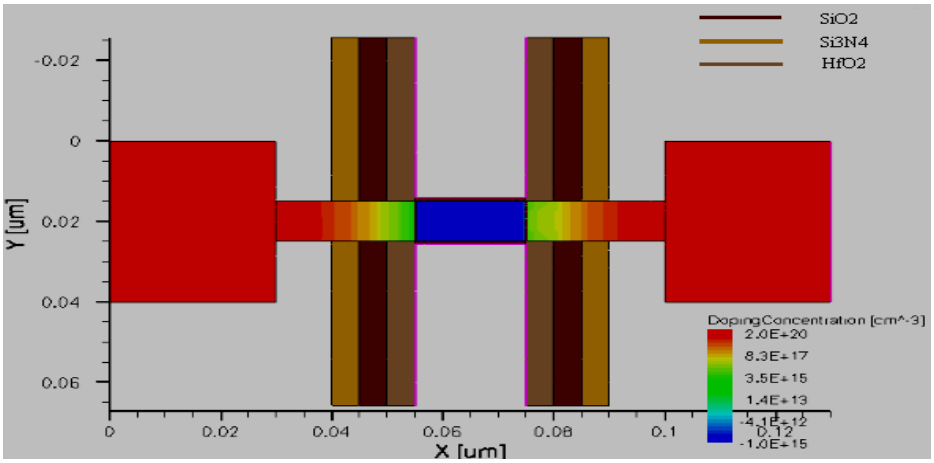


**Fig.2:** N5S5H5 spacer FinFETs

The on state current, off state current, sub threshold slope and DIBL for triple material spacer are tabulated in table II wherein it can be seen that the performance is best when high k dielectric is used immediate to the gate. The on-state current obtained in case of S5N5H5 spacer and single $SiO_2$ material is same, but there is improvement in other parameters such as off-state current, sub threshold slope and drain induced barrier lowering. That means, for the same drive current that off-state current, sub threshold slope and DIBL improve.

### II.3 Comparison of the Performances of Single, Dual and Triple Material Spacers

The performances comparison of single, dual and triple material are tabulated in table III. The maximum on state current is obtained with single material Hafnium Oxide spacer FinFET. The lowest off state leakage current is obtained using S5H10 dual material spacer. The highest $I_{ON}/I_{OFF}$ ratio is obtained for single material spacer FinFET of Hafnium Oxide followed by N10H5 spacer. The performances of dual and triple material spacer are better than single material spacer of $SiO_2$ and $Si_3N_4$. Also, the performance of dual material spacer is better than triple material spacer while the performances of triple material spacer are still better than single material spacers of $SiO_2$ and $Si_3N_4$. The combination of different materials in a FinFET facilitates the different current levels and performance

parameters. Thus, the dual and triple material spacers in FinFETs can be useful. Table III enables comparison of the single, double and triple material FinFET devices.

**Table I:** FinFET performances with dual material spacers

| Dual materials for spacer | Ion (mA) | Ioff (nA) | SS (mV/dec) | DIBL (mV/V) |
|---|---|---|---|---|
| N5S10 | 4.93 | 170 | 68.07 | 20.52 |
| N10S5 | 6.09 | 172 | 67.22 | 21.11 |
| H10S5 | 6.54 | 184 | 67.6 | 21.22 |
| H5S10 | 5.13 | 175 | 67.9 | 20.75 |
| S10H5 | 7.05 | 95.7 | 65.7 | 15.16 |
| S5H10 | 6.54 | 87 | 65.15 | 13.64 |
| N5H10 | 6.66 | 87.8 | 65.15 | 13.34 |
| N10H5 | 7.33 | 96.2 | 65.14 | 15.10 |
| H5N10 | 5.76 | 140 | 66.81 | 17.22 |
| H10N5 | 7.0 | 134 | 66.81 | 17.59 |
| S5N10 | 5.42 | 131 | 66.51 | 17.46 |
| S10N5 | 6.31 | 134 | 67.23 | 18.45 |

**Table II:** FinFET performances with different triple material spacers

| Triple spacer materials | Ion (mA) | Ioff (nA) | SS (mV/dec) | DIBL (mV/V) |
|---|---|---|---|---|
| N5S5H5 | 5.90 | 98.5 | 65.69 | 15.11 |
| S5N5H5 | 6.00 | 94.9 | 65.80 | 14.6 |
| S5H5N5 | 5.80 | 124 | 67.42 | 17.17 |
| H5S5N5 | 5.50 | 142 | 68.50 | 18.37 |
| N5H5S5 | 5.45 | 164 | 67.65 | 19.94 |
| H5N5S5 | 5.27 | 178 | 68.07 | 20.78 |

**Table III:** Comparison of performances with single, dual and triple material spacers

| Combination of spacer materials | Ion (mA) | Ioff (nA) | SS (mV/dec) | DIBL (mV/V) |
|---|---|---|---|---|
| $SiO_2$ | 5.98 | 162 | 67.39 | 20.418 |
| S22 | 6.48 | 134 | 66.036 | 18.36 |
| Hf2 | 8 | 92 | 65.92 | 13.35 |
| S5H10 | 6.54 | 87 | 65.146 | 13.34 |
| S5N5H5 | 6.02 | 94.9 | 65.8 | 14.6 |

## III. CONCLUSION

Use of dual, triple spacer material and different combinations of the two or three dielectrics in a single spacer, facilitates the different values of on-state and off-state currents. For dual and triple material spacers performance is best when a high K material is used immediate to the gate and is better than the single material spacers of $SiO_2$ and $Si_3N_4$. Also the performance of dual material FinFET is better than the triple material FinFET.

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