Journal of Electron Devices, Vol. 17, 2013, pp. 1406-1411

© JED [ISSN: 1682 -3427 ]

Journal of Electron Devices
www.jeldev.org

# FABRICATION POSSIBILITIES OF METAL SOURCE/DRAIN SCHOTTKY FETS USING WET CHEMICAL ETCHING TECHNIQUE ON p-TYPE (100) SILICON

**A. A. Sadiqa, B. S. Naseem, F.Iqbal***

Centre of Excellence in Solid State Physics, University of The Punjab, Lahore, Pakistan

*University of Engineering and Technology. Lahore. Pakistan

ayeshacssp@gmail.com

*Received 27-12-2012, revised 14-01-2013, online 17-01-201*

## ABSTRACT

The Schottky source/drain field effect transistor was fabricated, structural and electrical behavior was investigated and different device parameters were determined. Wet chemical etching technique was used to form the desired structure on the face of the silicon wafer. Structural characterization includes examination of wafer with profilometer and optical microscope at different magnifications. Titanium metal in pure form was evaporated source and drain of FET to form Schottky contacts. Current-Voltage (C-V) and Capacitance-voltage (I-V) measurements were performed at different applied drain voltages. The ideality factor yielded by I-V characteristics was 1.18 and barrier heights are 0.49eV and 0.34eV by I-V and C-V curves.

**Keywords:** Schottky FET, Wet chemical etching, Fabrication, Electrical characterization.

## I. INTRODUCTION

The efficacious demand for smaller, efficient and inexpensive computing devices has brought the semiconductor industry to its present arena, as well as drastically increases the microprocessor's applications. Traditional MOSFETs regulate the thermal barrier to carry the switching. As this is a thermal barrier so extremely sensitive to ambient temperature. The slight change into temperature cause anomalous change in the current as discussed by Wessely Rapsal [1].

The source/body and drain/body regions in conventional transistors are oppositely doped, so, a built-in potential barrier appears at junctions. The depletion region intrudes into the body region and decreases the length of the channel for gate control. The solutions proposed to these problems are, to decrease the thickness of the gate oxide and to increase the dopant concentration in body region. The decrease in thickness causes the increase in the gate capacitance and higher dopant concentration causes high mobility of charge carriers. Higher dopant concentration increases the scattering as discussed by Vega [2].

Metal source/drain Schottky Field Effect Transistors (MSD SFET) have been anticipated as substitute to the conventional Transistors because of its immense scaling properties and ease of fabrication as discussed by Calvet and Tucker [3]. The Schottky FET was proposed and demonstrated by Lepselter and Sze in 1968 [4].While early devices show low drive currents as discussed by elsewhere [5]. The advantage of Schottky FET includes simple fabrication and do not require any ion-implantation and high temperature anneals as discussed by Wessely and Raspal [1]. It also form abrupt junction at source/body and drain/body junction, which makes the transistor less susceptible to short channel effect as described in many research papers [6-8].

The MSD SFET has metal source and drain. A Schottky barrier is formed using correct type of metal and correct type of semiconductor [4]. A gate region is evaporated perpendicular to the source/body and drain/body junctions changes the dimensions of barrier at junctions. So the interface becomes less and more resistive to applied voltage as described by Vegs [2]. Metal silicides are the most frequently used materials for the source and

drain junctions Silicides discussed in literature by many writers [8-11]. Metal source/drain FET (MSD FET) presented in this paper made use of pure metals for the source and drain , so, the succeeding heating steps are useless, thus decreasing the manufacturing cost described by Tucker and Winstead [12-13]. Metal/III-V Schottky barrier FETs, MSD FETs using ultrathin gate-contacts and silicon on insulator (SOI) technology are the recent developments in this arena as discussed by Tucker, Frenzel and Hu [14-16].

## II. EXPERIMENTS

### II.1 Cleaning

The Schottky source/drain field effect transistor (FET) in this experiment was fabricated using P-type Silicon (100) having resistivity (0.047 Ω-cm) and with 0.1397 mm thickness. The procedure of producing smooth and clean surfaces plays very significant role in modern microelectronic industry. To remove the native layer of silicon oxide ($SiO_2$) from the silicon wafer surface hydrofluoric acid (HF) is most frequently used chemical. However, since 49% HF etches silicon dioxide so rapidly that is difficult to control it is rarely used in full strength. HF etching was followed by degreasing consecutively in trichloroethylene and acetone for 10 min. XP-1 profilometer was used to study the surface roughness of the wafer after the cleaning.

Examination of the Si wafer with profilometer is shown in fig.1 the fluctuations on the wafer are up to 6nm which confirms the smooth surface of wafer. After cleaning, the wafer was pre-baked at 80°C for 30 minutes to ensure that the wafer was completely dry. Any moisture on the surface of the wafer will interfere with the further manufacturing processes and cause the poor results. To form the structure on the Silicon wafer wet chemical etching was used because of it is cost effectivel, reliable and easy in use as discussed by Steinert [17].

### II.2 Etching

We used the chemical etchant and mixture of NH4F, Deionized water and $HNO_3$ was used. Photoresist was used as a mask to protect the

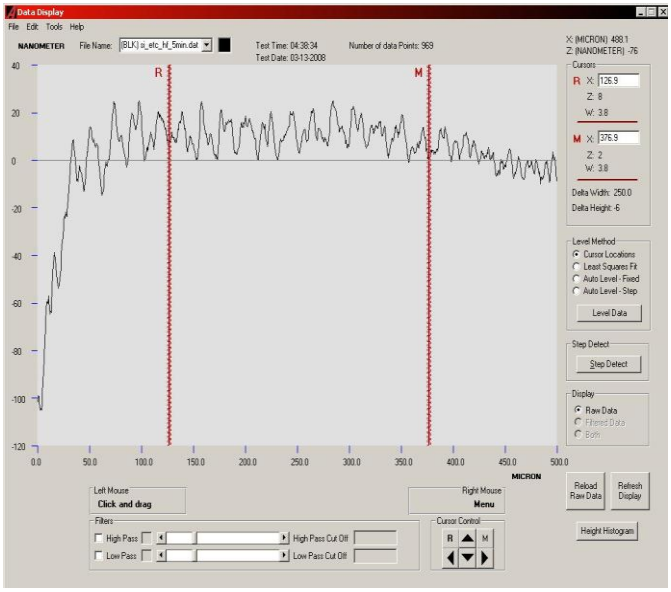


**Figure 1:** Surface Profile of the Si wafer after cleaning.

desired area on wafer surface and proved its reliability during the etching processes. Resist coating, or the procedure of producing a uniform, adherent, and defect-free resist film of correct thickness upon the wafer, was performed by spin-coating. Spin-coating processes were conducted at spin speeds of 2000 rpm for duration of 30 seconds. All the spinning process was done by Suss Microtech 6RC spinner

The mask will define the areas that will be exposed to chemical mixture and which will be covered. Resist coating is followed by a post bake, which is done to evaporate the solvent from the spun-on resist and adhesion improvement of the resist to the wafer. The post bake was done at 180°C for 30 minutes in post-bake hot-plate oven which provides well-control and Wafer surface for different concentration of the chemical solution was etched and examined by profilometer. Acid etching of silicon in the solution $HF/HNO_3/H_20$ was first studied by Robbins and Schwartz [18, 19]. The real

reaction mechanism is complicated which includes many elementary reactions. Different oxides of nitrogen and hydrogen can evolve as described by Kulkarni [20].

Uniform distributed of temperatures and a bake environment that provides a high degree of cleanliness as described by Wolf [21].

$$Si + 4HNO_3 \longrightarrow SiO_2 + 4NO_2 + 2H_2O \quad (1)$$

$$SiO_2 + 6HF \longrightarrow H_2SiF_6 + 2H_2O \quad (2)$$

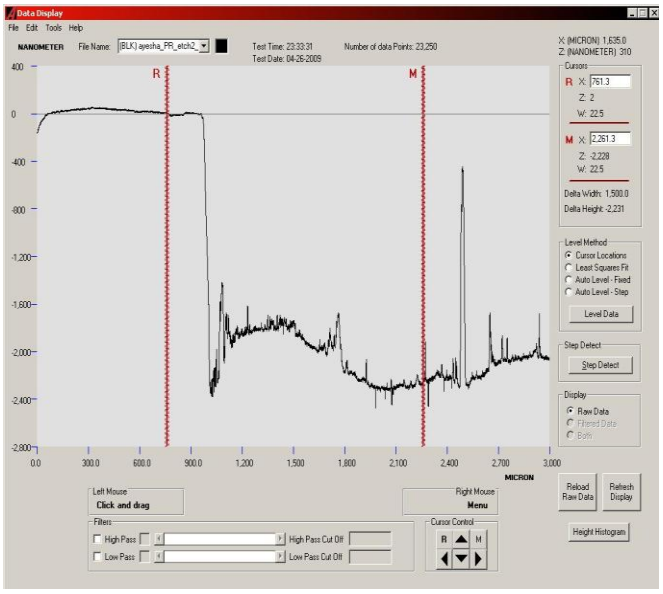


**Figure 2:** Etching Profile of Si wafer when solution concentration was 40% and exposure time was 15min.

Figure 2 describes the surface profile of the wafer surface when the etchant solution concentration was 40% and wafer was etched for 15 minutes. In graph a sharp fall at 900 microns shows the depth of etched pit 2,261.3 nm. The etching rate calculated from the result is 150nm per minute. It confirms the appropriate solution concentration. Figure 3 shows the etching profile of the silicon wafer which was etched for 1 minute in 40% concentrated solution at room temperature.

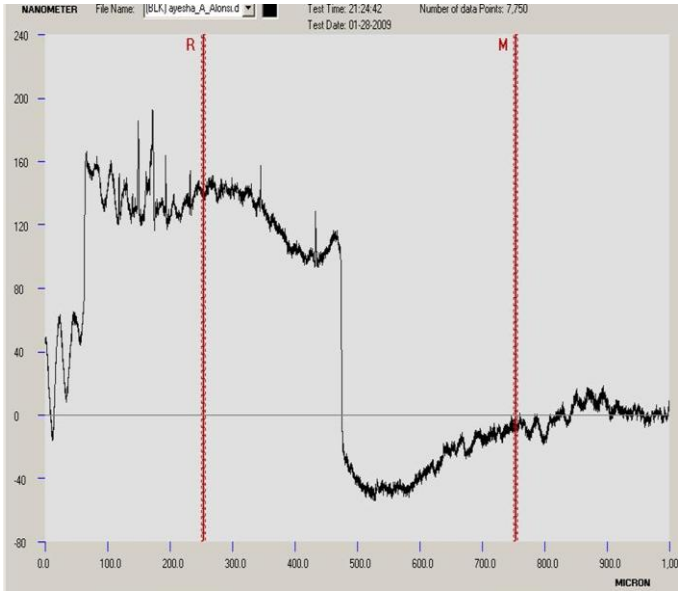


**Figure 3:** Etching profile of the Si wafer at 40% concentration of solution and expoure time was 1 min.

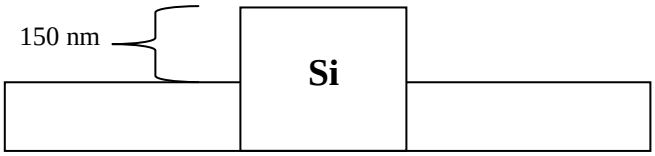


**Figure 4:** Schematic diagram of the Silicon wafer after the wet chemical etching.

## II.3 Structural Characterization

After forming the source and drain pits with chemical etching, Titanium metal was thermally evaporated to form the Schottky contacts at source/body and drain/body junctions and aluminum was evaporated to form ohmic contacts with the gate of the device with the help of metal mask which was used to expose only the gate area on the face of wafer.

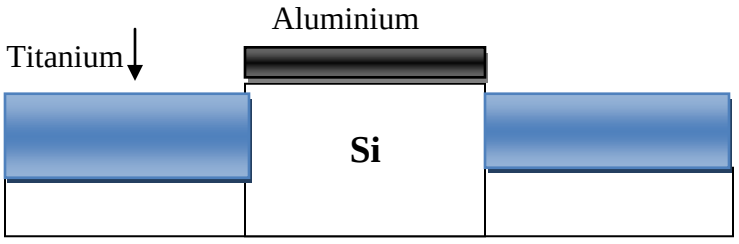


**Figure 5:** Schematic diagram of device with evaporated Titanium in the pits to form Schottky contacts.

Structural characterization also includes optical micrograph. Optical micrographs were taken by Leica DM4000 M optical microscope.

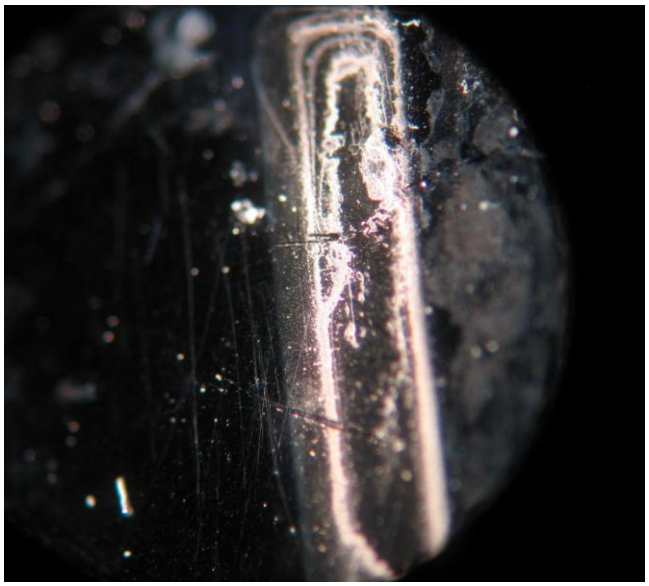

**Figure 6:** Optical micrograph of the device at 100X

All evaporation procedures were carried out by Edward 306 thermal coating unit at about $10^{-6}$ Torr. Figure 6 is the micrographs of Schottky FET. Aluminum gate is shown perpendicular to the channel and the length of the gate is 350 micrometer. Gate length can be reduced by using techniques like lithography. Source and drain areas covered with evaporated Titanium can be seen reflecting bluish color.

## III. RESULTS AND DISCUSSION

In electronics, the relationship between the DC current through an electronic device and the DC voltage across its terminals is known as current – voltage characteristic of the device. These characteristics are also known as I-V curves, referring to the customary symbols use for current and voltage respectively as described by Streetman [22].

The I-V and C-V measurements of Schottky FET were measured with Keithley instrument 4200 semiconductor characterization system parameter analyzer.

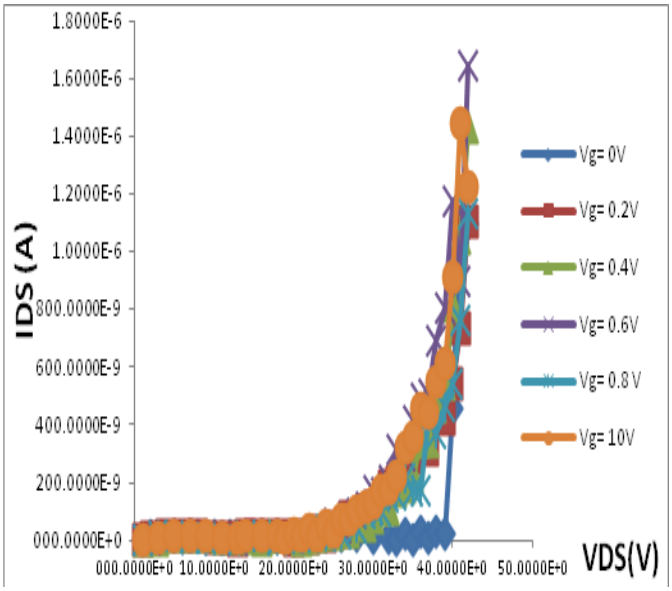


**Figure 7:** Current-Voltage characteristics of Schottky FET for negative gate voltage.

IDS (A) and VDS (V) plots are shown for different gate voltages ranging from 0 V to 1.0 V and step width is 0.2 V. These are not the typical FET plots. For zero gate voltage, plot describes a diode like characteristics. When the gate voltage is increased above zero, there is reasonable increase in the current. At 40 V the value of the current is $100.10^{-9}$ nA. But with further increase in gate voltage current is not increasing successively. A fluctuation of current can be observed in the curves. The current is 1.6 µA for Vg=0.4 V and 1.4 µA for Vg=10 V. The results imply the lack of gate control over the device.

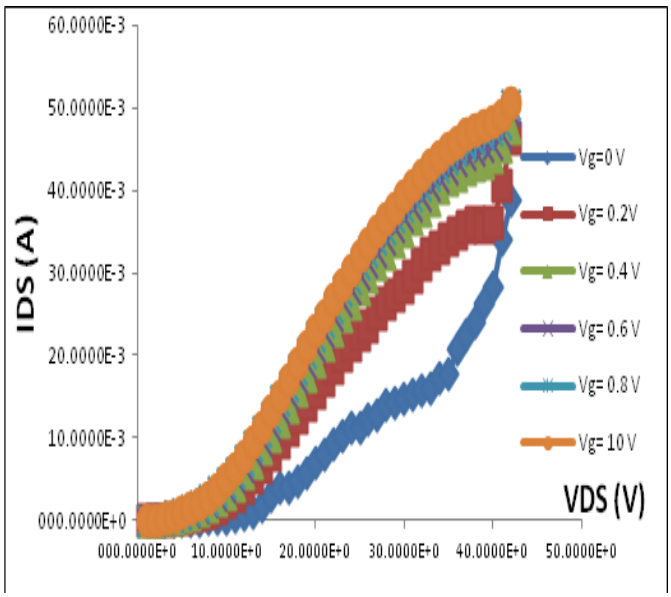


**Figure 8:** I-V characteristics of the Schottky Fet with positive gate voltage.

Fig10 shows the I-V characteristics of the same Schottky Transistor but with positive gate voltage. These characteristics are like typical MOSFETs characteristics. There is a successive increase in the current with gate voltages. All the graphs are clearly separated and can distinguish from each other. We can conclude from the I-V characteristics that transistor is Schottky MOSFET rather than the Schottky FET. The reasons for oxide layer between gate and silicon substrate is the oxide layer may grow again because of the time spend between cleaning and the growth of the gate metal.

The non-ideal behavior in Schottky FETs is attributed by the effect of interfacial layer present at the interface of metal and semiconductor contact as discussed by streetman and Sugimura [22, 23]. Performanc of Schottky FETs strongly depends upon interface states and their distribution of energy. The states present at the interface can increase trapping, scattering and recombination, all of which change the current-voltage (I-V) and capacitance-voltage (C-V) characteristics of Schottky FETs. The interface states impart an essential role in the determination of barrier height. The energy distribution of interfaces states in a semiconductor band gap plays a crucial role in the properties of a metal semiconductor barrier and these interface states may affect the deviations of the differential capacitance measured at the forward bias. The interface states have been considered localised at the oxide semiconductor edge. The energy and distribution of these states is reliant on the metal contact and on the quantity of thermal annealing discussed in Chattopadhyay and Ozdimir [24, 25].

Large information about the MOS device and the oxide-semiconductor interface can be gathered from the capacitance - voltage (C-V) characteristic of device as discussed by Zamora and Neeman [26, 27].

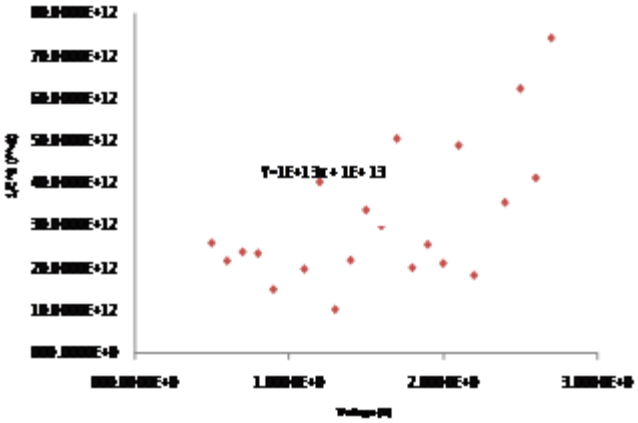

**Figure 9:** Capacitance-Voltage characteristics of Schottky FET.

Figure 9 shows the graph between capacitance and voltage. The points are scattered and not perfectly align in a straight line. It can be stated that the slope of the C-V curves changes appreciably due to ionized defect centers for. A strong effect due to a change of concentration on ionized deep traps on the capacitance measurements.

The ideality factor found by I-V characteristics curve is 1.18 and barrier heights are 0.49 eV and 0.34 eV by I-V and C-V curves. Built-in potential ($V_{bi}$) is 0.7 V and carrier concentration ($N_d$) is 3 x $10^{13}$ $cm^{-3}$. The value of barrier height found by I-V and C-V curves is in agreement with each other.

## IV. CONCLUSION

The Schottky Source/Drain FET was fabricated and structural and electrical characteristics were measured and investigated. The results indicate that the value of the barrier height calculated by Current-Voltage and Capacitance-Voltage characteristics are agreement with each other and non-ideality was attributed by interface states and interfacial layers.

### References


[1] F. Wessely, L. Rispal, U. Schwalke, "Mix-and-Match Lithography Based Ultrathin-body SOI Nanowires and Schottky-S/D-FETs", J. Vacc. Tech. B., **27**, 478-481 (2007).

[2] R. A. Vega, "Metal Source/Drain Schottky Field Effect Transistors and Schottky CMOS Circuitry", IEEE Trans. Elec. Dev., **55**, 2665 (2008).

[3] L. E. Calvet, H. Luebben, M. A. Reed, J. R. Tucker, C. Wang, J. P. Snyder, "Electron transport measurements of Schottky barrier inhomogeneities", J. Appl. Phys. Lett., **80**, 1761 (2002).

[4] M. P. Lepselter, S. M. Sze, "Suppression of leakage current in Schottky barrier metal-oxide-semiconductor field effect transistors", IEEE Proc. Lett., **56**, 1400 (1968).

[5] S. M. Sze, "Physics of Semiconductor Devices", 2nd Edition, John Wiley & Sons, **245**, 491 (1981).

[6] Z. Zhang, "Integration of silicide nanowires as Schottky barrier source/drain in FinFETs". Ph.D thesis, Royal Institute of Technology. Sweden, (2008).

[7] C. Wang, J. P. Snyder, J. R. Tucker, "Electron transport measurement of Schottky barrier inhomogenities", Appl. Phys. Lett., **74**, 1174 (1999).

[8] M. Jang, Y. Kim, M. Jun, S. Lee, "Catalyst-free Growth of Single-Crystal Silicon and Germanium Nanowires", Nano. Lett., **9**, 864 (2009).

[9] M. Jang, M. Jun, Y. Choi, S. Choi, "20-nm-gate-length erbium-/platinum-silicided n-/p-type Schottky barrier metal-oxide-semiconductor field-effect transistors", Appl. Phys. Lett., **93**, 192 (2008).

[10] C. Wang, J. R. Tucker, "Sub-40 nm PtSi Schottky source/drain metal-oxide-semiconductor field-effect transistors", Appl . Phys. Lett., **74**, 1174 (1999).

[11] J. P. Snyder, C. R. Helms, Y. Nishi, 2An MOS transistor with Schottky source/drain contacts and a self-aligned low-resistance T-gate", Appl. Phys., **35**, 361, (1997).

[12] J. Kedzierski, P. Xuan, V. Subramanian, J. Bokor, T-J King, C. Hu, "20 nm Gate-Length Ultra-Thin Body p-MOSFET with silicide source/drain", Superlattices and microstructures., **28**, 445 (2000).

[13] D. Winstead, U. Ravaioli, "Towards a compact model for Schottky-barrier nanotube FETs", IEEE Trans. Elec. Dev., **47**, 303 (2002).

[14] J. Hu, K. C. Saraswat, H. S. P. Wong, "Metal/III-V Schottky barrier height tuning for the design of nonalloyed III-V field-effect transistor source/drain contacts", J. Appl. Phys. Lett., **107**, 063712 (2010).

[15] J. R. Tucker, C. Wang, T. C. Shen, "Metal silicide patterning: a new approach to silicon nanoelectronics", Nanotechnology, **7**, 275 (1996).

[16] H. Frenzel, A. Lajn, H. V. Wenckstern, M. Grundmann, "Recent Progress on ZnO-Based Metal-Semiconductor Field-Effect Transistors and Their Application in Transparent Integrated Circuits", Advance Mat. **89**, 114515 (2010).

[17] M. Steinert, J. Acker, K. Wetzig, "Reactive Species Generated during Wet Chemical Etching of Silicon in $HF/HNO_3$ Mixtures", J. Phys. Chem B., **110**, 11377-82 (2006).

[18] H. Robbins, B. Schwartz, "Chemical etching of Silicon II". J. Electrochem, Soc., **107**, 108 (1960).

[19] H. Robbins, B. Schwartz, "Chemical etching of Silicon II", J. Electrochem. Soc., **108**, 365 (1961).

[20]M. S. Kulkarni, H. F. Erk, "Acid-based etching of silicon wafers: Mass-transfer and kinetic effects", J. Electrochem. Soc., **147**, 176 (2000).

[21] S. Wolf, R. N. Tauber, "Semiconductor manufacturing wafer process", 2nd Edition, Lattice press, (2000).

[22] B. Streetman, S. Banerjee, "Solid State Electronic Devices", 5th Edition, Prentice Hall. (1999).

[23] T. Sugimura, T. Tsuzuku, Y. Kasai, K. Liyama, 2I–V Characteristics of Schottky/Metal-Insulator-Semiconductor Diodes with Tunnel Thin Barriers", J. Appl. Phys., **39**, 4521 (2000).

[24] P. Chattopadhyay , "Admittance of metal–insulator–semiconductor tunnel contacts in the presence of donor–acceptor mixed interface states and interface reaction", J. Appl. Phys., 89, **364** (2001).

[25] A. F. Ozdemir, A. Turut, A. Kokce, "The interface state energy distribution from capacitance–frequency characteristics of goldy n-type Gallium arsenide Schottky barrier diodes exposed to air", Thin Solid Films, **425**, 210 (2002).

[26] M. Zamora, J. Gazecki, G. K. Reeves, "Interface states capacitance in AuPtTi/nGaAs Schottky contacts--a modified Schottky capacitance spectroscopy method, Solid-State Electron". Solid-State Electron., **38**, 1771 (1995).

[27] D. Neamen, "Semiconductor physics and devices", 3rd Edition, McGraw Hill. (2002).