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ANALYTICAL MODELING OF CROSSTALK NOISE AND DELAY FOR HIGH SPEED ON-CHIP GLOBAL RLC VLSI INTERCONNECTS

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ABSTRACT

With the advancement of high frequency in the VLSI technology, the modeling of the interconnections is much important as the performance of the electronics systems is limited by interconnect related failure modes such as coupled noise and delay. Exact estimation of on-chip signal delay through RC tree network is difficult. Inductance causes noise in the signal waveforms, which can adversely affect the performance of the circuit and signal integrity. In this research article, analytical expressions for crosstalk noise voltage and delay are derived for the high speed VLSI RLC global interconnects. This work presents an accurate and efficient model to compute the crosstalk noise and delay of the high-speed RLC interconnections. We analyze L type interconnect models in deriving analytic expressions for peak noise voltage and delay.

Keywords: Crosstalk, Delay Modeling, RLC interconnect, VLSI

I. INTRODUCTION

VLSI began in early 1970s when complex semiconductor and communication technologies were being developed. The process of fabrication of integrated circuits by combining hundreds of thousands of transistors into a single chip is usually referred to very-large-scale-integration (VLSI). Now a day, VLSI circuits and integrated circuit (IC) chips find application in numerous fields like mobile and satellite communication, computer hardware, micro-electromechanical systems (MEMS) devices, robotics and other electronic systems. VLSI circuit density and complexity has exponentially increased over the years leading to miniaturization of electronic systems, increase in speed of production from circuit specifications to actual hardware development and a resulting decline in prices of electronic devices. With the increase in speed of high performance VLSI circuits, inductance and conductance effect of interconnects are becoming more and more important and can no longer be neglected. Under these circumstances, the Elmore model [1] is inadequate since this model takes only the resistance and capacitance effects into account. The rapid decrease in featured size has followed by a commensurate increase in operating frequencies [2]. At Gigahertz range [3] frequencies design of clocks has been very critical which mainly determines the speed of operation of such circuits. As anticipated by Moore's law, the number of transistors in an integrated circuit (IC) has doubled every two to three years. Modern ICs are now composed of millions of transistors switching simultaneously within a fraction of a second. There are several approaches proposed to estimate the on-chip interconnect performance characteristics; where the interconnect is modeled as distributed RC [4-7], RLC [8-11], The following contributions have been made in this paper: a closed form expression for delay metric and crosstalk peak noise voltage for on-chip RLC VLSI interconnect using L-type network model has been proposed.

The rest of the paper is organized as follows: basic theory of transmission line when considered as a distributed RLC model is discussed in section 2. Section 3 discusses proposed crosstalk noise and aggressor line voltages and peak time delay model of RLC interconnection network is given. In section 4, Simulation results are shown and discussed and finally section 6 concludes the paper.

II. BASIC THEORY

Defining the point at which an interconnect should be treated as a transmission line and hence reflection analysis applied, has no consensus of opinion. A rule of thumb is that when the delay from one end to other is greater than rise-time/2, the line is considered electrically long. If the delay is less than rise time/2, the line is electrically short [12].

An interconnect line [13] can be described at the circuit level using series inductance and resistance combined with shunt capacitance and conductance. But at the frequency of operation used in today's DSM technologies, the conductance could be neglected. An infinitesimal unit length of the transmission line looks like the circuit in Figure 1. Where the different distributed parameters are defined as,

R = Series resistance per unit length
L = Series inductance per unit length
C = Shunt capacitance per unit length.

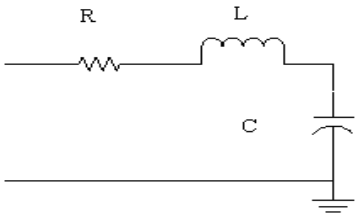

Figure 1: RLC parameters of a segment of a transmission line

It is critical to model the transmission path when designing a high-performance, high-speed serial interconnection system. The transmission path may include long transmission lines, connectors, vias and crosstalk from adjacent interconnects. Values [14] for R, L, and C are extracted automatically. The extracted values for the parameters R, L, C for 180 nm technology are shown in Table 1.

Table 1 RLC parameters of a minimum sized wire in a 180 nm technology

Parameter(s)	Value/m
Resistance(R)	120 kΩ/m
Inductance(L)	270 nH/m
Capacitance(C)	240 pF/m
Coupling Capacitance (C_c)	681.23 pF/m

III. PROPOSED MODEL

This section contains L model to represent the RLC interconnect between the driver and the load as shown in the Figure 2. In this paper, for the estimation of the peak noise voltage and delay we discuss the case when the victim line is quiet and the aggressor line is switching. In our analysis, we consider the step input regime and we take driver resistance and load capacitance into account when deriving closed form expressions for peak noise voltage and delay.

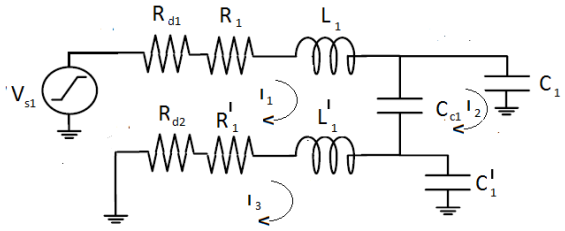

Figure 2: Equivalent RLC Circuit using L model for Interconnect

In the circuit shown in the Figure 2, we compute the voltage at the aggressor line output at node C on the victim line. Using the nodal analysis at node B & C, we get the nodal equations at node B & C as follows:

Applying KVL in the 1st mesh

$$V_{s1} = I_1 R_{d1} + I_1 R_1 + L_1 \frac{dI_1}{dt} + \frac{1}{c_1}\int (I_1 - I_2)dt \tag{1}$$

Taking Laplace transform of the equation (1)

$$V_{s1}(s) = I_1(s)R_{d1} + I_1(s)R_1 + sL_1 I_1(s) + \frac{1}{sc_1}\int (I_1(s) - I_2(s))dt \tag{2}$$

After simplification we can write

$$V_1(s) = \frac{(M_1 sc_1 + 1)I_1(s) - I_2(s)}{sc_1} \tag{3}$$

where $M_1 = R_{d1} + R_1 + sc_1$ (4)

Applying KVL in the 2nd mesh

$$\frac{1}{sc_1}(I_1(s) - I_2(s)) = \frac{1}{sC_{c1}} I_2(s) + \frac{1}{sc_1'}(I_2(s) + I_3(s))$$

$$\frac{1}{sc_1} I_1(s) - \left(\frac{1}{sc_1} + \frac{1}{sc_1'} + \frac{1}{sC_{c1}}\right) I_2(s) - \frac{1}{sc_1'} I_3(s) = 0 \tag{5}$$

Similarly applying KVL in the 3rd mesh

$$0 = I_3(s)R_{d2} + I_3(s)R_1' + sL_r' I_3(s) + \frac{1}{sc_1'}(I_2(s) + I_3(s)) \tag{6}$$

After simplification we can write the above equation (6)

$$I_2(s) + (sM_2 c_1' + 1)I_3(s) = 0 \tag{7}$$

where $M_2 = R_{d2} + R_1' + sL_r'$ (8)

After putting the values of $I_3(s)$ and $I_1(s)$ from equations (3) and (7) in equation (5), we get

$$V_1(s) = \frac{s^2 M_1 M_2 \alpha + \beta s + 1}{sC_{c1}(sM_2 c_1' + 1)} I_2(s) \tag{9}$$

where

$$\begin{cases} \alpha = c_1 c_1' + c_1 C_{c1} + c_1' C_{c1} \\ \beta = M_1 c_1 + M_2 c_1' + M_1 + M_2 . \end{cases} \tag{10}$$

From equations (7) & (9), we can write for $I_3(s)$ as bellow

$$I_3(s) = \frac{-sC_{c1}V_{s1}}{1 + \beta s + s^2 M_1 M_2 \alpha} \tag{11}$$

Now calculating voltage at node c as shown in figure (2), we can write

$$V_c = \frac{1}{sc_1^{'}}\left[I_2(s) + I_3(s)\right] \tag{12}$$

From equations (9), (11) and (12), we can write for V_c

$$V_c = \frac{s(M_2C_{c1})}{1+\beta s + M_1M_2\alpha s^2}V_1(s) \tag{13}$$

Similarly we can calculate the voltage across node B

$$V_B = \frac{1}{sc_1}\left[I_1(s) - I_2(s)\right] \tag{14}$$

From equations (3) & (14), after simplification we can write

$$V_B = \frac{1+(\beta - M_1C_{c1})s + M_1M_2c_1(c_1^{'}+C_{c1})s^2}{1+(\beta+M_1c_1)s+(M_1c_1\beta+M_1M_2\alpha)s^2+M_1^2M_2^2c_1\alpha s^3}V_1(s) \tag{15}$$

We considered an aggressor line switching from low to high and a quiet victim line. For the quiet victim line, the input voltage V_{s2}=0 and for the aggressor line with step input, we have $V_1(s) = 1/s$.

After putting the value of $V_1(s) = 1/s$ in the equation (13)

$$V_c = \frac{s(M_2C_{c1})}{1+\beta s + M_1M_2\alpha s^2}.\frac{1}{s} \tag{16}$$

After simplification,

$$V_c(s) = \frac{c_{c1}/\alpha M_1}{\left[\left(s+\frac{\beta}{2M_1M_2\alpha}\right)^2 + \left(\sqrt{\frac{4M_1M_2\alpha-\beta^2}{4M_1^2M_2^2\alpha^2}}\right)^2\right]} \tag{17}$$

Taking the inverse Laplace transform of equation (17)

$$V_c(t) = \frac{C_{c1}}{2M_1}\frac{}{a}\,Sin\,at\,e^{-bt} \tag{18}$$

where $b = \frac{\beta}{2M_1M_2\alpha}$ & $\frac{1}{a} = \frac{2\alpha M_1M_2}{\sqrt{4M_1M_2\alpha-\beta^2}}$ (19)

On differentiating with respect to t,

$$\frac{dV_c(t)}{dt} = \frac{C_{c1}}{\alpha M_1 a}\frac{d}{dt}\left[\sin at\, e^{-bt}\right] \tag{20}$$

Taking first derivative and equal to zero for calculating peak time after simplification,

$$t_{pc} = \frac{1}{a}\tan^{-1}\left(\frac{a}{b}\right) \tag{21}$$

Put the peak time value in equation (18), after simplification

$$V_c(t)_{\max} = \frac{C_{c1}}{\alpha M_1\sqrt{a^2+b^2}}\; e^{-\frac{b}{a}\tan^{-1}\left(\frac{a}{b}\right)} \tag{22}$$

After putting the value of step input $V_1(s) = 1/s$ in equation (15)

$$V_B = \frac{1+(\beta - M_1C_{c1})s + M_1M_2c_1(c_1^{'}+C_{c1})s^2}{1+(\beta+M_1c_1)s+(M_1c_1\beta+M_1M_2\alpha)s^2+M_1^2M_2c_1\alpha s^3}\frac{1}{s} \tag{23}$$

After simplification

$$V_B(s) = \frac{1/M_1C_1}{s\left(s+1/M_1C_1\right)} - \frac{C_1^{'}C_{c1}\left(s+1/M_2C_1^{'}\right)}{M_1\alpha\, C_1\left(s+1/M_1C_1\right)\left(s^2+\frac{\beta}{M_1M_2\alpha}s+\frac{1}{M_1M_2\alpha}\right)} \tag{24}$$

For first term, using partial fraction

$$\frac{1/M_1C_1}{s\left(s+1/M_1C_1\right)} = \frac{1}{s} - \frac{1}{\left(s+1/M_1C_1\right)} \tag{25}$$

For second term,

$$\frac{C_1^{'}C_{c1}\left(s+1/M_2C_1^{'}\right)}{M_1\alpha\, C_1\left(s+1/M_1C_1\right)\left(s^2+\frac{\beta}{M_1M_2\alpha}s+\frac{1}{M_1M_2\alpha}\right)} \tag{26}$$

Using partial fraction, we have

$$C_{c1}\left[Y.\frac{(s+b)}{(s+b)^2+a^2} + \frac{X}{(s+b)^2+a^2}\right] \tag{27}$$

where

$$Y = \frac{M_1C_1 - M_2C_1^{'}}{M_2\alpha - \beta C_1 + M_1C_1^2} \quad \text{and} \quad X = \frac{2M_1 - 2M_1YC_1 - Y\beta}{2M_1M_2\alpha}$$

So, with equation (25) & (27), the equation (24) becomes,

$$V_B(s) = \frac{1}{s} - \frac{(1-C_{c1}Y)}{\left(s+1/M_1C_1\right)} - C_{c1}\left[Y.\frac{(s+b)}{(s+b)^2+a^2} + \frac{x}{(s+b)^2+a^2}\right] \tag{28}$$

Taking inverse Laplace,

$$V_B(t) = 1-(1-C_{c1}Y)\,e^{-\frac{t}{M_1C_1}} - C_{c1}Y\cos at\; e^{-bt} - \frac{x}{a}C_{c1}\sin at\; e^{-bt} \tag{29}$$

On differentiating with respect to time,

$$\frac{dV_B(t)}{dt} = \frac{(1-C_{c1}Y)}{M_1C_1}e^{\frac{-t}{M_1C_1}} + C_{c1}\left[\left(Ya + xb/a\right)\sin at + (Yb-x)\cos at\right]e^{-bt} \tag{30}$$

Taking first derivative and equal to zero for calculating peak time after simplification,

$$\frac{(1-C_{c1}Y)}{M_1C_1}e^{\frac{-t_p}{M_1C_1}} + C_{c1}\left[\left(Ya + xb/a\right)\sin at_p + (Yb-x)\cos at_p\right]e^{-bt_p} = 0 \tag{31}$$

Ignoring higher order term and after implification, we get

$$t_{pa} = \frac{M_1C_1YC_{c1} + C_{c1}Yb - M_1C_1 - xC_{c1}}{C_{c1} - C_{c1}Ya^2 + xbC_{c1} - C_{c1}Yb^2 + C_{c1}bx - 1} = \frac{z}{u} \tag{32}$$

where

$$z = M_1C_1YC_{c1} + C_{c1}Yb - M_1C_1 - xC_{c1}$$

$$u = C_{c1} - C_{c1}Ya^2 + xbC_{c1} - C_{c1}Yb^2 + C_{c1}bx - 1$$

Put the peak time value in equation (29), after simplification

$$V_B(t)_{\max} = 1-(1-C_{c1}Y)\,e^{-\frac{z}{M_1C_1u}} - C_{c1}Y\cos a\frac{z}{u}e^{-b\frac{z}{u}} - \frac{x}{a}C_{c1}\sin a\frac{z}{u}e^{-bt\frac{z}{u}} \tag{33}$$

The expressions given in equations (21), (22), (32) are (33) are the expressions for the estimation of peak delay time and peak voltages at node C and node B respectively. The expression given in equations (18) and (22) are the required crosstalk voltage and peak crosstalk noise voltages respectively at node C.

IV. SIMULATION RESULT AND DISCUSSION

For the validity and accuracy of our proposed crosstalk noise voltage and delay models, we have considered a RLC

capacitively coupled interconnect system as shown in the figure 2. Aggressor line is excited by a step input signal with finite rise time of 10 ps. We assume identical interconnects are driven by identical inverters of size, and also assume that the loads at the end of the lines are identically sized inverters. We simulate the coupled interconnects by using different input slew times ranging from 0ps to 200ps for the driving inverters. Our results for the L-interconnect model are discussed in Table 2 for the peak crosstalk noise voltage for different slew times of the input signal. These results are within 10 % of the values derived by SPICE.

Table 2 Comparative Result for Peak Crosstalk Noise obtained from Proposed Model and SPICE

R_{d1} (Ω)	R_{d2} (Ω)	C'_L (fF)	T_s=0		T_s=100		T_s=200	
			SPICE Values (mV)	Our Model (mV)	SPICE Values (mV)	Our Model (mV)	SPICE Values (mV)	Our Model (mV)
15	15	1.2	115	121	165	161	206	210
15	25	1.2	131	139	182	179	225	231
25	15	1.2	148	147	211	202	247	245
25	25	2.4	173	182	235	238	273	279
25	50	2.4	218	221	262	271	297	291

The comparative result for aggressor line voltage with SPICE values is discussed in Table 3 for the different input slew values. All the aggressor line voltages are measured in volts (V).

Table 3 Comparative Result for Agressor Line Voltage obtained from Proposed Model and SPICE

R_{d1}	R_{d2}	C_L	T_s=0		T_s=100		T_s=200	
			SPICE Values	Our Model	SPICE Values	Our Model	SPICE Values	Our Model
15	15	2.4	0.782	0.761	0.901	0.951	1.02	1.17
15	25	2.4	0.891	0.872	0.992	1.02	1.21	1.26
25	15	2.4	1.12	1.01	1.32	1.35	1.43	1.41
25	25	3.6	1.72	1.29	1.42	1.48	1.64	1.68
25	50	3.6	1.43	1.52	1.62	1.71	1.72	1.74

Table 4 and Table 5 give the comparative result of the peak times t_{pc} and t_{pa} for the victim line and aggressor line peak voltages respectively for the different slew times of the input signal. All the time values are measured in nanoseconds (ns).

Table 4 Comparative Result for Victim Line Peak time obtained from Proposed Model and SPICE

R_{d1}	R_{d2}	C'_L	T_s=0		T_s=100		T_s=200	
			SPICE Values	Our Model	SPICE Values	Our Model	SPICE Values	Our Model
15	15	1.2	21.34	23.12	38.21	37.73	61.17	59.29
15	25	1.2	29.23	27.34	47.32	48.24	78.21	77.92
25	15	1.2	37.42	39.71	72.23	73.84	96.33	98.28
25	25	2.4	42.51	45.64	89.47	91.27	107.23	105.37
25	50	2.4	61.27	59.69	102.12	103.12	112.19	118.23

Table 5 Comparative Result for Agressor Line Peak Time obtained from Proposed Model and SPICE

R_{d1}	R_{d2}	C'_L	T_s=0		T_s=100		T_s=200	
			SPICE Values	Our Model	SPICE Values	Our Model	SPICE Values	Our Model
15	15	1.2	11.93	10.64	27.32	28.43	47.32	46.54
15	25	1.2	23.64	25.32	35.72	36.21	58.35	59.32
25	15	1.2	35.32	38.65	48.17	47.32	72.67	73.72
25	25	2.4	57.21	55.23	61.74	65.81	81.37	82.82
25	50	2.4	69.72	68.84	72.45	75.32	98.71	99.32

V. CONCLUSION

In this paper, we presented the problem of crosstalk noises in high-speed RLC coupled interconnect systems. Simulation result shows that the proposed model for crosstalk noise voltage is most accurate and efficient. In this paper we considered unit step input excited aggressor line which is present near the victim net. The proposed model is based on the L-type interconnect RLC network. Simulation results demonstrate the validity and correctness of our method. This work can be used in much other application at various levels to guide noise aware DSM circuit. The proposed model results in an error of less than 10% when compared to that of the SPICE simulation.

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