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MULTI-GATE MOSFET STRUCTURES WITH HIGH-K DIELECTRIC MATERIALS

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Abstract: Multi-gate MOSFETs has shown better results in subthreshold performances. The replacement of SiO_2 by high-k dielectric can fulfill the requirements of Multi-gate MOSFETS with scaling trend in device dimensions. The advancement in fabrication technology has also boosted the use of different high K dielectric materials as oxide layer at different places in MOSFET structures. One of the most important multigate structure is FinFET which shown better subthreshold swing (SS) and drain-induced barrier lowing (DIBL), which is possible with optimum ratio of gate length to Fin width. In this paper we have discussed the different FinFET structures with use of high K dielectric materials for performance improvement. Also the performance of Fin shaped GAA with gate oxide HfO_2 are simulated and compared with conventional gate oxide SiO_2 for the same structure.
Index term: Silicon-On-Insulator(SOI), SOI FinFET, Bulk FinFET, Punchthrough stopper, Short channel effect, DIBL, Subthreshold Slope, High K dielectric material

I. INTRODUCTION

The continuous scaling of semiconductor has allowed reduction in the size of device, improving the speed of operation [1] and area requirement in the VLSI circuits. Beyond 45 nm technology the short channel effects [2] deteriorate the performances of the MOSFETs, so new structures such as Bulk and SOI FinFET have been proposed by the designers and efforts being made to enhance the performance of these devices. The improvement in a device can result in terms of improvement in the area, power and speed of the VLSI circuits. A lot of research works has been done on the feasibility of other alternative high-k dielectric (e.g. Al_2O_3, ZrO_2, Ta_2O_5, HfO_2, $ZrSi_xO_y$, Y_2O_3, Ya_2O_3) for submicron MOSFET in order to reduce current leakage and increase the gate capacitance [3]. Recently binaries and ternaries of hafnium (Hf) and zirconium (Zr) have shown promising performances. Even though TiO_2 had a very high dielectric constant, due to better thermo dynamical stability with silicon, HfO_2 and ZrO_2 became most favorable among many research groups [3]. Since HfO_2 has been found to form a more stable interface than ZrO_2, HfO_2 as gate dielectric has good potential for present and future CMOS applications.

The critical requirements, that a high-*K* dielectric must fulfill before it can replace SiO_2, where considered in particular during high temperature processing and annealing [4]. The other key issues which complicates the use of high-k materials such as reduction in drain current, transconductance and mobility, are resolved by replacing polysilicon by thermally stable and low work function metal gate [5,6].

In this paper we explain the various issues regarding the replacement of SiO_2 by high-k dielectric which can fulfill the requirements in subthreshold region of multi-gate MOSFETs [7]. Thus an optimum design of FinFET structure with the use of high K materials in gate oxide results into the increase in on-state current while off-state current, subthreshold slope and DIBL decreases, enhancing the FinFET performance due to the fringing electric field [8]. The magnitude of the fringing electric field depends upon the dielectric constant of the medium in which it is getting leaked. The fringing field increases with the use of high k dielectric material. The high K dielectric material is utilized at different places in different MOS devices for performance improvement [9]. The use of spacer increases the fringing electric field in the FinFET. The fringing electric field is leakage electric field which originates from the side walls of a spacer and ends in the fin region. The use of spacer in a FinFET device results in increased on-state

current while reducing the off-state current, sub threshold slope and drain induced barrier lowering. Thus the use of spacer improves the performance of the FinFET. Further, the high k dielectric materials such as Si_3N_4, HfO_2 improve the strength of the fringing electric field resulting in increase of the on state current while the off state current, sub threshold slope and drain induced barrier lowering of the FinFET is decreased, thus resulting in improvement of the device performances. The performance of Fin shaped GAA structure [10] is also studied for different high K dielectric gate oxides [11].

II. DEVICE STRUCTURE AND DIMENSIONS

The device simulations were performed by the 3-D TCAD simulator [12]. In the first part of simulations a FinFET of Fig.1 with 20 nm channel length is used. The channel of the FinFET is lightly doped with the concentration of 1E15 cm^{-3} with doping level in source, drain region is 1E20 cm^{-3}. The gate electrode thickness used is 40 nm while the spacer width is kept at 15 nm. The fin thickness used for the FinFET is 10 nm. The Spacer materials used are silicon oxide (SiO_2), silicon nitride (Si_3N_4) and hafnium oxide (HfO_2) having dielectric constant of 3.9, 7 and 25 respectively. The threshold voltage of the device is 0.2 V.
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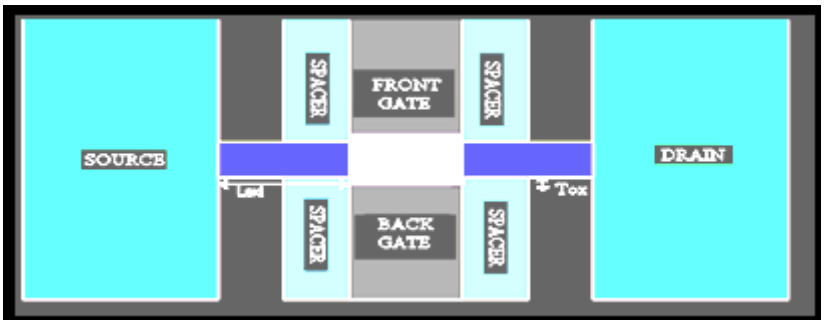

Fig.1: Actual FinFET device structure

In the second part of analysis GAA MOSFETs are designed with 3-D device simulator for different fin width and dielectric constants. Fig.2 shows the bird's eye views GAA MOSFETs used in device simulations. SOI substrate was used in both TG FinFET and GAA MOSFETs having n-type channels and the same physical parameters as follows. Basically, the tri-gate FinFET designed is of 32nm channel length with source/drain doping is 1E20 cm^{-3}(n type). Metal is used as gate contact material and the work function of metal is kept 4.6 eV. Silicon dioxide is as gate oxide material. Gate oxide thickness is kept 1.1 nm. The channel doping is 1E16 cm^{-3} (p type) with V_{DD}=1.0V.

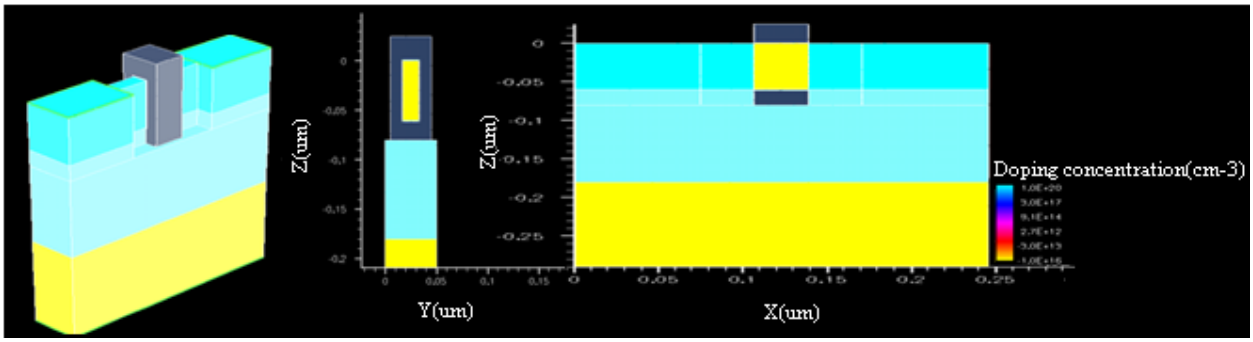

Fig.2: 3-D structure of GAA MOSFET with Y-cut of 3-D GAA structure and X-cut of 3-D GAA structure

III. SIMULATION AND RESULTS

The simulations are performed mainly for FinFET structure with high K dielectric spacers and Fin shaped GAA structure with high K dielectric gate oxide. The device dimensions are according to the International Technology Roadmap for Semiconductors (ITRS) [13].

III. 1 Use of high K dielectric material as spacer

The FinFET structures with high K dielectric material spacers, are studied by using different materials such as Silicon Oxide (SiO_2), Silicon Nitride (Si_3N_4) and Hafnium Oxide (HfO_2) having dielectric constants 3.9, 7 and 25 respectly. In these HfO_2 shows best performance(high on current) with dielectric constant of 25. The transfer characteristics for different material spacer FinFETs are shown in Fig.3

It is clear from the characteristics that there is an increase in on state current of the device with the use of high k dielectric material spacer. Simultaneously, the off-state leakage current of the FinFET decreases with the use of high k dielectric material, thus increasing the I_{on}/I_{off} ratio of the device which is very essential for low power operation of the device. The decrease in off state current is basically because of increase in the barrier potential faced by the carriers as explained earlier. Here, the on state current has doubled for Hafnium Oxide spacer FinFET if it is compared with FinFET without spacer. Thus, there is substantial improvement in the on state current of the device. Also, the off state current is lowest for Hafnium Oxide spacer FinFET device. So, in all maximum on state current and minimum off state leakage current is obtained for the Hafnium Oxide spacer FinFET device.

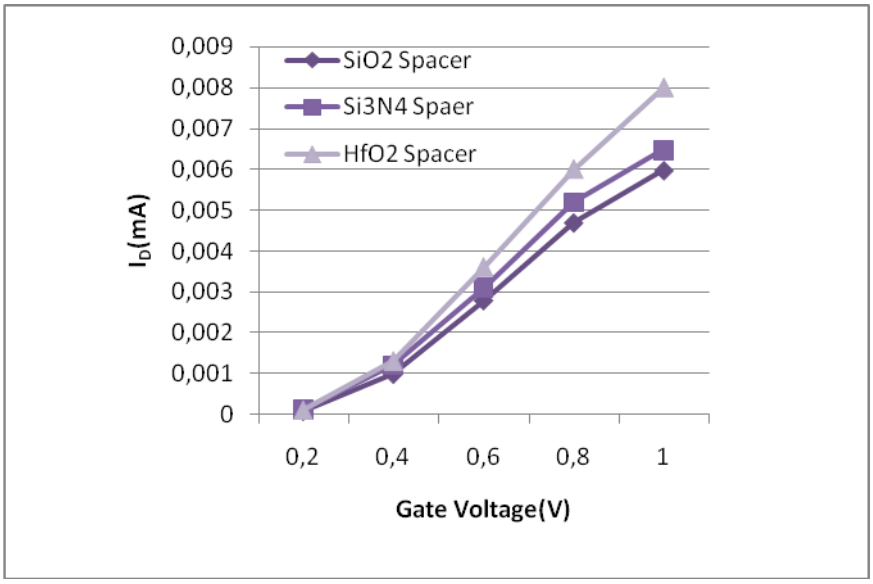

Fig.3: Transfer characteristics of the FinFET with different dielectric materials at $V_{DS}=V_{dd}$

The variation of on-state current (I_{ON}) and off state leakage current (I_{OFF}) with different dielectric materials is shown in Fig.4. Fig.5 shows that the I_{on}/I_{off} ratio increases with increasing dielectric constant. Also the use of spacer increases the overall gate capacitance of the FinFET as additional capacitance comes in parallel with the gate capacitance. The value of this capacitance increases with the use of high k dielectric material[14]. Thus, with use of high k dielectric material for spacer the overall gate capacitance of the FinFET also increases. The subthreshold slope and drain induced barrier lowering are also important parameters of the FinFET where subthreshold slope indicates how fast a device can switch from the on state to the off state or vice versa. The value of sub threshold slope should be as minimum as possible so as to have a faster switching operation and also drain induced barrier

lowering should be as minimum as possible for the better performance of the device. The variation in sub threshold slope and DIBL with different dielectrics is shown in Fig.6. The sub threshold slope as well as DIBL is minimum for Hafnium Oxide spacer FinFET while it is maximum for FinFET without spacer.

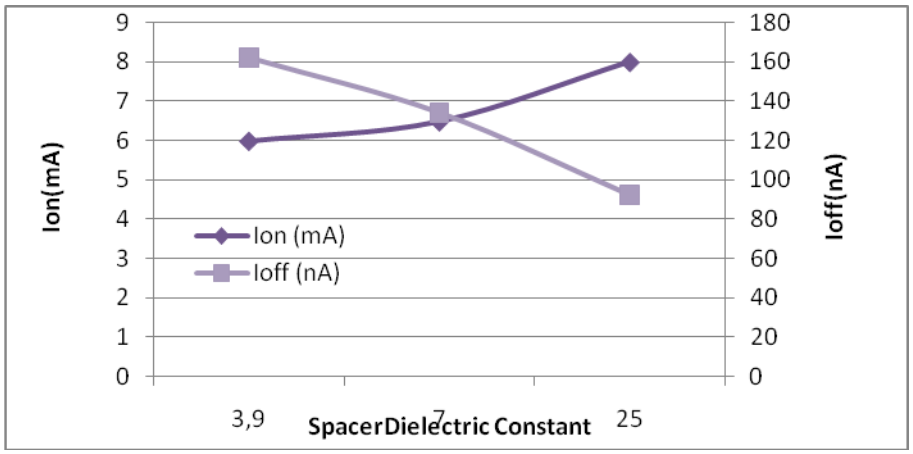

Fig.4: Variation in I_{on} and I_{off} with dielectric constant of the spacer material for FinFET

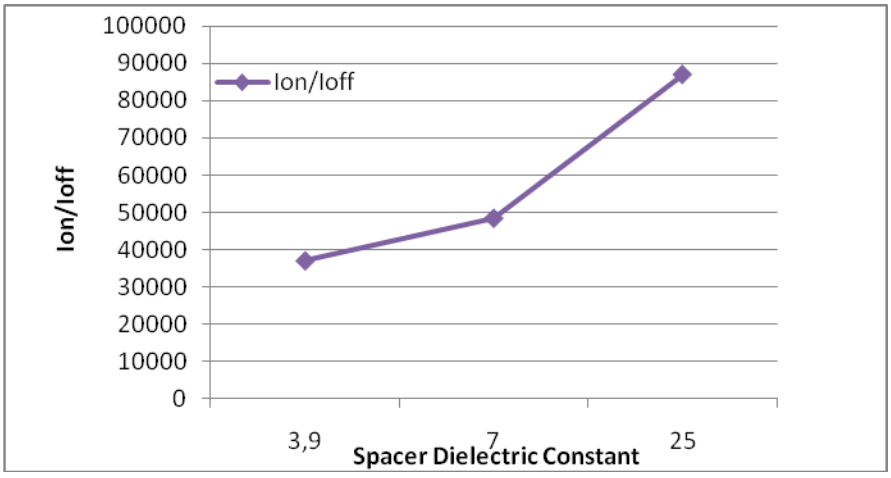

Fig.5: Variation I_{on}/I_{off} with spacer dielectric constant

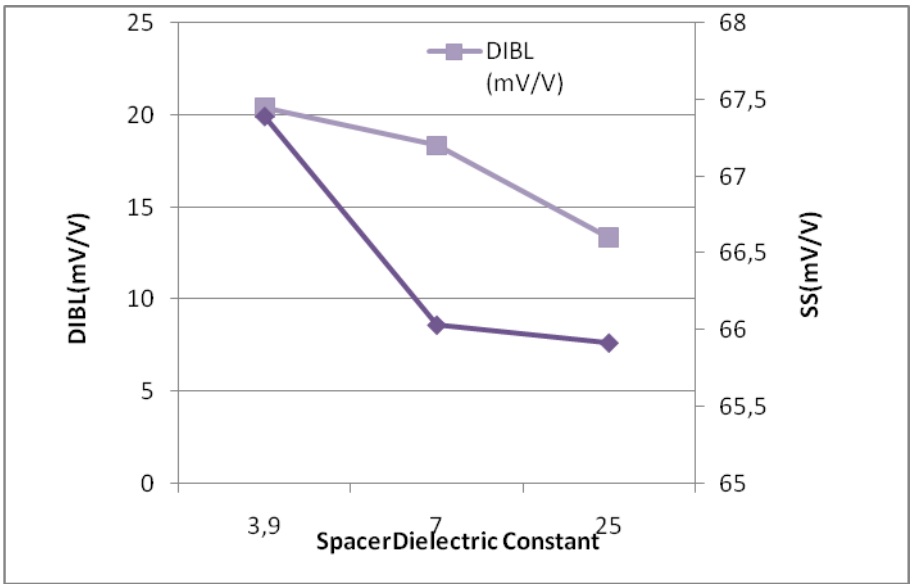

Fig.6: Variation in sub threshold slope and DIBL with spacer dielectric constant

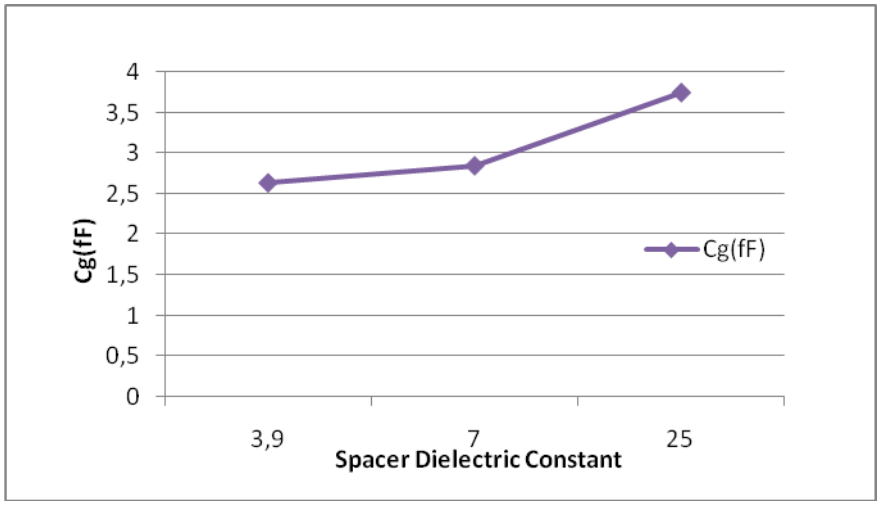

Fig.7: Gate Capacitance with spacer dielectric constant

Due to the use of high k material for spacer, the overall gate capacitance increases, that is shown in Fig.7.

III.2 Use of high K dielectric material as gate oxide

Use of high K dielectric materials for gate oxide, increases the Ion/Ioff ratio of the device which is very essential for low power operation of the device as in Fig.8. The decrease in off state current is basically because of increase in the barrier potential faced by the carriers. Use of high K material(HfO2) gate oxide is suitable to get improved subthreshold performance with high W_{fin} specially in GAA MOSFET[15]. Fig.9 shows the comparison between subthreshold characteristics of GAA structure with SiO2 and HfO2 as dielectric material for gate oxide.

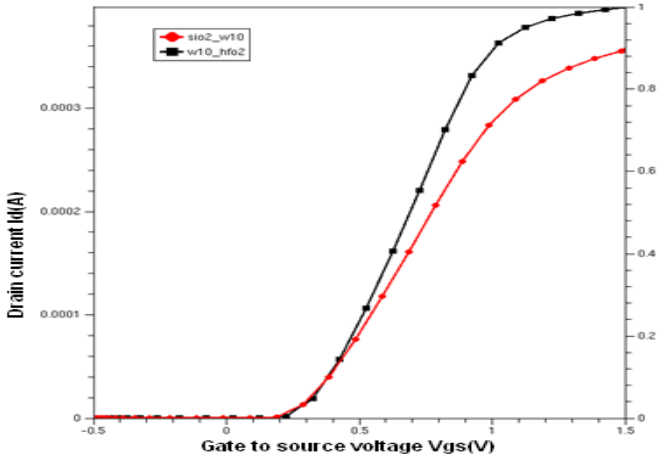

Fig.8: Transfer characteristics of GAA structure with SiO_2 and HfO_2 gate oxide material for 10nm W_{fin}

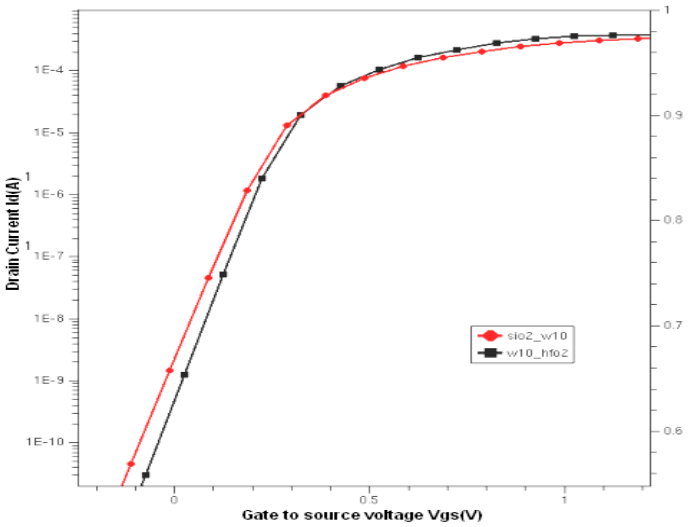

Fig.9: Subthreshold characteristics of GAA with SiO_2 and HfO_2 gate oxide for 10nm W_{fin}

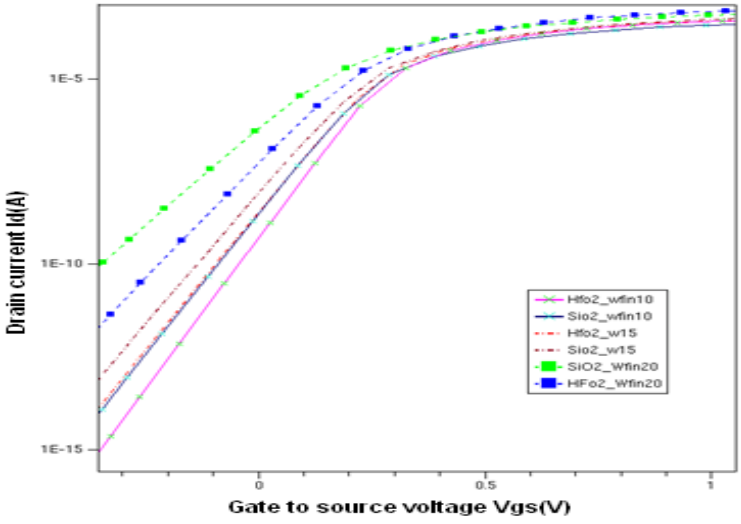

Fig.10 Subthreshold characteristics of GAA with SiO_2 and HfO_2 gate oxide for different W_{fin}

Fig.8 and Fig.9 indicate that GAA structure with HfO_2 oxide material gives improved I_{on}/I_{off} ratio with the improvement in subthreshold performance. The increase in the Ion/Ioff ratio of the device which is very essential for low power operation of the device and the value of it can be controlled by proper design of W_{fin} .

IV. CONCLUSION

The use of high k dielectric materials such as Si_3N_4, HfO_2 improves the strength of the fringing electric field resulting in increase in the on state current while the off state current, sub threshold slope and drain induced barrier lowering of the FinFET is decreased, thus resulting in improvement of the device. FinFET with high K dielectric material increases I_{on}/I_{off} ratio which increases the scope for high W_{fin}(Fig.10) . There is also scope of using multiple layers of high K dielectric materials for performance improvement in nano scale applications.

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