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DOUBLE GATE-CONTROLLED DUAL BASE SOI BIPOLAR JUNCTION TRANSISTOR: A PROMISING CANDIDATE FOR HIGH SPEED ELECTRONICS

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ABSTRACT

A silicon-on-insulator double gate-controlled dual base bipolar junction transistor (BJT) is proposed here. The device structure is same as SOI MOSFET with two body contacts. Here a novel mode of operation of this existing structure has been investigated. The device combines two lateral BJTs and features two MOS gates to control the BJT action of the device. The neutral base region in which the BJT action takes place and carrier concentration profile in the base region can be modulated by the two MOS gate biases which in turn modulate the current gain of the device. This novel transistor's multiple bases and extra functional flexibility may give rise to exciting circuit opportunities for analog, RF, mixed signal and digital applications.

Keywords*:* FD SOI MOSFET, Dual Base BJT, Multi-gate Transistors, Emitter Efficiency, Surface Recombination Rate.

I. INTRODUCTION

Bipolar Junction Transistors (BJTs) are attractive for speed, low noise performance and current driving capability while the complementary MOS transistors offer the low standby power consumption and high-packaging density. An increase in interest in the fabrication of CMOS transistors and bipolar transistors in a

monolithic structure has been observed in the past [1] in order to incorporate all these advantages in a single transistor. To obtain a pure BJT action, the MOS gate was biased in such a way that an accumulation layer is formed under the gate oxide to ensure a quasi-neutral base region. This required four terminal connections along with a negative bias on the gate. Later a three terminal hybrid mode device was fabricated using a bulk CMOS technology where the gate and well were internally connected to form the base [2]. This hybrid lateral BJT demonstrated high gain.

The Gate-controlled BJT was first proposed as two gated p-n junction diodes [3] and as surface potential controlled transistor [4]. This exhibited a MOS gate on top of the emitter-base junction to control the surface potential, minority carrier generation and recombination rate and thereby the current gain of the transistor. Lateral BJT in a regular MOSFET structure was studied to propose a gate-controlled lateral pnp (GC-LPNP) BJT, which was fabricated using 0.8 μm BiCMOS technology which exhibited a unique combination of MOS action and BJT action under the control of gate bias [5].

Silicon-on-insulator (SOI) devices are popular for high performance integrated circuits due to very low parasitic capacitance. The investigation of parasitic lateral bipolar structure with floating base [6], [7] opened a new mode of operation of SOI devices. Novel lateral bipolar SOI structures has been investigated to exploit new circuit opportunities [8], [9], [10], [11]. A short channel SOI MOSFET fabricated on a thick SOI film was explored, which lead to the proposal of Voltage-Controlled Bipolar MOS (VCBM) device [12]. The floating base (substrate) was connected to the gate which allowed the bipolar current to be added to the MOS channel current. This novel mode of operation is quite attractive for high speed operation with greater current drive.

An investigation of the parasitic BJT mode in fully depleted SOI n-MOSFET was reported in [13]. This BJT mode provides very high transconductance-to-current ratio as well as better immunity to short channel effect than the MOSFET mode. But the substrate bias was not considered. In this paper, the substrate is considered as a back-gate and the effect of both MOS gates on the base region is investigated. Moreover, in this paper the analysis is made on a fully-depleted SOI MOSFET with two independent body contacts located on either side of the body. These two body contacts act as two bases. The separation between these

two base contacts is so long that these two bases emulate a combination of two independent BJTs with same emitter and same collector. The parasitic BJT action can also be controlled with the back-gate or substrate bias along with the front-gate as previously reported in [13]. The two MOS gates are used to modulate the neutral base region and the minority carrier concentration in the base region, which in turn noticeably modulate the current gain of the transistor. Utilizing this novel mode of operation will provide new circuit opportunities for both analog and digital applications. Moreover, the two independent bases and multi-gate flexibility in a single transistor will reduce the transistor count in significant amount. The benefit of double MOS gate control on the parasitic BJT action of two independent bases can be envisioned as a double gate-controlled dual base bipolar junction transistor or $(GB)^2$-BJT.

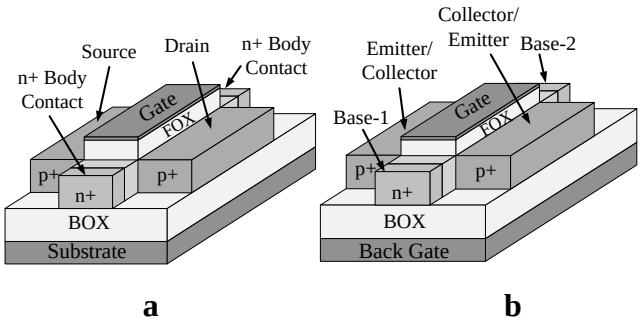

Fig. 1: Schematic view to show the equivalency between two structures
a) p-channel SOI MOSFET structure, **b)** pnp $(GB)^2$-BJT structure.

II. DEVICE STRUCTURE

The pnp $(GB)^2$-BJT is originally a p-channel SOI MOSFET with two body contacts located on either side of the body. This type of MOSFET structure with two body contacts has been successfully fabricated and envisioned as a four-gate transistor [14], [15]. In case of the device proposed here, the drain and source of the MOSFET are used as collector and emitter and the two body contacts are used as two bases for BJT mode operation (see Fig. 1). The substrate emulates a back-gate for the device. Thus no extra fabrication steps are required to manufacture the device. The base width is same as the channel length of the MOSFET. The separation between two bases (channel width) is sufficiently large that the actions of the two lateral BJTs remain independent.

The analysis was done using 3-D Silvaco/ATLAS simulation on a device with 50 nm thick buried oxide and 40 nm thick silicon film. The gate contact is p^+ polysilicon and the gate oxide thickness is 5 nm. The base width (channel length) of the device is 80 nm and the separation between two bases (channel width) is 5 μm. The doping concentration of the body is 10^{17} cm^{-3}.

III. TRANSISTOR CHARACTERISTICS

The simulation was done on a SOI p-MOSFETof 40 nm thick silicon film on 50 nm thick buried oxide. The gate material is p^+ polysilicon and the gate oxide thickness is 5 nm. The channel length(base width) and channel width (separation between two body contacts i.e. two base contacts) of the device is 80 nm and 5 μm respectively. The doping concentration of the body is 10^{17} cm^{-3}.

Different combinations of front and back surface charge conditions have been considered for analysis (Fig. 2) andinitially both bases are tied together for simplicity. For inverted front-surface (V_{G1}<-2.5V), collector current becomes a combination of MOS action near the front surface and BJT action away from the front surface. The collector current decreases as the front surface is driven to depletion(-2.5V<V_{G1}<-0.5V), because the contribution from the MOS action is negligible.For depleted surface, base resistance becomes strong function of both of the gate biases. As the base resistance increases with gate bias, the effective base to emitter voltage decreases due to ohmic drop, causing the reduction in the collector current. For accumulated front surface (V_{G1}>-0.5V), minority carriers are repelled away from the surface increasingthe concentration in the mid region of the body which altogether contribute to BJT action. This dependence on front-gate bias is true for any back surface charge condition.For accumulated back surface (V_{G2}=15V), the dependence of collector current on front-gate bias is similar to that observed for depleted back surface (V_{G2}=0V) except the collector current is slightly reduced. This is because the minority carriers are repelled from the back surface and the region in which the BJT action is now taking place is smaller than the previous. When the back surface is driven to inversion (V_{G2}=-15V), the back channel component elevates the total collector current, making this region of operation less BJT like.

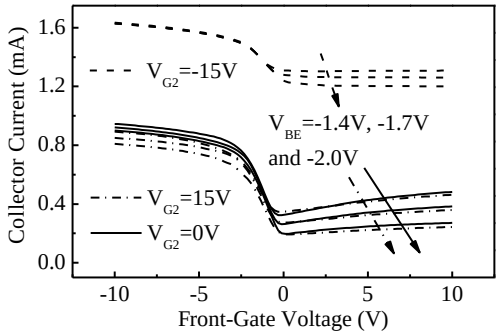

Fig. 2: Collector current as a function of front-gate bias when the back surface is accumulated (V_{G2}=15V), depleted (V_{G2}=0V) and inverted (V_{G2}=-15V). Bias condition: V_{CE}=-3V.

The operation mechanism of a BJT highly depends on the minority carrier concentration in the base region. Emitter and collector currents are given by the minority density gradients at the junction boundaries [16]. The minority carrier concentration profile in the base can be modulated by changing the MOS gate biases which in turn control the hole injection from emitter and diffusion mechanism of holes in the base region. Thus the common emitter current gain (β) and common base current gain (α) become functions of the gate biases, as shown in Fig. 3. The biasing ranges are chosen such that both surfaces remain either in accumulation or depletion, ensuring proper BJT action (MOS actions are negligible). The current gain is lowest (α ≈ 0.65, β ≈ 1.86) when both of the surfaces are in strong accumulation (V_{G1}=5V and V_{G2}=10V). α stays close to unity and β remains moderately high when both the surfaces are in depletion.

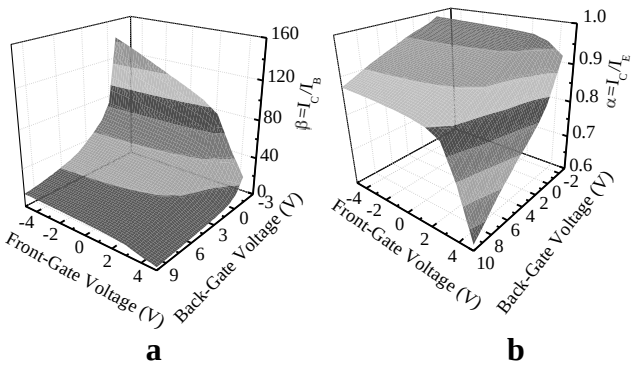

Fig. 3: a) Common emitter current gain, **b)** Common base current gain.
Bias conditions:V_{CE} = -2V and V_{BE} = -1V.

When both the surfaces are accumulated, the minority carriers are repelled away from the surfaces and gathered at the mid region in the body. An increased concentration of minority carriers significantly reduces

the hole injection from the emitter near the mid region of the base between the surfaces as shown in Fig. 4. The injection efficiency is ~100% as long as the front surface remains depleted. The neutral base region is very small compared to the diffusion length of holes. That is why the recombination rate is very low (see Fig. 5a). But when the front gate bias is increased towards accumulation, the length of this neutral region slightly increases causing recombination rate to increase and also lower emitter efficiency is observed. The back-gate bias in these analyses was kept such that the back surface remains depleted.

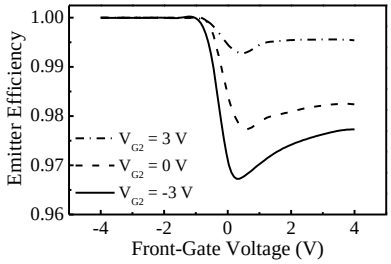

Fig. 4: Emitter efficiency. Bias Conditions: V_{CE} = -2V and V_{BE} = -1V.

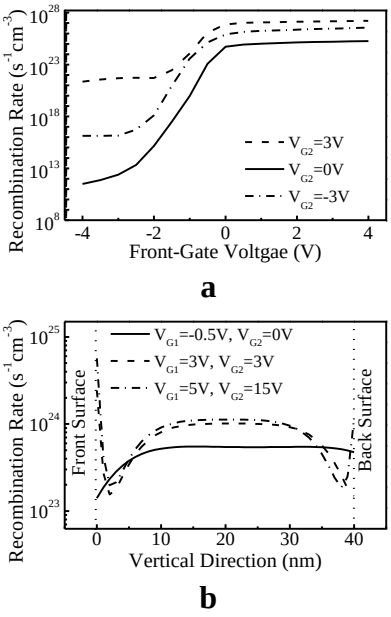

Fig. 5: Recombination rate as a function of **a)** front gate voltage for different back-gate biases and **b***)* vertical direction (from front surface to back surface), at the mid position between the two junctions. Bias Conditions: V_{CE} = -2V and V_{BE} = -1V.

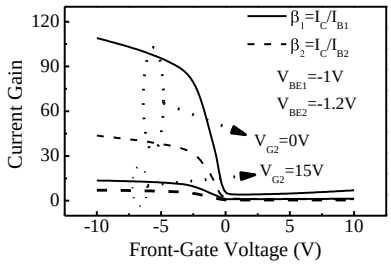

Fig. 6: Common emitter current gain considering dual base action. Bias Conditions: V_{CE} = -2V and V_{BE} = -1V.

Moreover, the holes injected near the surface areas get recombined with the accumulated majority carriers if the surfaces are in accumulation (see Fig. 4c). For both surfaces depleted (V_{G1}=-0.5V, V_{G2}=0V), the surface recombination rates are very low. When surfacesare driven to accumulation (V_{G1}=3V and 5V, V_{G2}=15V), the recombination rate becomes very high. Back surface recombination rate decreases as the back surface is made more depleted (i.e. as V_{G2} is changed from 0V to 3V). Fig. 4d describes the dual base action of the device. The gain associated with these two individual base actions depend on the amount of charge contributed through each base. The base contributing fewer carriers has greater gain. The relation between collector current (I_C) and base currents ($I_{B1,2}$) can be stated as $I_C = \beta_1(V_{G1}, V_{G2})I_{B1} + \beta_2(V_{G1}, V_{G2})I_{B2}$, where $\beta_{1,2}$ are common emitter current gains.

In order to exploit full advantage of a gated controlled BJT, the front and back surfaces must be either in depletion or accumulation. This limits the biasing range of both control-gates. Moreover, in order to operate this device in dual base mode, the gate-biases should be varied in such a range which ensures depleted surfaces only. Because an accumulation layer in any surface may induce a current component from one base to another, if they are biased with unequal voltages.

IV. CONCLUSION

The proposed device combines all the advantages offered by BJT and MOSFETs in a single transistor. Utilizing this novel mode of operation will provide new circuit opportunities for both analog and digital applications. The two independent bases and multi-gate flexibility in a single transistor will reduce the transistor count in significant amount. Moreover this device offers greater current drive.

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