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TRANSPORT CHARACTERISTICS AND SUBTHRESHOLD BEHAVIOR OF HIGH-K DIELECTRIC DOUBLE GATE MOSFETS WITH PARALLEL CONNECTED GATES

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ABSTRACT

Transport characteristics and subthreshold behavior of a structurally modified high-κ dielectric Double Gate MOSFET in which each gate was a parallel combination of three gates with different work functions were analyzed. Various scattering mechanisms were modeled through simple Büttiker probe method. The subthreshold leakage and the drain induced barrier lowering decreased and the threshold voltage increased when the screen gate workfunction was greater than the middle gate (control gate) workfunction. The improvement in the subthreshold parameters was further enhanced when high- κ materials were used as insulator layers. High workfunction parallel connected metal gates exhibited better ballisticity as energy relaxing scattering mechanisms in those devices were less because of the decrease in the critical scattering length. It was concluded that to enhance further the comparatively better subthreshold behavior exhibited by double gate MOSFETs with high- κ insulator materials, screen gates with large work function could be used.

Keywords: DG MOSFET, high- κ materials, screen gate, control gate, gate workfunction, critical scattering length.

I. INTRODUCTION

The double gate MOSFET (DG MOSFET) is one of the best device structures [1] to carry on the process of downscaling as envisaged in the ITRS road map, as it shows significantly superior short channel behavior when compared with its other competitors in miniaturization [2]. Many theoretical and experimental endeavours to further improve the short channel behavior of double gate MOSFETs have been reported recently [3]-[8]. In a previous work, D. Datta et al. proposed a novel DG MOSFET structure [9] in which parallel connected hetero-material double-gates were employed. They reported that such parallel connected hetero-material double-gate (PCHEM-DG) MOSFETs showed a reduction in the leakage components compared to bulk MOSFETs.

Double Gate MOSFETs with high-κ dielectric materials have shown better subthreshold performance compared to their SiO_2 counterparts. However, such high-κ devices show poor ballisticity, because of the dominance of energy relaxing phonon scattering. In our work, it was found that a double gate structure, that combined parallel connected gate contacts of different workfunctions and high-κ dielectric materials, possessed superior subthreshold behavior and ballisticity. The aim of this paper is to present using two-dimensional simulation, the reduced short channel effects and better ballisticity exhibited by such a device structure while simultaneously achieving a higher on current and better on-off ratio compared to the 'conventional' DG MOSFET.

II. DEVICE STRUCTURE OF DG MOSFETS WITH HIGH κ GATE DIELECTRICS AND PARALLEL CONNECTED GATE CONTACTS OF DIFFERENT WORK FUNCTIONS

The structure of the device under study is that of a double gate MOSFET with heavily n-doped ($N_D=10^{20}$ cm^{-3}) source and drain regions. Si is the channel

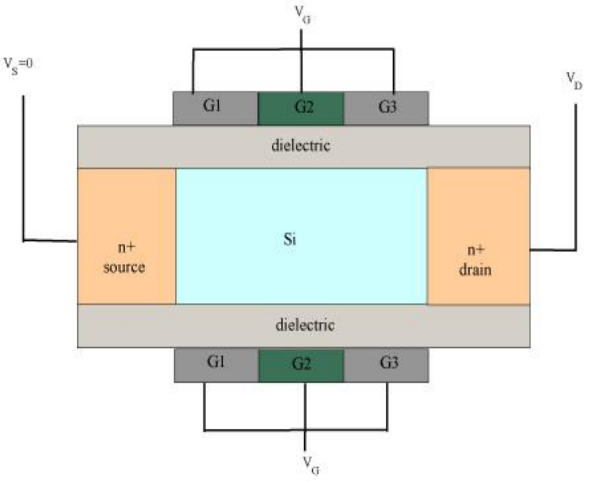

Figure 1: A Double Gate MOSFET with parallel connected metal contacts of different workfunctions forming the bottom and top gates.

material. The top and bottom gates of the MOSFET consist of three laterally contacting metals of different work functions as shown in figure 1. The pairs of top and bottom gates G_1 and G_3 closer to the source and drain extension regions are called screen gates, which are shorter in extension when compared with the middle gate G_2, called the control gate. The parallel combination of the gates $G_1G_2G_3$ forms the top and bottom gates. Unlike in an ordinary DG MOSFET, the effective gate voltage is controlled by the work-function differences of different metals used in the gate, thereby introducing variation of electrostatic potential in the active device region.

All the device structures that we analyzed in this work had channel length of 10 nm and channel thickness of 3nm. Different gate dielectric materials–SiO_2, Si_3N_4, $HfSiO_4$, Y_2O_3 and Ta_2O_5–were used in different structures and metals Ta, TaSiN and Al were used to form gate combinations such as Ta-Al-Ta, TaSiN-Al-TaSiN, Al-Al-Al etc. These metals were selected as they give the desired on and off currents when used as gate contact materials in DG MOSFETs in the 10 nm regime. Each screen gate had an extension of 2nm and the control gate had a length of 6nm in all cases. The source and drain extension regions were 3nm in extension and the physical thickness of the insulator layer was kept at 1nm to minimise the gate leakage current.

III. MODELING SCHEME OF THE DG MOSFET WITH PARALLEL CONNECTED GATE CONTACTS

The non-equilibrium nature of electron transport from source to drain is well represented by the non equilibrium Green's function formalism. For a given sub band m, the 1D electron density can be obtained from the diagonal elements of

$$n^m(x) = \frac{1}{\hbar a}\sqrt{\frac{m_z^* k_B T}{2\pi^3}} \int_0^\infty \left[\Im_{-\frac{1}{2}}(\mu_S - E_l) A_S^m + \Im_{-\frac{1}{2}}(\mu_D - E_l) A_D^m \right] \quad (1)$$

where $\mu_{S/D}$ are the electrochemical potentials of source/drain contacts, a is the length of one finite difference mesh along the propagation direction, $\Im_{-\frac{1}{2}}$ is Fermi integral of order -1/2 and $A_{S/D}^m$ is the spectral function relevant to the source/drain contacts. The 2D electron density for each sub band is obtained by multiplying the 1D density with the corresponding distribution function $\left|\zeta^m(y,x)\right|^2$ at each longitudinal lattice node, and the total 2D electron density is calculated by summing the contributions from all sub bands.

$$n(x,y) = \sum_m n^m(x,y) = \sum_m n^m(x)\left|\zeta^m(y,x)\right|^2 \quad (2)$$

In a self consistent simulation scheme, the electron density obtained in (2) is substituted into the 2D Poisson equation

$$-\frac{\partial}{\partial x}\left(\varepsilon_r \frac{\partial U}{\partial x}\right) - \frac{\partial}{\partial y}\left(\varepsilon_r \frac{\partial U}{\partial y}\right) = -\frac{q}{\varepsilon_0}(N_D - n) \quad (3)$$

to obtain the electrostatic solution. In (3) U is the electrostatic potential, N_D is the donor concentration, and n is the free carrier electron concentration. The above equation can be solved to obtain the potential energy, after imposing suitable boundary conditions at all contact electrodes. The Dirichlet boundary conditions at the gate electrodes are calculated from the gate bias and the band bending.

$$U_{G_j} = -V_{G_j} + \Phi_{M_j} - \Psi_{Si} \quad (4)$$

where V_{G_j} is the gate bias at the gate G_j, Φ_{M_j} is the work function of the metal forming the gate G_j, and

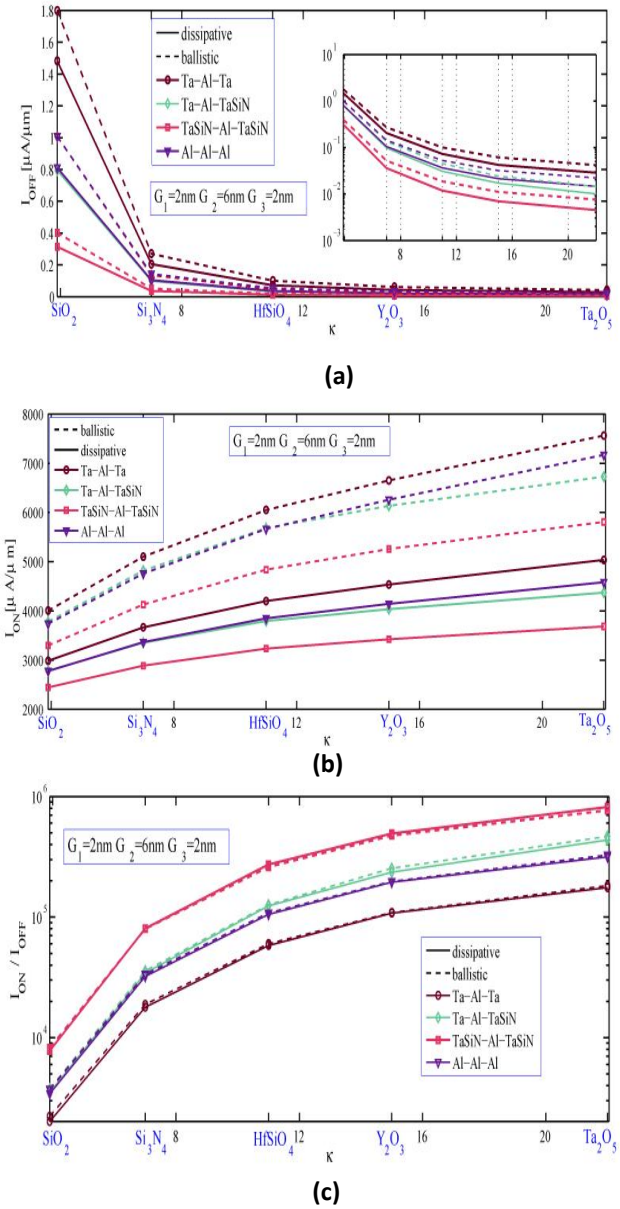

Figure 2: Plot of (a) on-current I_{ON} (b) off-current I_{OFF} and (c) on-off ratio I_{ON}/I_{OFF} (logarithmic scale) versus κ .

Ψ_{Si} is the electron affinity in the silicon channel. At the source/drain contacts, Neumann boundary conditions are applied. The coupled set of NEGF equations and Poisson equation could be solved in a self-consistent loop to obtain the charge density and electric potential in the active region.

IV. SCATTERING IN HIGH κ DG MOSFETS WITH PARALLEL CONNECTED GATES

Experimental data [10], [11] show that the on-current in a nanoscale device increases with decreasing dimensions initially, however decreasing the dimensions further reverses the trend and reduces current density. This behavior has been attributed to electron-phonon scattering and interface roughness scattering [12]. In our work Büttiker probes, a phenomenological treatment of scattering based on a simple approximation that individual scattering centers couple to the device in a manner identical to the S/D reservoirs [13], were used to simulate the cumulative effects of scattering due to all possible mechanisms as implemented in the popular 2D simulator nanoMOS [14].

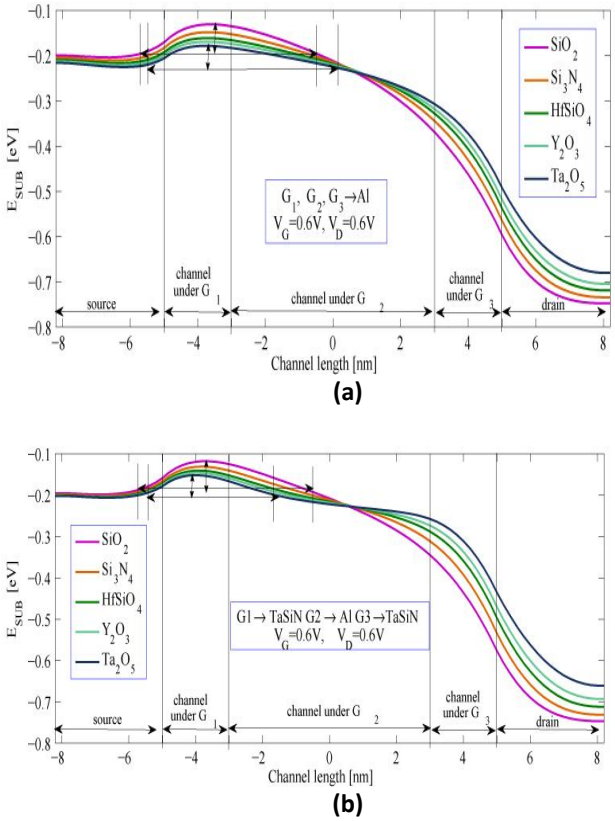

Figure 3: Potential profile along the middle of the Si channel with different high-κ dielectric layers for a device (a) with Al and (b) with TaSiN-Al-TaSiN gates.

V. RESULTS AND DISCUSSION

A finite difference mesh of grid spacing 0.1nm both in the x and y directions was used for the discretization of the Hamiltonian and the Poisson equation. The bulk values of silicon effective mass were used in the calculations. Both the top and the bottom gates were biased at the same potential from 0 to 600mV. The source electrode was grounded while the drain electrode was biased from 0 to 600mV.

Figure 2(a) is the plot of the off-current I_{OFF} (which is the drain current at $V_G = 0$ and $V_D = V_{DD}$) in linear scale, for different insulator layers and gate combinations. The inset of figure 2(a) shows the same quantities in logarithmic scale for presenting the variation of the current at lower magnitudes more clearly. It shows an almost exponential decrease in I_{OFF} with the increase in κ. For a given κ, the off-current depends on the screen gate metal, being

smaller for larger workfunctions.

Figure 2(b) shows the variation of on-current I_{ON} (the drain current at $V_G = V_{DD}$ and $V_D = V_{DD}$) for different insulator layers and gate combinations. I_{ON} increases almost linearly with κ for a given screen gate metal. The on current decreases for high workfunction screen gates because of the increase in the height of the potential barrier at the source, but this reduction is not appreciable as most of the channel is under the control gate and the high workfunction screen gates were very much shorter in extesion than the control gate.

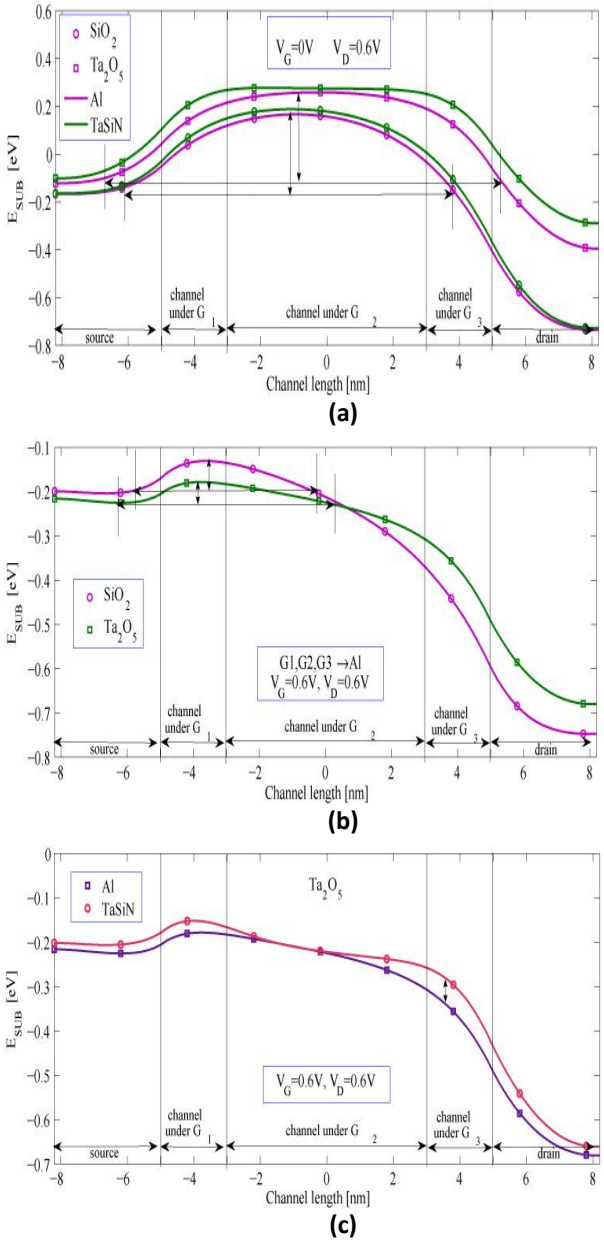

Figure 4: Potential profile along the middle of the Si channel with different dielectric layers for (a) Al and TaSiN-Al-TaSiN gates at V_G=0 and V_D=600 mV (b) Ta_2O_5 and SiO_2 layers with Al gates at V_G=600 mV and (c) Al and TaSiN screen gates at V_G=600 mV.

Substantial increase of I_{ON}/I_{OFF} is evident from figure 2(c) as κ increases, for all gate combinations. For a given κ, I_{ON}/I_{OFF} increases with the workfunction of the screen gates. The increase in on-current and the reduction in off-current for high-κ devices and high workfunction screen gates could be explained by analyzing the potential profile along the channel at different gate voltages and drain voltages. The transmission and hence the drain current is determined by the height and width of the potential barrier at any V_G and V_D. Figure 3 shows the potential profile of the device for different gate combinations and κ. Figure 3(a) is the potential along the channel for screen metal Al at a gate voltage $V_G = 0.6V$ and drain voltage $V_D = 0.6V$ for different insulator layers. As κ

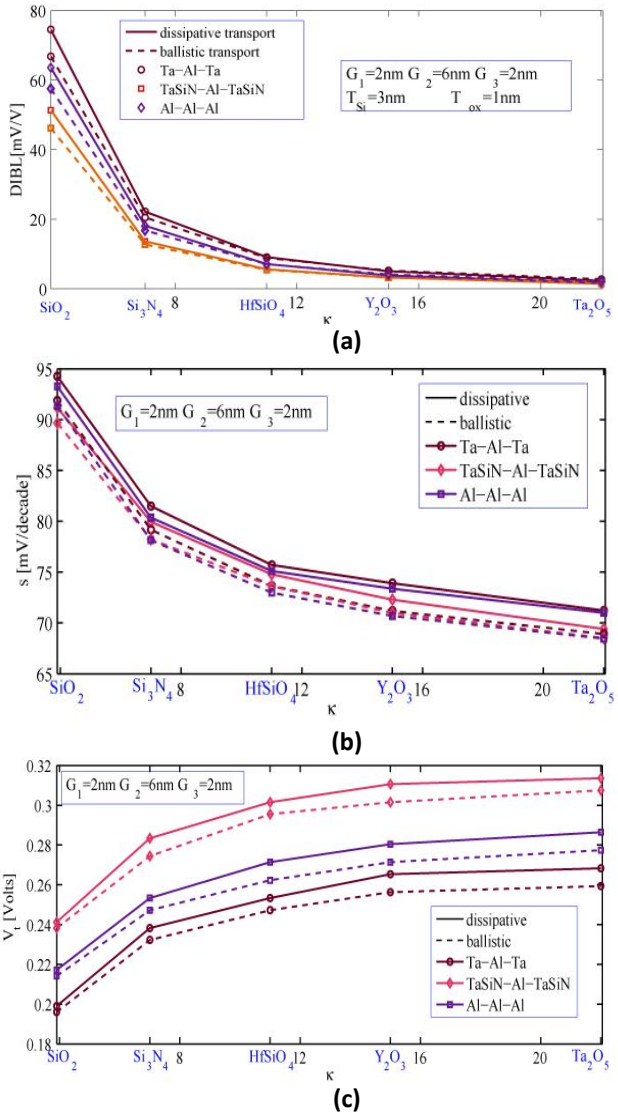

Figure 5: Plot of subthreshold parameters against dielectric constant. (a) DIBL (b) subthreshold swing S and (c) threshold voltage for different parallel connected gate materials.

increases, the width of the barrier increases slightly, decreasing the on-current. But at the same time, the height of the barrier decreases, contributing to the on-current. For instance, in figure 4(b) where we have redrawn the potential profile of Ta_2O_5 and SiO_2 for better analysis, the potential barrier for Ta_2O_5 starts near the source-channel junction and extends all the way to the middle of the channel. The width of this barrier is larger than that of SiO_2. But the barrier height of Ta_2O_5 is smaller than that of SiO_2. The net effect is a slight increase in on-current with κ for all gate combinations, a fact shown quantitatively in figure 2(b). Comparing the potential barriers of a given insulator for different gate combinations, we observe

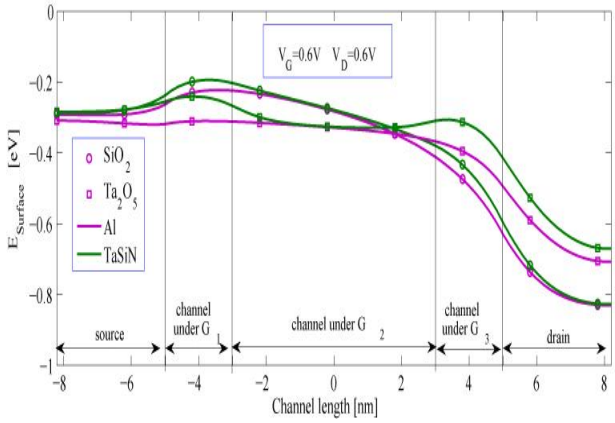

Figure 6: The surface potential along the channel of an Al gate device and a TaSiN-Al-TaSiN device for SiO2 layer and Ta_2O_5 layer.

that the on-current must increase with an increase in screen gate workfunction. It indeed is the case as is evident from figure 2(b).

The off-current depends on the shape of the barrier at $V_G = 0$. In figure 4 we have plotted the potential profile of Ta_2O_5 and SiO_2 for two gate combinations TaSiN-Al-TaSiN and single gate Al at (a) $V_G = 0V$ and (b) $V_G = 0.6V$. It is clear from figure 4(a) that the height and width of the potential barrier increases as κ increases for all gate combinations, reducing the off-current. Figure 2(a) is a quantitative demonstration of this fact. It must be noted that the dielectric constant of the insulator layer is the most crucial parameter determining the on-current and off-current. The workfunction of the screen gate can however modify the on-current and off-current appreciably.

The deviation of the transistor from ballistic transport can be expressed in terms of the decrease in drain current due to various scattering mechanisms from its value in the ballistic limit. It has been shown that only a short low field region near the source end of the channel controls the steady state on-current of MOSFETs [15]. Carriers diffuse across this low field region and they are collected by the high-field portion of the channel near the drain. The length of this current-limiting region at the beginning of the channel can be termed as the critical scattering length ℓ, which is the distance from the top of the potential barrier to the point where potential drops by $\alpha(k_BT/q)$, where α is a numerical factor greater than 1.

Table 1 shows the decrease in the drain currents from their ballistic values along with the critical scattering lengths ℓ, for devices of different screen gates and insulator layers. ℓ was calculated from the potential profiles shown in figure 4, with $\alpha = 3$. The critical scattering length increases with κ, and hence the drain current decreases from the ballistic limit, as obvious from table 1. However for a given insulator layer, the critical scattering length is smaller for a higher workfunction screen gate and the reduction in drain current is less for such higher workfunction screen gates. Thus it is clear that to obtain simultaneously better ballisticity and subthreshold behavior, the combination of high-workfunction screen gates and insulator layers with suitably high- κ is desired.

Table 1: Critical scattering length *l(nm)* and the reduction in drain current $\delta I_D(\mu A/\mu m)$ from the ballistic value for different screen gate metals and insulator layers.

	SiO_2	Si_3N_4	$HfSiO_4$	Y_2O_3	Ta_2O_5	
ℓ	3.39	3.65	4.12	4.36	4.82	
δI_D	851	1240	1604	1835	2125	TaSiN
ℓ	3.49	3.99	4.64	4.95	5.34	
δI_D	962	1391	1815	2115	2586	Al

In figure 5(a) we have plotted the variation of DIBL with change in κ of the insulator, for different gate combinations. For all gate combinations, DIBL decreases rapidly and asymptotically approaches zero as κ is increased. For any particular insulator material, the DIBL decreases with the increase in screen gate workfunction. This suppression of DIBL in high workfunction screen gates is attributed to the perceivable step in the surface potential profile under the screen gate G_3, which screens the drain potential as in dual gate MOSFETs [16]. The potential profile along the middle of the channel and the surface potential along the channel for devices with different gate combinations and insulator layers at a drain bias

of $600mV$ are shown in figure 4(c) and figure 6 respectively. It is clear that under G_3 near the drain the surface potential and the potential along the middle get lifted up for high workfunction screen gates. For the high κ material this lifting up is even more significant. So devices with high κ insulator and high workfunction screen gate exhibit only extremely small DIBL.

Figure 5(b) shows the variation of subthreshold swing s with κ. It is clear that s decreases with κ first, and then flattens out at high values of κ for all gate combinations. For a given κ, s is almost the same for all screen gates. Thus, a high-κ device has low s, making transistor switching more efficient. Figure 5(c) shows the plot of threshold voltage V_T against κ for different gate combinations. It is clear that V_T increases with κ first, and then saturates at high values of κ for all gate combinations. However for a given κ, high workfunction screen gates can significantly increase V_T. It is evident from figure 5(c) that a suitable combination of screen gate metal and insulator provides the possibility of fixing the threshold voltage of the transistors at any value during fabrication process.

VI. CONCLUSION

We implemented a numerical model for a structurally modified DG MOSFET the gates of which consisted of three laterally contacting metals of different work functions. The device performance with various insulator layers was analysed for a variety of gate metal combinations. It was found that high-κ oxide layer improved device performance as in ordinary DG MOSFETs. Gate combinations of different workfunctions could improve it further and even provided the opportunity of setting the threshold voltage of the device to the desired value at the fabrication phase by suitably choosing the workfunctions of the screen and control gates. The critical scattering length, which determines the drain current, was less in high workfunction screen gates making such devices more ballistic than the those with homogeneous gates. A prudent choice of screen gates and insulator layer can improve the subthreshold behavior of the device without sacrificing the ballisticity much. Thus, a double gate MOSFET with parallel connected gates of different workfunctions and high-κ oxide layer turned out to be having more potential for downscaling than a homogeneous gated high-κ transistor.

References

[1] T. Ernst, S. Cristoloveanu, G. Ghibaudo, T. Ouisse, S. Horiguchi, Y. Ono, Y. Takahashi, K. Murase "Ultimately Thin Double-Gate SOI MOSFETs", IEEE Trans. Electron Devices **50**, 830–838 (2003).

[2]M. Ieong, H.S.P. Wong, E. Nowak, J. Kedzierski, E.C. Jones "High performance double-gate device technology challenges and opportunities", Procedings of International Symposium on Quality Electronic Design, San Jose, CA, USA, 21 March 2002 pp 492-495.

[3]T. Ohtou, N. Sugii, T. Hiramoto "Impact of parameter variations and random dopant fluctuations on short-channel fully depleted SOI MOSFETs with extremely thin BOX", IEEE Electron. Device Lett. **28**, 740–742 (2007).

[4]S. Govindarajan, T.S. Boscke, P. Sivasubramani, P.D. Kirsch, B.H. Lee, H.H. Tseng, R. Jammy, U. Schroder, S. Ramanathan, B.E. Gnade "Higher permittivity rare earth doped HfO_2 for sub-45 nm metal-insulator-semi conductor devices", Appl. Phys. Lett. **91**, doi: 062906 (2007).

[5]J. Liu, H.C. Wen, J.P. Lu, D.L. Kwong "Dual-work-function metal gates by full silicidation of poly-Si with Co-Ni bi-Layers", IEEE Electron. Device Lett. **26**, 228–230 (2005).

[6]C.H. Lu, G.M.T. Wong, M.D. Deal, W. Tsai, P. Majhi, C.O. Chui, M.R. Visokay, J.J Chambers, L. Colombo, B.M Clemens, Y. Nishi "Characteristics and mechanism of tunable work function gate electrodes using a bilayer metal structure on SiO_2 and HfO_2", IEEE Electron. Device Lett. **26**, 445–447 (2005).

[7]A. Misra, M. Waikar, A. Gour, H. Kalita, M. Khare, M. Aslam, A. Kottantharayil "Work function tuning and improved gate dielectric reliability with multilayer graphene as a gate electrode for metal oxide semiconductor field effect device applications", Appl. Phys. Lett. **100**, doi: 233506 (2012).

[8]J. Yuan, J.C.S. Woo "A novel split-gate MOSFET design realized by a fully silicided gate process for the improvement of transconductance and output resistance", IEEE Electron. Device Lett. **26**, 829–831 (2005).

[9]D. Datta, S. Ganguly, S. Dasgupta, A.A.P. Sarab "Novel nanoscale device architecture to reduce leakage currents in logic circuits: a quantum-mechanical study", Semicond. Sci. Technol. **21**, 397–408 (2006).

[10]S.D. Suk, M. Li, Y.Y. Yeoh, K.H. Yeo, K.H. Cho, I.K. Ku, H. Cho, W.J. Jang, D.W. Kim, D. Park, W.S. Lee "Investigation of nanowire size dependency on TSNWFET", IEDM Tech. Dig., IEEE International Electron Devices Meeting, Washington DC, USA, 10-12 Dec. 2007, pp 891-894.

[11]C. Riddet, A.R. Brown, C. Alexander, J.R. Watling, S. Roy, A. Asenov "Impact of quantum confinement scattering on the magnitude of current fluctuations in double gate MOSFETs", Silicon Nanoelectronics Workshop Kyoto, Japan (12-13 June 2005).

[12]R. Kotlyar, B. Obradovic, P. Matagne, M. Stettler, M.D. Giles "Assessment of room-temperature phonon-limited mobility in gated silicon nanowires", Appl. Phys. Lett. **84**, 5270–5272 (2004).

[13]M. Büttiker "Four terminal phase coherent conductance", Phys. Rev. Lett. **57**, 1761–1764 (1986).

[14]Z. Ren, R. Venugopal, S. Goasguen, S. Datta, M.S. Lundstrom "nanoMOS 2.5: A Two Dimensional Simulator for Quantum Transport in Double Gate MOSFETs", IEEE Trans. Electron Devices **50**, 1914–1925 (2003).

[15]M.S. Lundstrom "Elementary Scattering Theory of the Si MOSFET", IEEE Electron. Device Lett. **18**, 361–363 (1997).

[16]G.V. Reddy, M.J. Kumar "A New Dual-Material Double-Gate (DMDG) Nanoscale SOI MOSFET–Two-dimensional Analytical Modeling and Simulation", IEEE Trans. Nanotechnology **4**, 260–268 (2005)