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Characteristics Variation of CMOS Inverter with RLC Global VLSI Interconnect Under the Influence of Skin Effect

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ABSTRACT

As the technology scales down to nanometer regime and the frequency of operation has gained the GHz range, the characterization of delay and noise is the center of attraction for researchers. As the technology has attained high frequency range various high frequency effects i.e. Skin effect, Proximity Effect, Electron migration theory etc. have become prominent to consider while modeling the circuit. In DSM technology Interconnect are the back bone of any system. The on-chip interconnect are now the most emergent field where the rest of the scaling down mechanism is applied. In previous research high frequency effect i.e. Skin Effect has been modeled on interconnect and verified by results. But this modeling is inefficient till the complete circuit is analyzed under this effect. This paper strives to make an impact upon the characteristics variations of a CMOS inverter when a RLC VLSI interconnect is connected at its load to drive and then evolutions of delay, noise and total harmonic distortion (THD) are analyzed.

Keywords: Electron Migration**,** On-Chip Interconnect, Total Harmonic Distortion (THD) , Delay, Noise , Proximity Effect, VLSI.

I. INTRODUCTION

As the present day technology is shrinking towards nanometer regime, interconnect delay and noise are more dominant to be considered. When it comes to verify the system integrity, only interconnect delay and noise modeling is not just sufficient. Hence the calculation of interconnect delay and noise with a complete system is more crucial and plays a major role for both performance and physical design optimization for high speed CMOS integrated circuits. Several approaches have been proposed to find the interconnect delay of the linear circuits. Almost in every research skin effect has been neglected. But as the frequency has attained a range of GHz it has become important to consider high frequency effects i.e. Skin Effect.

As the die size of CMOS integrated circuits continue to decrease, interconnections have become increasingly significant [1]. With a linear increase in length, interconnect delay increases quadratically due to the linear increase in both interconnect resistance and capacitance [2]. Large interconnect loads not only affects the performance but also cause excessive power dissipation. A large load degrades the shape of output waveform; dissipates excessive short circuit power in the following stages loading a CMOS logic gate. Several methods have been introduced to reduce interconnect delay so that these impedances don't dominate the delay in the critical path [2-7]. Furthermore, with the introduction of portable computers, power has become an important factor in the circuit design process. Thus, power consumption must be accurately estimated for improving circuit speed when driving long interconnections. Therefore, circuit level models describing both dynamic power and, recently, short-circuit power have become increasingly important [8-11].

In this paper, an analytical expression for the transient response, noise and total harmonic distortion of a CMOS inverter driving a lumped RLC load is presented. This approach is different from [12-13], where a lumped lossless capacitive load is considered. The proposed method is the extension of [15] where a lumped RC load is considered. Furthermore, Sakurai's alpha power law [14] is used to describe the circuit

operation of the CMOS transistors rather than the classical Shichman-Hodges model [16]. The alpha power law model considers short channel behavior, permitting increased accuracy and generality in the delay and power expressions. These expressions are used to estimate the propagation delay and rise and fall times (or transition time) of a CMOS inverter. Since the output waveform is accurately calculated, the short-circuit power [17, 18] dissipated by the following stage can also be estimated. Furthermore, due to its simplicity, these expressions permit linear programming techniques to be used when optimizing the placement of buffers for both speed and power. Delay and power expressions for on-chip RC interconnect have been proposed in [19]. In [20], the authors have proposed a delay and power formula using 4model. But the model is computationally complex. A number of delay models [21-23], and power models [24] have been proposed for RC interconnect. But with the increase in the frequency of operation and the wire sizes, the inductance play an important role in determining the performance of on-chip interconnects. In order to overcome these problems, this paper models the on-chip interconnect as distributed RLC segments.

This paper is organized as follows: Section 2 describes the High Frequency Effect i.e. Skin Effect. Section 3 presents the results and characteristics variation of a CMOS inverter under the influence of skin effect. Section 4 describes the conclusions.

II. SKIN EFFECT

The "Skin Effect" is the tendency of high frequency current to concentrate near the outer edge, or surface, of a conductor, instead of flowing uniformly over the entire cross sectional area of the conductor. The higher the frequency, the greater the tendency for this effect to occur. There are three possible reasons we might care about skin effect:-

(1)The resistance of a conductor is inversely proportional to the cross sectional area of the conductor. If the cross sectional area decreases, the resistance goes up. The skin effect causes the *effective* cross sectional area to decrease. Therefore, the skin effect causes the effective resistance of the conductor to increase.

(2) The skin effect is a function of frequency. Therefore, the skin effect causes the resistance of a conductor to become a function of frequency (instead of being constant for all frequencies.) This, in turn, impacts the impedance of the conductor.

(3) If the skin effect causes the effective cross sectional area of a trace to decrease and its resistance to increase[26].

Fig.(1) clearly defines how at high frequencies the skin effect can be visualized in a simple conducting wire. This figure is self capable of explaining how the resistance due to skin effect increases in the presence of skin effect.

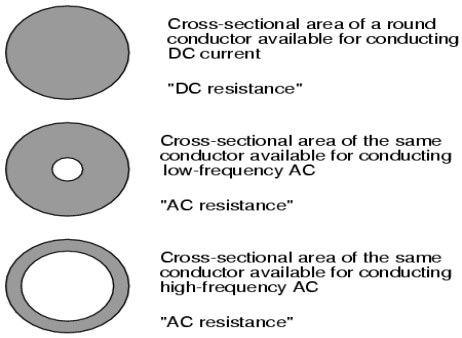

Figure 1: Skin effect on Resistance

When the skin effect is considered, thinking tends towards the current flowing only at the outer surface. This is not really true. The issue really is current density. Normal currents have a current density that is uniform and equal everywhere over the cross sectional area. But currents impacted by the skin effect have a current density is highest at the surface of the conductor and then decays exponentially between the surface and the center of the conductor. If current density is represented by J, then:

J = constant (1)

for uniform current density

$$J = J_0.e^{(-)\frac{d}{\delta}} \quad (2)$$

for skin effect currents.

In Equation 2:

J_0	Current density at the surface of the conductor
e	Base of the natural logarithm .
d	distance measured from the surface toward the Center of the conductor
δ	Skin depth.

Figure 1 illustrates the two cases of uniform current density, and current density impacted by the skin effect.

II.1. Skin Effect on Resistance

$$R_{total} = R_{DC} + \sqrt{f}\,R_{AC}, \tag{3}$$

$$\text{Where, } R_{DC} = \frac{\rho L}{W.t} \tag{4}$$

$$R_{AC} = \frac{\rho L}{A_{current\_densityar\_area}} = \frac{L\rho}{\omega\sqrt{\frac{2}{\omega\sigma\mu}}} = \frac{L\sqrt{\rho}}{\omega\sqrt{2}}\sqrt{\mu f} \tag{5}$$

Therefore,

$$R = R_{total} = \frac{\rho L}{Wt} + \frac{L\sqrt{\rho}}{\omega\sqrt{2}}.\sqrt{\mu f} \tag{6}$$

II.2. Skin effect on inductance

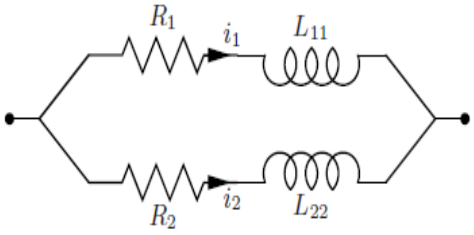

Figure 2: A circuit model with two different current paths with different Inductive properties

Consider a simple case with two current paths with different inductive properties. The impedance characteristics are represented by the circuit diagram shown in the figure (2). The inductive coupling between the two paths is neglected for simplicity. Assume that L1 < L2 and R1 > R2.The inductive time constant is given by the ratio of [27]

$$\tau = \frac{L}{R} \tag{7}$$

As it has already explained in the section that the resistance increases with the square root of the frequency hence it can be observed from the above equation that the inductance will decrease with a factor of square root of frequency [28].

III. SKIN EFFECT ON CMOS CHARACTERISTICS

An analytical model of CMOS driving RLC load is shown in the figure.

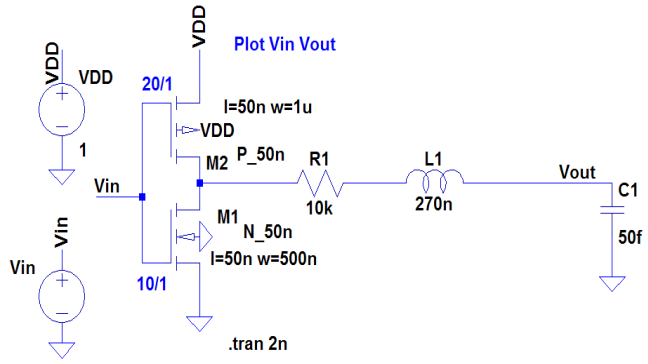

Figure 3: CMOS Driving RLC load

The alpha power law is used to describe the characteristics variation of CMOS inverter when it is operating at higher speed and the measurements are made under the influence of Skin Effect. The linear region form of alpha-power model is used to characterize the I-V behavior of the ON transistor, since a large portion of the circuit operation occurs withitn this region under the assumption of a step or a fast ramp input signal. When the input to the inverter is a unit step or a fast ramp, Vout is initially larger than (VGS-VT) for a short period of time than for the case of a slow ramp. Therefore, the circuit operates in linear region for a greater portion of the total transition time for a large RLC interconnect load. When the load resistance is large, a large IR voltage drop occurs across the load resistor once the capacitor begins to discharge, thus VDS is nearly immediately less than (VGS-VT). The N-channel device operates in the linear region once the step input goes high. However, if the input waveform increases more slowly or the load impedance is small, the inverter operates in saturation region for longer time period before switching to the linear region. Only the falling output (rising input) waveform has been considered in this paper. The following analysis, however, is equally applicable to a rising output (falling input) waveform. The lumped load is modelled as a resistor in series with an inductor and a capacitor. The current through the output load capacitance is of same magnitude and of opposite polarity to that of the N-channel drain current (the P-channel current is ignored under the assumption of the step or fast ramp input)[21]. The capacitive current is,

$$i_c = C\frac{dV_{out}}{dt} = -i_d \tag{8}$$

$$-C\frac{dV_{out}}{dt} = \frac{I_{d0}}{V_{d0}}\left(\frac{V_{GS}-V_T}{V_{DD}-V_T}\right)^{\alpha} V_{DC} \tag{9}$$

where,

$$V_{GS} \geq V_T$$

$$V_{DS} \leq V_{GS} - V_T$$

$$-CsV_{out}(s) + CV_c(0) = \psi_{d0}V_{out}(s) + \psi_{d0}R\sqrt{f}\,I_c(s) + \psi_{d0}\frac{L_s}{\sqrt{f}}I_c(s) \tag{10}$$

where

$$\psi_{d0} = \frac{I_{d0}}{V_{d0}}$$

is the Saturation Conductance.

$$V_{out} = V_{in}(0)\left(A_1 e^{-\lambda_1 t} + A_2 e^{-\lambda_2 t}\right) \tag{11}$$

$$\lambda_{1=2} = \frac{-\gamma \pm \sqrt{\left(\gamma^2 - \frac{4}{\frac{L}{\sqrt{f}}C}\right)}}{2} \tag{12}$$

$$\gamma = \frac{\psi_{d0}R\sqrt{f}+1}{\psi_{d0}L/\sqrt{f}} \tag{13}$$

and $A_1 = \frac{\gamma-\lambda_1}{\lambda_2-\lambda_1}$, $A_2 = \frac{\gamma-\lambda_2}{\lambda_1-\lambda_2}$.

Delay is expressed by the following expression:

$$t = \frac{\ln(A_2) + \ln\left(\frac{V_c(0)}{V_{out}(t)}\right)}{2\lambda_1 + \lambda_2} \tag{14}$$

For 50% delay, $V_{out}(t) = V_c(0)$ then,

$$t = \frac{\ln(A_2) + \ln\left(\frac{V_c(0)}{0.5V_c(0)}\right)}{2\lambda_1 + \lambda_2} \tag{15}$$

$$t = \frac{\ln(A_2) + 0.0693}{2\lambda_1 + \lambda_2} \tag{16}$$

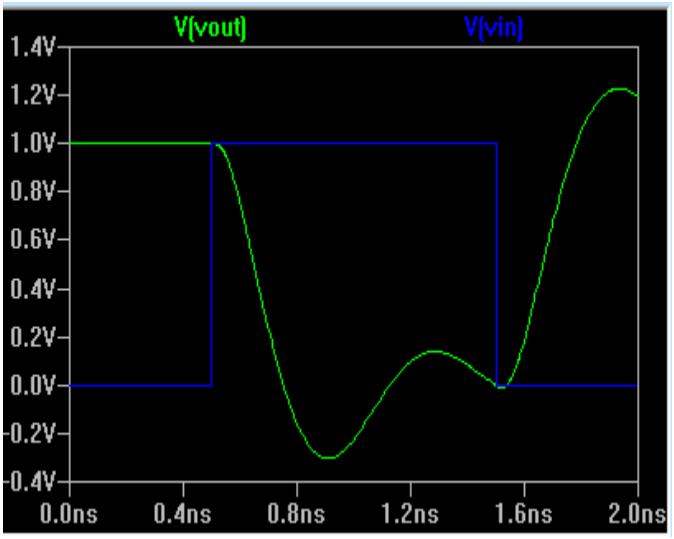

Figure 4: Delay Characteristics of CMOS Inverter without Skin Effect

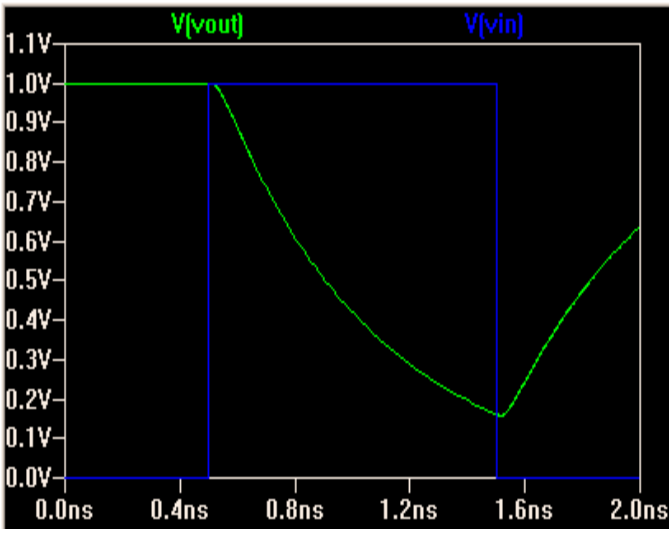

Figure 5: Delay Characteristics of CMOS Inverter with Skin Effect

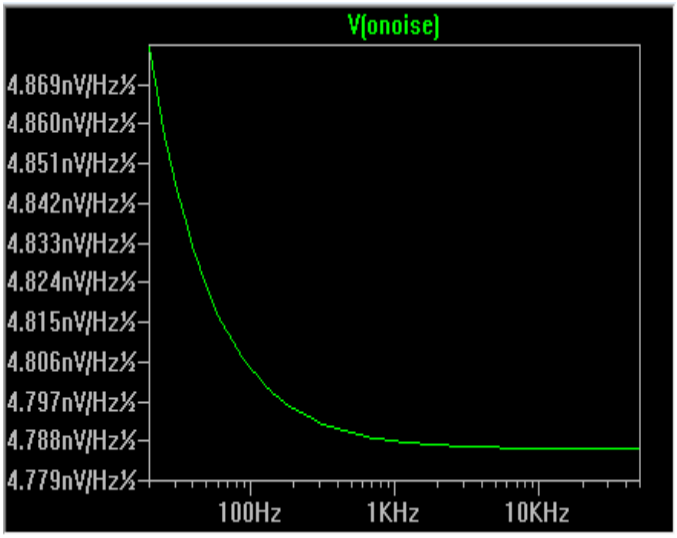

Figure 6: Output Noise Characteristics of CMOS Inverter without Skin Effect

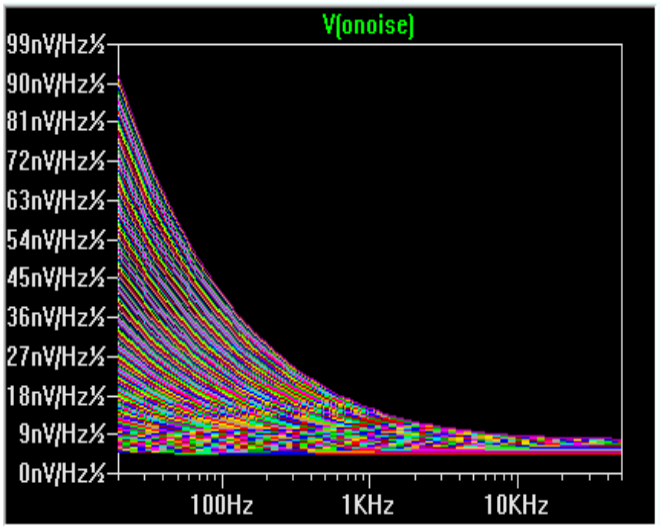

Figure 8: Output Noise Characteristics of CMOS Inverter without Skin Effect, at different temperatures

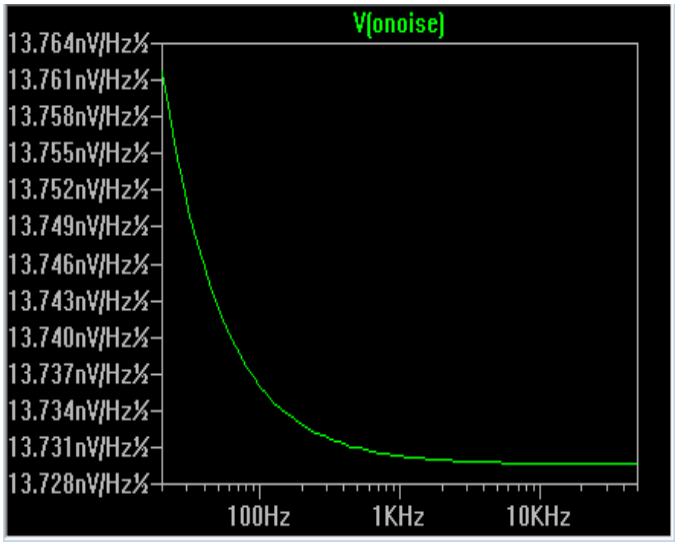

Figure 7: Output Noise Characteristics of CMOS Inverter with Skin Effect

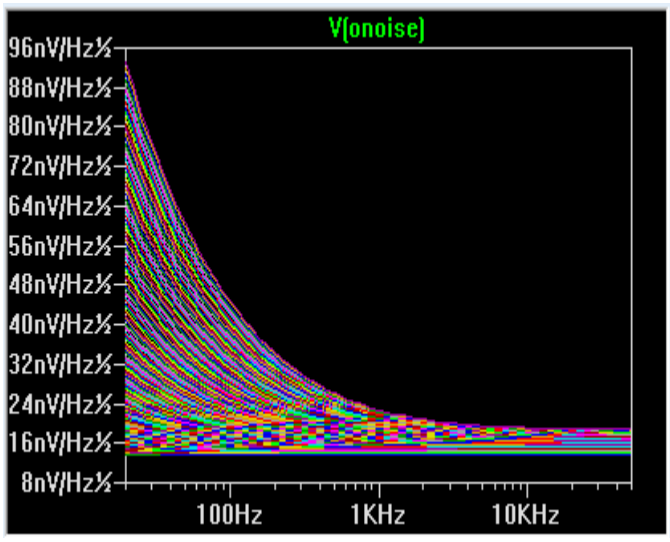

Figure 9: Output Noise Characteristics of CMOS Inverter with Skin Effect, at different temperatures.

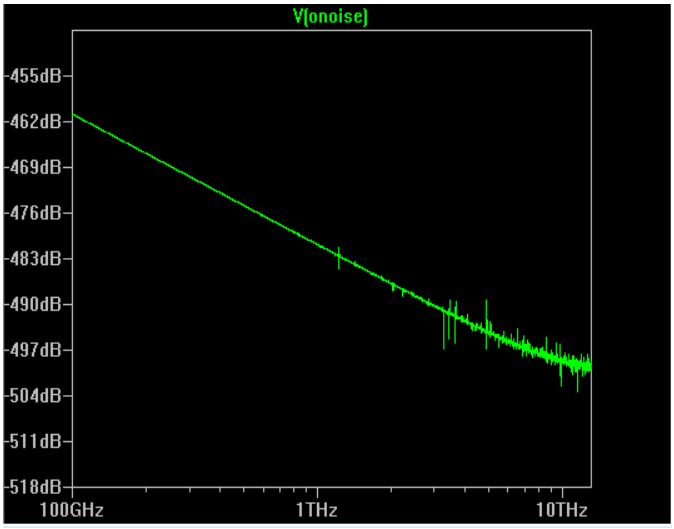

Figure 10: Total Harmonic Distortion of CMOS Inverter without Skin Effect

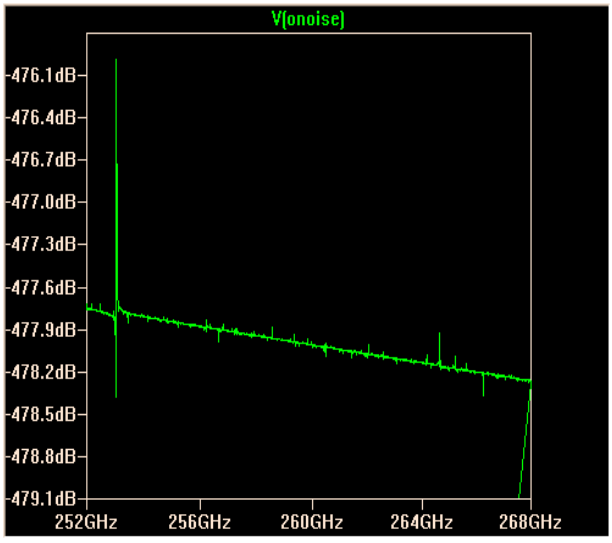

Figure 11: Total Harmonic Distortion of CMOS Inverter with Skin Effect

IV. CONCLUSION

A simple and efficacious model describing the affect of Skin Effect on the characteristics of a CMOS inverter are elaborated with the help of equations as well as using SPICE simulation. Results are represented along Figure 4 to Figure 11. Delay equation accurately explains the percussion of Skin Effect on it. As previously explained in section III that under the influence of skin effect the resistance and inductance becomes frequency dependent, the simulation results clearly interpret this concept and accommodate the fact that under the perturbation of Skin Effect the delay has been increased as shown in Figure 5. The impact of Skin Effect on noise in Figure 7 provides the obvious conclusion that in the presence of Skin Effect the output noise level increases. In Figure 6 the noise level is 4.698nV/Hz$^{1/2}$ where as the noise level under the influence of Skin Effect is 13.761nV/Hz$^{1/2}$. Similarly under the influence of Skin Effect when temperature is taken into account the minimum noise level is 16nV/Hz$^{1/2}$. In case of total harmonic distortion (THD) the level of distortion when skin effect was not there accounted in THz range of frequency with almost linear decay in distortion but in case of skin effect consideration the distortion starts taking place at GHz range of frequency. These results provides enough evidence that in the presence of skin effect CMOS characteristics vary dramatically which can influence the system evoking integrity and response.

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