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AN ANALYTICAL SURFACE POTENTIAL MODEL FOR STRAINED-Si ON SILICON-GERMANIUM MOSFET INCLUDING THE EFFECTS OF INTERFACE CHARGES

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ABSTRACT

In this paper, an analytical surface potential model is developed for short-channel Strained-Si on Silicon-Germanium MOSFET including the effect of interface charges, which are both positive and negative in polarity. The two-dimensional Poisson's equation is solved in the undamaged and damaged strained-Si and relaxed $Si_{1-x}Ge_x$ regions to find the surface potential in the channel. The effects of variations in damaged length and interface charge density on the surface potential are discussed comprehensively. The surface potential dependency on the variation in the germanium mole fraction of silicon-germanium layer is also discussed. The results obtained from the developed model have been compared with the numerical simulations obtained using ATLAS™ from Silvaco Inc.

Keywords: Strained, Silicon, Germanium, MOSFET, Interface, Surface potential.

I. INTRODUCTION

The use of strained-silicon channel has become an unavoidable feature for sub 100nm regime of the CMOS technology to maintain the expected performance improvements through scaling [1]. Strained-silicon (s-Si) on silicon-germanium ($Si_{1-x}Ge_x$, where x is germanium mole fraction) MOSFETs offer better performance than conventional MOSFETs due to its higher electron and hole mobility. Oberhuber *et al* [2,3] confirms a mobility enhancement factor up to 2.3 (56%) for germanium concentrations of 30% in the substrate and even higher enhancements for higher Ge content. However, hot-carrier induced interface charges grievously affect the scaled device performance [4,5] and further downscaling of device makes the short-channel effects (SCEs) severe [5,6]. It has been reported that the performance of the nanometer strained-Si devices is significantly dependent on the interface state charges at the Si/SiO_2 interface near the drain [7, 8, 9]. Thus, it becomes obligatory to investigate the depth up to which the interface charges can affect the performance of short-channel s-Si on $Si_{1-x}Ge_x$ MOSFETs. It is a well known fact that the analytical modelling of surface potential is essential to model other device parameters like threshold voltage, sub-threshold current and subthreshold swing of a short-channel MOSFET device[10].

In this paper, a surface potential model is presented for s-Si on $Si_{1-x}Ge_x$ MOSFETs including the effects of interface charges. Although the actual distribution of interface charges resembles a Gaussian profile, yet for a thin layer of gate oxide it can be approximated as a uniform profile [6, 7]. Hence, a uniform distribution of localized charges has been taken into consideration. All the theoretical results have been compared with the 2D simulation results obtained by commercially available ATLAS ™, a 2D device simulator.[11]

II. BAND STRUCTURE

Fig. 2 displays the change in silicon energy band structure because of strain in the silicon channel. The device simulator model library of ATLAS™, thus, has been modified according to the effects of strain on Si

band structure [9]. The effects of strain on Si band structure can be modeled as [12]

$$(\Delta E_C)_{s-Si} = 0.57x \quad (1)$$

$$(\Delta E_g)_{s-Si} = 0.40x \quad (2)$$

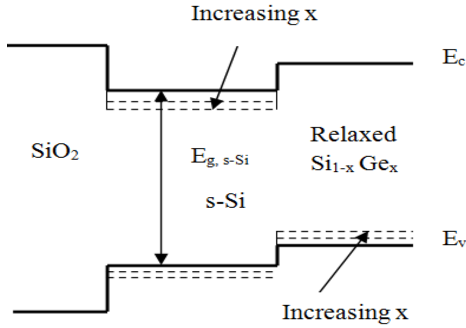

Fig. 1: Effect of strain on band structure of Silicon

$$V_T \log\left(\frac{N_{v,Si}}{N_{v,s-Si}}\right) = V_T \log\left(\frac{m^*_{h,Si}}{m^*_{h,s-Si}}\right) \approx 0.075x \quad (3)$$

where, x is the Ge mole fraction in the $Si_{1-x}Ge_x$ substrate; $(\Delta E_C)_{s-Si}$ is the increase in electron affinity of silicon due to strain; $(\Delta E_g)_{s-Si}$ is the decrease in the band gap of silicon due to strain; V_T is the thermal voltage; m^*_h is the hole effective mass; $(\Delta V_{bi})_{s-Si}$ is the change in built-in voltage; $N_{v,Si}$ and $N_{v,s-Si}$ are the density of states in the valance band in normal and strained silicon, respectively and q is the electronic charge.

The energy band parameters for $Si_{1-x}Ge_x$ substrate have been estimated as follows.

$$(\Delta E_g)_{SiGe} = 0.467x \quad (4)$$

$$N_{vSiGe} = (0.6x + 1.04(1-x)) \times 10^{19}\,\mathrm{cm}^{-3} \quad (5)$$

$$\varepsilon_{SiGe} = 11.8 + 4.2x \quad (6)$$

where, $(\Delta E_g)_{SiGe}$ is the decrease in the band gap of $Si_{1-x}Ge_x$; $N_{v,SiGe}$ is the density of states in the valance band of the relaxed $Si_{1-x}Ge_x$ film and ε_{SiGe} is the permittivity of the $Si_{1-x}Ge_x$. .

The effect of strain on front-channel flat-band voltage can be modeled as

$$(V_{FB,f})_{s-Si} = (V_{FB,f})_{Si} + \Delta V_{FB,f} \quad (7)$$

where, $$(V_{FB,f})_{Si} = \phi_M - \phi_{Si} \quad (8)$$

$$\Delta V_{FB,f} = -\frac{(\Delta E_C)_{s-Si}}{q} - \frac{(\Delta E_g)_{s-Si}}{q} - V_T \ln\frac{N_{V,Si}}{N_{V,s-Si}} \quad (9)$$

ϕ_M, χ_s and E_g are the metal work function, electron affinity and band gap of the silicon, respectively;

$$\phi_{Si} = \frac{\chi_{Si}}{q} + \frac{E_{g,Si}}{2q} + \phi_{f,Si}\ ,\ \phi_{f,Si} = V_T \ln\left(\frac{N_a}{n_{i,Si}}\right) \quad (10)$$

here, ϕ_{si} is the unstrained Si work function, $\phi_{f,si}$ is the Fermi potential in unstrained Si, q is the electronic charge, N_a is the body doping concentration and $n_{i,si}$ is the intrinsic carrier concentration in unstrained Si.

The built-in voltage across the source-body and drain-body junctions in the strained-Si thin film is also affected by strain as

$$V_{bi,SiGe} = V_{bi,Si} + (\Delta V_{bi})_{SiGe} \quad (11)$$

$$V_{bi,Si} = \frac{E_{g,Si}}{2q} + \phi_{f,Si} \quad (12)$$

$$(\Delta V_{bi})_{s-Si} = \frac{-(\Delta E_g)_{s-Si}}{q} - V_T \ln\frac{N_{V,Si}}{N_{V,s-Si}} \quad (13)$$

III. DEVICE STRUCTURE

Fig. 2 shows the schematic cross sectional view of the strained-Si on $Si_{1-x}Ge_x$ MOSFET structure with induced localized charges in the oxide layer towards the drain. The interface charge density in the damaged oxide region is assumed to be $N_f cm^{-2}$. L_1 and L_d are undamaged and damaged region lengths respectively. $L=L_1+L_d$ is total taken channel length. The symbols t_{Si}, t_f and t_{SiGe} represents the thicknesses of the strained-Si, front gate oxide and $Si_{1-x}Ge_x$ layers respectively.

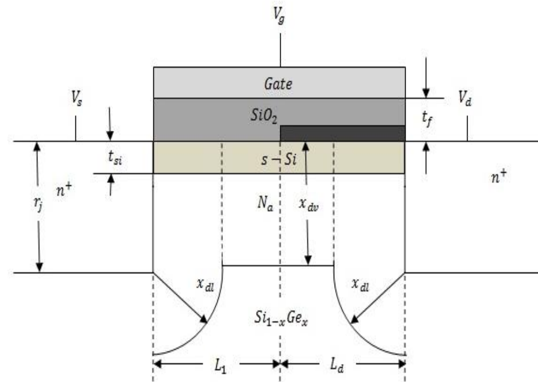

Fig. 2: Cross sectional view of Strained-Si on SiGe MOSFET

As shown in Fig.2, the depletion region is not uniform and hence a box type approximation of the depletion region is considered. The device structure with modified depletion region is shown in Fig.3. Charge density $N_{a,eff}$ and depth of depletion thickness x_d of approximated depletion region are defined as

$$N_{a,eff} = N_a\left[1-\left(\left(1+\frac{2x_{dv}}{r_j}\right)^{\frac{1}{2}}-1\right)\frac{r_j}{L}\right] \tag{14}$$

and

$$x_d \cong \frac{2x_{dl}\left(r_j+\frac{\pi}{4}x_{dl}\right)+(L-2x_{dl})x_{dv}}{L} \quad \text{for} \quad L \geq 2x_{dl} \tag{15}$$

$$x_d \cong r_j+\left(x_{dl}^2-\frac{L^2}{4}\right)^{\frac{1}{2}}+\frac{\theta}{2}x_{dl} \quad \text{for} \quad L \leq 2x_{dl} \tag{16}$$

where, $\theta = \sin^{-1}\left(\frac{L}{2x_{dl}}\right)$ (17)

x_{dl} and x_{dv} lateral and vertical source-body (drain-body) depletion region width.[xyz]

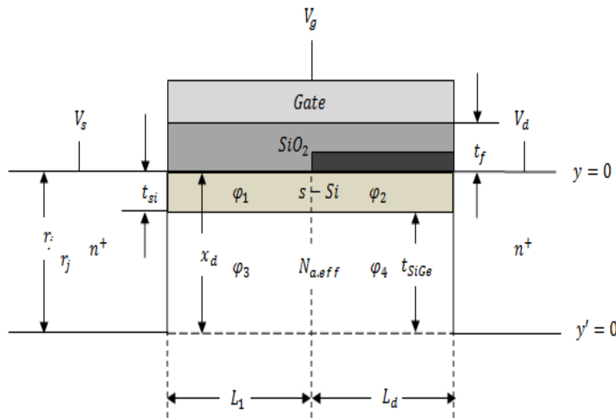

Fig. 3: Box approximation of the depletion region

As shown in Fig.3, depletion region is divided into the undamaged region represented by regions 1 and 3 whereas the damaged region is represented by regions 2 and 4.

IV. SURFACE POTENTIAL MODELING

To find out the potential distribution $\phi(x,y)$ in the channel region, the following 2D Poisson's equations have been solved in all the four regions of strained-Si and relaxed $Si_{1-x}Ge_x$ layers

$$\frac{\partial^2\phi_{i,j}(x,y)}{\partial x^2}+\frac{\partial^2\phi_{i,j}(x,y)}{\partial y^2}=\frac{qN_{a,eff}}{\varepsilon_{Si,SiGe}} \tag{18}$$

For $Si_{1-x}Ge_x$ layer, y-coordinate should be considered as y' shown in Fig.3. Subscripts denote the channel region as i stand for 1 and 2 whereas j stands for 3 and 4; N_a is the body doping concentration; q is the electronic charge; ε_{Si} and ε_{SiGe} are the permittivity of strained-Si film and relaxed $Si_{1-x}Ge_x$. The coefficients $C_{i(j)}$ are the functions of x only. The potential distributions in all the four regions are approximated by parabolic approximation [10] as

$$\phi_i(x,y)=\phi_{si}(x)+C_{i1}(x)y+C_{i2}(x)y^2 \tag{19}$$

$$\phi_j(x,y')=\phi_{bj}(x)+C_{j1}(x)y'+C_{j2}(x)y'^2 \tag{20}$$

Here, ϕ_{si} is the surface potential at SiO_2/s-Si interface for both damaged and undamaged regions. The continuity of potential and electric field across the interface of undamaged and damaged regions are:

$$\phi_1(L_1,0)=\phi_2(L_1,0) \tag{21}$$

$$\phi_3(L_1,0)=\phi_4(L_1,0) \tag{22}$$

$$\left[\frac{\partial\phi_1(x,y)}{\partial x}\right]_{x=L_1}=\left[\frac{\partial\phi_2(x,y)}{\partial x}\right]_{x=L_1} \tag{23}$$

$$\left[\frac{\partial\phi_3(x,y')}{\partial x}\right]_{x=L_1}=\left[\frac{\partial\phi_4(x,y')}{\partial x}\right]_{x=L_1} \tag{24}$$

Electric flux at SiO_2/s-Si interface should be continuous in the undamaged and damaged regions:

$$\left[\frac{\partial\phi_1(x,y')}{\partial y}\right]_{y=0}=\frac{\varepsilon_f}{\varepsilon_{Si}}\frac{\phi_{s1}-V'_{gs}}{t_f} \tag{25}$$

$$\left[\frac{\partial\phi_2(x,y')}{\partial y}\right]_{y=0}=\frac{\varepsilon_f}{\varepsilon_{Si}}\frac{\phi_{s1}-V''_{gs}}{t_f} \tag{26}$$

where ε_f is the permittivity of the SiO_2, t_f is the thickness of front gate oxide.

$$V'_{gs}=V_{gs}-(V_{FB,f})_{s-Si} \tag{27}$$

$$V''_{gs}=V_{gs}-(V_{FB,f})_{s-Si}\pm qN_f/C_f \tag{28}$$

with V_{gs} as the gate to source voltage, $(V_{FB,f})_{s-Si}$ is the front channel flat-band voltage of strained-Si film and.

$\pm qN_f$ represents the amount of charge of any polarity (positive/negative) trapped in the oxide.
Electric flux at $Si_{1-x}Ge_x$ and Si substrate interface is continuous and is given as

$$\left[\frac{\partial \phi_3(x, y')}{\partial y'}\right]_{y'=0} = 0 \tag{29}$$

$$\left[\frac{\partial \phi_4(x, y')}{\partial y'}\right]_{y'=0} = 0 \tag{30}$$

The potential and electric field at the $Si/Si_{1-x}Ge_x$ interface should be equal and continuous respectively as

$$\phi_1(x, t_{Si}) = \phi_3(x, t_{SiGe}) \tag{31}$$

$$\left[\frac{\partial \phi_1(x, y)}{\partial y}\right]_{y=t_{Si}} = -\frac{\varepsilon_{SiGe}}{\varepsilon_{Si}}\left[\frac{\partial \phi_3(x, y')}{\partial y'}\right]_{y'=t_{SiGe}} \tag{32}$$

$$\phi_2(x, t_{Si}) = \phi_4(x, t_{SiGe}) \tag{33}$$

$$\left[\frac{\partial \phi_2(x, y)}{\partial y}\right]_{y=t_{Si}} = -\frac{\varepsilon_{SiGe}}{\varepsilon_{Si}}\left[\frac{\partial \phi_4(x, y')}{\partial y'}\right]_{y'=t_{SiGe}} \tag{34}$$

The potentials at the source and drain end can be given by

$$\phi_1(0,0) = V_{bi,s-Si} \tag{35}$$

$$\phi_3(0,0) = V_{bi,SiGe} \tag{36}$$

$$\phi_2(0, L) = V_{bi,s-Si} + V_{ds} \tag{37}$$

$$\phi_4(0, L) = V_{bi,SiGe} + V_{ds} \tag{38}$$

where $V_{bi,s-Si}$ is the built-in voltage for strained-Si and $V_{bi,SiGe}$ is the built-in voltage for $Si_{1-x}Ge_x$; V_{ds} is drain-to-source voltage.
Solving eq. (18) and (19), (20), using the boundary conditions described from (21) to (38) forms the one dimensional differential equation of the surface potential as

$$\frac{\partial^2 \phi_{si}(x)}{\partial x^2} - P\phi_{si}(x) = Q_i \tag{39}$$

where, $$P = \frac{\alpha_1\alpha_2 - \beta_1\beta_2}{\alpha_1 + \alpha_2} \tag{40}$$

$$Q_1 = \frac{\alpha_2\gamma_1 + \beta_1\gamma_3}{\alpha_1 + \alpha_2} \tag{41}$$

$$Q_2 = \frac{\alpha_2\gamma_2 + \beta_1\gamma_4}{\alpha_1 + \alpha_2} \tag{42}$$

$$\alpha_1 = \alpha_2 = \frac{2C_{sige}C_{si} + 2C_f C_{sige} + C_f C_{si}}{C_{si}(C_{sige} + C_{si})t_{si}^2} \tag{43}$$

$$\beta_1 = \beta_2 = \frac{2C_{sige}}{(C_{sige} + C_{si})t_{si}^2} \tag{44}$$

$$\gamma_1 = \frac{qN_a}{\varepsilon_{si}} - \frac{C_f(2C_{sige} + C_{si})V'_{gs}}{C_{si}(C_{sige} + C_{si})t_{si}^2} \tag{45}$$

$$\gamma_2 = \frac{qN_a}{\varepsilon_{si}} - \frac{C_f(2C_{sige} + C_{si})V''_{gs}}{C_{si}(C_{sige} + C_{si})t_{si}^2} \tag{46}$$

$$\alpha_3 = \alpha_4 = \frac{2C_{Si}}{(C_{SiGe} + C_{Si})t_{SiGe}^2} \tag{47}$$

$$\beta_3 = \beta_4 = \frac{2C_{Si} + C_f}{(C_{SiGe} + C_{Si})t_{SiGe}^2} \tag{48}$$

$$\gamma_3 = \frac{qN_a}{\varepsilon_{sige}} + \frac{C_f C_{sige}V'_{gs}}{C_{sige}(C_{sige} + C_{si})t_{sige}^2} \tag{49}$$

$$\gamma_4 = \frac{qN_a}{\varepsilon_{sige}} + \frac{C_f C_{sige}V''_{gs}}{C_{sige}(C_{sige} + C_{si})t_{sige}^2} \tag{50}$$

Final expressions of surface potential can be written as[10]

$$\phi_{s1} = \frac{\psi_{d1}\sinh(\lambda x) - \psi_{s1}\sinh(\lambda(x - L_1))}{\sinh(\lambda L_1)} - \sigma_1 \tag{51}$$

$$\phi_{s2} = \frac{\psi_{d2}\sinh(\lambda(x - L_1)) - \psi_{s2}\sinh(\lambda(x - L))}{\sinh(\lambda L_d)} - \sigma_2 \tag{52}$$

$$\lambda = \sqrt{P} \tag{53}$$

$$\sigma_i = \frac{Q_i}{P} \tag{54}$$

$$\psi_{s1} = V_{bi,s-Si} + \sigma_1 \tag{55}$$

$$\psi_{d2} = V_{bi,s-Si} + V_{ds} + \sigma_2 \tag{56}$$

$$\psi_{d1} = V_p + \sigma_1 \tag{57}$$

$$\psi_{s2} = V_p + \sigma_2 \tag{58}$$

$\lambda, \psi_{s1}, \psi_{s2}, \psi_{d1}, \psi_{d2}, \sigma_1$ and σ_2 are the constants obtained from the boundary conditions mentioned above.

$$V_p = \frac{\psi_{d2}\cos ech(\lambda L_d) + \psi_{s1}\cos ech(\lambda L_1) - \sigma_1\coth(\lambda L_1) - \sigma_2\coth(\lambda L_d)}{\coth(\lambda L_1) + \coth(\lambda L_d)} \tag{59}$$

Table 1: Device parameters used in the simulation

Parameter	Value
Ge mole fraction in SiGe substrate	0-0.4 (0-40%)
Source /Drain doping	10^{20} cm^{-3}
Body doping	$10^{17} cm^{-3}$
Oxide thickness,	2 nm
Gate Metal work function	4.77eV
Strained Si film thickness	15 nm, 10 nm
Source/Drain junction depth	20 nm
Drain bias	0.5 mV
Interface trapped charges,	$5x10^{12} cm^{-2}$

V. RESULTS AND DISCUSSION

The comparison between the analytical results obtained from our proposed model with the numerical simulation data extracted from simulating the device structure under consideration with a commercially available 2D device simulator ATLAS™ [8] is been presented. All the modifications are made in ATLAS library to include the effects of strain as discussed in Sec. II. The model shows an excellent agreement with the simulated results as shown.

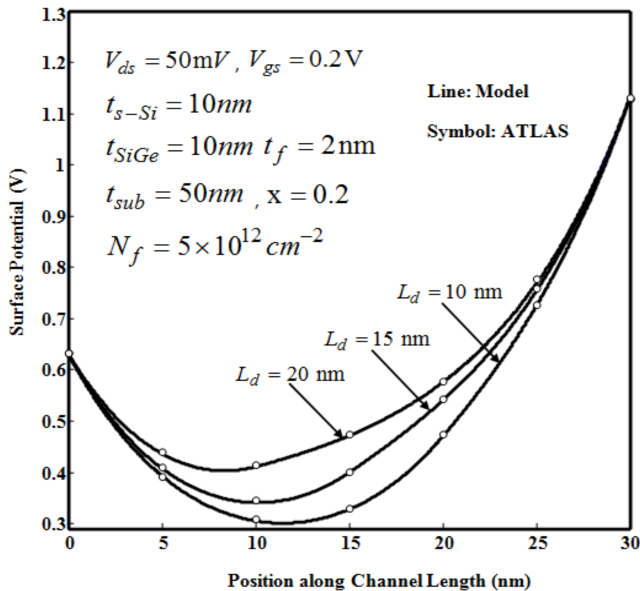

Fig. 4: Surface Potential Variation along the channel length x for various damaged region length

Fig.4 shows the surface potential variation of strained Si on $Si_{1-x}Ge_x$ MOSFET for different lengths of the damaged region. From the comparison, a step change of the potential along the channel is observed at the interface of the damaged and the undamaged regions. It is also seen that increase in the length of damaged region lowers the potential barrier height. Due to this reduction of potential barrier, threshold voltage reduces and subthreshold leakage current increases. Thus, the SCE increases with increase in damaged length in the oxide.

Fig. 5 shows a channel potential variation for various polar charges trapped in the oxide for a damaged length of L_d =15 nm. The positive trapped charges tends to pull up the surface potential curve with increased minimum surface potential whereas the negative charges pushes the potential curve down with a lower value of minimum potential. The positive charges reduce the potential barrier and the negative charges raises the barrier height. Hence, positive charges cause more SCE than the undamaged MOSFETs. This SCE increases with increase in the magnitude and bring more degrading performances. On the other hand, the negative charge shows more immunity to the SCE. The SCE decreases with increase in the magnitude of the negative charges in the oxide.

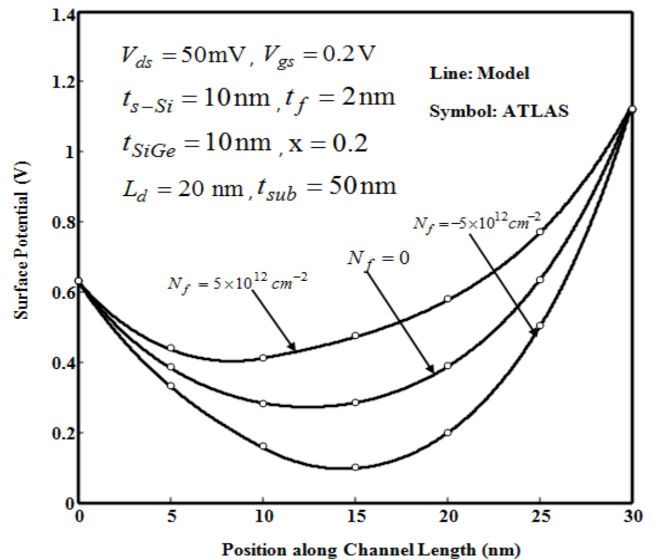

Fig. 5: Surface Potential Variation along the channel length x for various trapped charge magnitude and polarity

Fig. 6 shows the channel potential variation for different values of V_{ds} at a damaged length of =20nm for a positive interface charge, $N_f = 5x10^{12} cm^{-2}$. For each value of the drain voltage the mole fraction of the Ge in $Si_{1-x}Ge_x$ is varied. For a fixed amount of mole fraction, the potential height rises with the rise in V_{ds}. From the graph it is evident that this rise in potential barrier is significantly large for mole fraction of x=0

than that for x=0.4 (This effect is termed as drain induced barrier lowering (DIBL)).

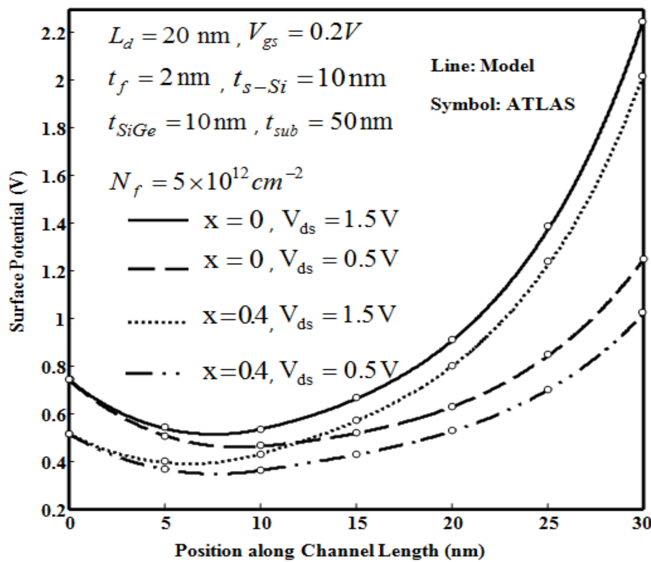

Fig. 6: Surface Potential Variation along the channel length x for different drain voltage and Ge mole fraction variation

Thus, it can be concluded that for a lower value of the mole fraction, the drain has more control over the channel potential than that for a higher value of mole fraction. In short, higher strain in Si causes more immunity to SCE. Also increasing strain enhances the mobility of the carriers in the channel region.

VI. CONCLUSION

An analytical surface potential model is derived including the effect of both positive and negative interface charges generated due to the hot carrier effects. The SCE increases with the damaged length of the oxide. Also the SCE increases with the increase in magnitude of positive trapped charges and it reduces with increase in negative trapped charges. One more finding was that increasing strain in the silicon channel suppresses short-channel effect (DIBL) and enhances the carrier mobility. Thus the concept of strain can be used to curb the SCE in sub 50nm technology and is an effective means of channel engineering. The proposed model results are in good agreement with the 2D device ATLAS™ simulator results and also with the physical understanding of the strain theory.

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