Journal of Electron Devices, Vol. 15, 2012, pp. 1241-1248

© JED [ISSN: 1682 -3427]

Journal of Electron Devices
www.jeldev.org

DESIGN AND RELIABILITY ANALYSIS OF A 4:1 MUX USING SINGLE ELECTRON TUNNELING TECHNOLOGY BASED THRESHOLD LOGIC GATE

Amit Jain, Subir Kumar Sarkar
Department of Electronics and Telecommunication Engineering
Jadavpur University, Kolkata-700032, India
amit2_8@yahoo.co.in

Received 24-08-2012, online 12-09-2012

ABSTRACT
As single electron tunneling technology based threshold logic gate uses less no of tunnel junctions so it reduces the size of Boolean logic gate compare to single electron tunneling based logic gate and single electron transistor based logic gate. The design and simulation of a 4:1 multiplexer based on buffered threshold logic gate is presented in this paper. The logic operation is verified using Monte Carlo based simulation tool SIMON. The reliability of the designed circuit is analyzed using MATLAB and SIMON. A comparison of the reliability for normal and uniform distribution of background charges has been shown in the present work. The stability of the circuit is analyzed using free energy history diagram and stability plot. Also the stability analysis for different operating temperature has been shown in this paper.

Keywords: Single electron tunneling (SET), Threshold logic gate (TLG), Reliability Analysis, 4:1 Mux, Free Energy History Diagram, Stability Plot.

I. INTRODUCTION

Due to size limitations even with scaling down MOSFET technology cannot continue forever. It can hardly go beyond a few nanometers even if adequate lithographical technology is available. There have been reports, that the CMOS technology will presumably be continued up to the year 2014 by the well known scaling of structure geometry[1]. As a consequence the search for new principles of operation of the small size devices is becoming more and more important. Given the anticipated end of the CMOS era, several alternative technologies have been under investigation for the last two decades. These candidate technologies include, amongst others, Single Electron Device (SED), Carbon Nanotubes, Rapid Single Flux Quantum (RSFQ), Resonant Tunneling Diodes (RTD), and Magnetic Spin devices. The single electron tunneling (SET) technology is one of the most promising candidates to meet the required increase in density, performance and decrease in power dissipation [2-5]. The key property of single electron tunneling technology is the ability to control the transport of individual electrons. This property can be used to encode Boolean values directly as single electron charges. One approach for that as first suggested in [2] is based on the transport of single electron charge from one island to another through tunnel junctions, such that Boolean input signals consist of the presence or absence of the arriving charge. So, Threshold logic gate(TLG) can be an alternative to Boolean logic gates in terms of logic functions. C. Lageweg et al implemented threshold logic gate for the first time employing SET technology. A number of investigations have been reported regarding the threshold logic based designs and implementation of useful Boolean logic functions [7-9].Even though the design and simulation of single electron 4:1 multiplexer have been reported in literature [13],there is no report of threshold logic based design of 4:1 multiplexer. Hence we have reported here the design and reliability analysis of a 4:1 multiplexer using single electron tunneling technology based TLG as Single electron tunneling based threshold logic gate uses less number of tunnel junctions compares to SET based system, which reduces the size of the logic gates.

Low dimensional semiconducting device (like SET based threshold logic) based circuits are statistically less reliable due to its sensitiveness towards a variety of random noises [10]. So, an important issue with the threshold logic based gate is the reliability which depends on circuit structure, parameter values, temperature and random background charges. From

designer point of view the most important one is the random background charges as it can not be controlled by the designer and completely depends on the fabrication process. There have been reports [10-11] regarding the reliability analysis of threshold logic gate but there is no report on reliability analysis of threshold logic gate based logic circuits. In this paper we have focused on the reliability analysis of a 4:1 multiplexer. We have further analyzed the stability of the designed circuit.

The main contribution of this paper can be summarized as follows:

- The design and simulation of a 4:1 multiplexer using single electron tunneling technology based threshold logic gates.
- Reliability analysis of the proposed circuit with different background charge distribution.
- Stability analysis of the designed circuit with different operating temperature.

II. BACKGROUND

The basic element of single electron tunneling technology is the tunnel junction. A tunnel junction can be considered as two conductors separated by a thin layer of insulating material as shown in Fig.1. The tunnel junction is characterized by a capacitance C_j and a resistance R_j each of which depends on the physical size of the tunnel junction and the thickness of the insulator. As the thickness of the dielectric is very thin the tunnel junction can be considered as a leaky capacitor [12]. The transport of charges through a tunnel junction is referred to as tunneling [2]. The charge transport mechanism is discrete in nature[2]. The voltage that is needed across the tunnel junction for a tunnel event to occur is known as critical voltage. The value of the critical voltage is given by [2]:

$$V_c = \frac{e}{2(C_e + C_j)} \tag{1}$$

Where e=1.602*10^{-19}C, Cj is the tunnel junction capacitance and C_e is the equivalent capacitance for remainder of the circuit as seen from the tunnel junction perspective. A tunnel event will occur across the tunnel junction if and only if the voltage across the junction V_j is greater than or equal to V_c i.e

$$\left|V_j\right| \geq V_c \tag{2}$$

Otherwise the tunnel event will not occur and this phenomenon is known as coulomb blockade. If no tunnel event occurs in any of the tunnel junction in the circuit then the circuit is in a stable state. As the charge transport mechanism is stochastic in nature [2] so a limited number of tunnel events can be considered to occur during a stable state of the circuit. The switching delay of a single electron transport can be calculated as [2]

$$t_d = \frac{-\ln(P_{eror}) q_e R_t}{\left|V_j\right| - V_c} \tag{3}$$

Where R_t is the tunnel resistance and it is assumed to be $10^5\Omega$. P_{error} is the probability that the tunnel even has not occurred after t_d seconds. The energy consumed by a single tunnel event can be calculated by determining the difference in the total amount of energy present in the circuit before and after the tunnel event which can be calculated by [2]

$$\Delta E = E_{initial} - E_{final} = -q_e(\left|V_j\right| - V_c) \tag{4}$$

III. THRESHOLD LOGIC GATE

Threshold logic gate operates on a principle of comparison between the weighted sum of inputs and a threshold value. If the weighted sum of inputs is greater than or equal to the threshold, the output is logic '1'.otherwise the output is a logic '0'. The function which satisfies the above conditions is given by [12]

$$\mathrm{F(X)} = sgn\{\mathrm{Y(X)}\} = \begin{cases} \text{if} \quad F(\mathrm{X}) < 0 \\ \text{if} \quad F(\mathrm{X}) \geq 0 \end{cases} \tag{5}$$

$$F(X) = \sum_{i=1}^{n} w_i x_i - T \tag{6}$$

where x_i are the n boolean inputs and w_i are the corresponding n integer weights. The threshold gate implemented in [4] allows only for positive weights. However the threshold logic gate proposed in [6]

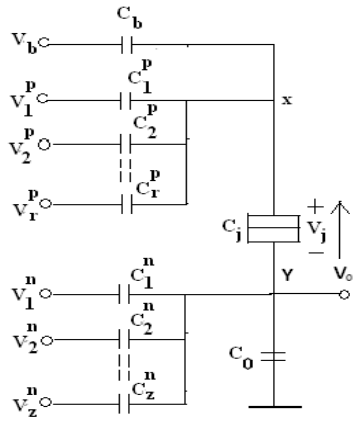


Fig.1: Threshold logic gate structure

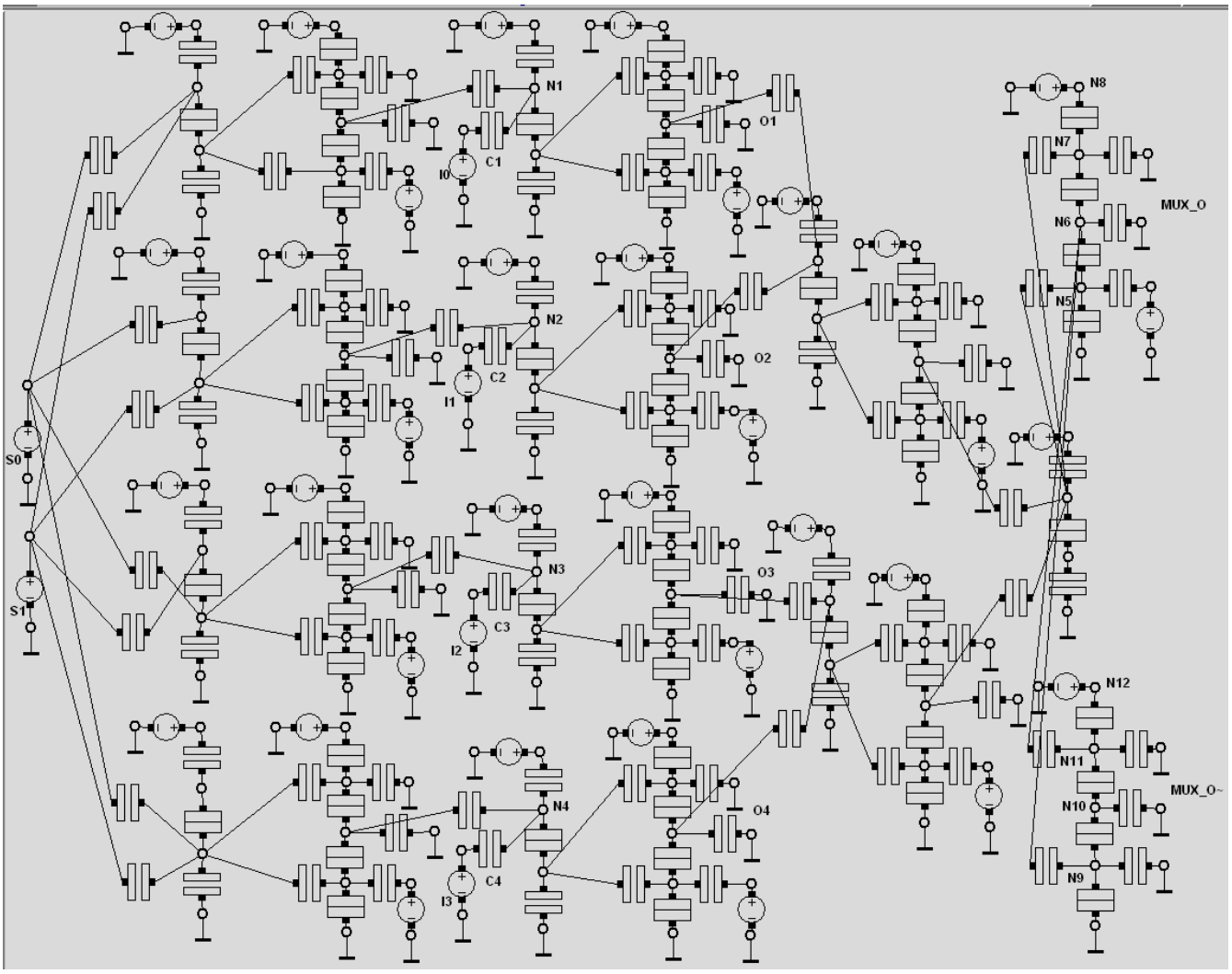


Fig. 2: The proposed circuit

allows for both positive and negative weights as shown in figure 1. The input voltages V_p(weighted by their input capacitors C_p) are added to the node x and inputs V_n(weighted by their input capacitors C_n) are subtracted from voltage across the junction. The bias voltage V_b is used to adjust the critical voltage V_c. the function F(X) for the circuit shown in Fig.1 is given by[6]

$$F(X) = C_{\Sigma}^{n} \sum_{k=1}^{r} C_K^P V_K^P - C_{\Sigma}^{P} \sum_{l=1}^{S} C_l^n V_l^n - T \qquad (7)$$

where

$$T = \frac{1}{2}(C_{\Sigma}^{P} + C_{\Sigma}^{n}) - C_{\Sigma}^{n} C_b V_b \qquad (8)$$

$$C_{\Sigma}^{p} = C_b + \sum_{k=1}^{r} C_k^P \qquad (9)$$

$$C_{\Sigma}^{n} = C_0 + \sum_{l=1}^{S} C_l^n \qquad (10)$$

In this brief we will assume the Boolean input/output signals correspond to the following voltages: logic 0= 0 V. and logic1=0.1*q_e/CV, where C=1aF which results in logic1=16 mV.

IV. THE PROPOSED CIRCUIT

In the proposed design of the multiplexer we have not used the conventional architecture of a multiplexer where two NOR gates, four three inputs AND gates and a four inputs OR gate are required. The proposed circuit is shown in Fig. 2, which consists of 101 nodes, 59 tunnel junctions and 104 capacitors. It has been reported that strong feedback effects occur in circuits consists of these gates so adding an active buffer at the output of the gate reduces the feedback effect considerably. Though the switching speed of the TLG is of the same order as electron tunneling

speed through a tunnel barrier, as output is taken from the island the practical implementation needs CMOS like SET inverters. That's why we have used buffered logic gates for the design. But to get the result correctly we need to place two cascaded buffer at the output of each gate, which makes the circuit bigger in size and takes lots of area. To solve this problem the circuit has been designed in a top-down manner and finally only one buffer has been added to each gate, so practically the circuit will not follow the conventional design flow, but it will operate like a multiplexer functionally. it is observed that the size of the designed circuit increases due to use of buffered logic gates but on the other hand it increases stability of the circuit We investigated that a three input or four input threshold logic gate does not work very well when incorporated in the circuit so we have used two input threshold logic gates in all cases. Only two different voltage sources have been used in the circuit whereas six different voltage sources have

Table 1
Different voltage sources

Voltage sources	V1(V)	V2(V)	V3(V)	V4(V)	V5(V)
Proposed Circuit	0.0160	0.0171			
[13]	0.115	0.113	0.110	0.1	0.083

been used in [13] as given in Table 1. S0 and S1 are two control signals and the four inputs are named as I0, I1, I2, and I3 as shown in Fig 2. For the buffer/inverter the parameters are taken from [2]. The proposed circuit has similar input and output digital levels i.e. high=16 mV and low=0 mV. The input voltages are applied to nodes N1, N2, N3, and N4 through the capacitors C1, C2, C3 and C4 respectively, which are identical, and their capacitance is 0.5 C. The output is taken from node N6. An electron tunneling from node N6 to Vdd1 corresponds to logic '1' as it leaves a positive charge in the output node. The absence of the positive charge in the island corresponds to logic '0'.

V. SIMULATION RESULTS AND DISCUSSION

The designed circuit has been tested using SIMON [12], a nanoelectronics structure simulation software. The control signals are piece wise linear and provides all four combinations of input. The input signals are either a logic '0' or a logic '1'. So depending upon the control signal's combination we will get the respective output. All the possible four outputs named as O1, O2, O3 and O4 have been shown in Fig. 3.The final output, MUX_O has been shown in Fig. 4 All the inputs corresponding to the control signal combination are given in Table 2. The control

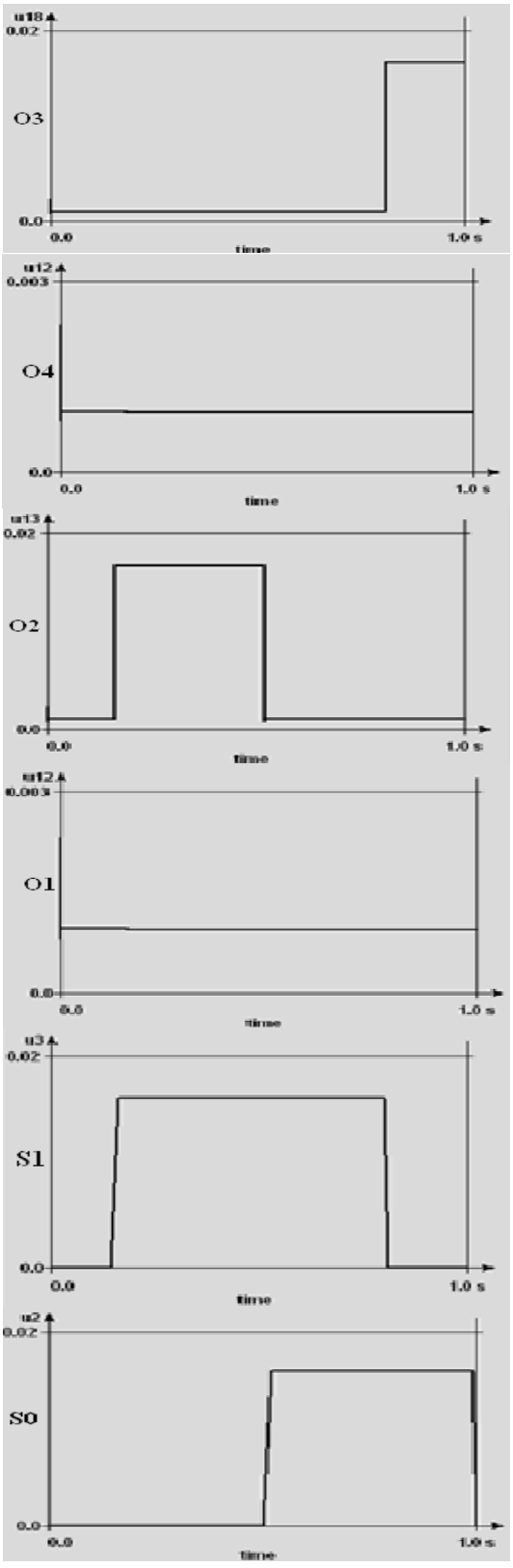


Fig. 3: Two control signals (S0 and S1) and four possible outputs (O1, O2, O3 and O4 corresponding to [S0, S1]=[0, 0], [0, 1], [1, 0] and [1, 1] respectively).

Table 2
Input's Values

S0	S1	INPUT(V)	Logic Value	Designation
0	0	0.0	'0'	I0
0	1	0.016	'1'	I1
1	0	0.0	'1'	I2
1	1	0.016	'0'	I3

signals S0 and S1 have been shown in Fig. 3. It can be observed from Fig. 3 that the value for both the signals O1 and O4 is 0.001V, which is being considered as logic '0'. A point to be noted here is we have used pulse wave form for control signals instead of using a DC signal of value 0.0V or 0.016V. If we would have used a DC signal as a control signal each time to check for all the possible combinations

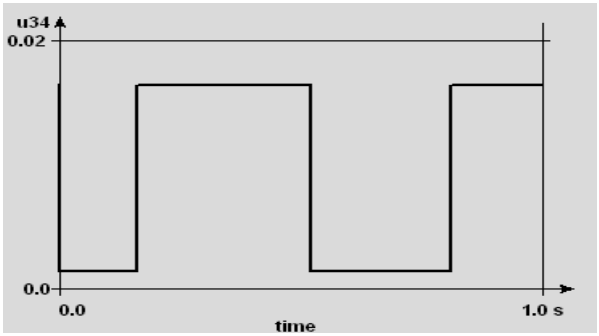


Fig. 4: Final Output of the Multiplexer

then we would have needed eight different signals with four for each of the control signal. But with the approach we have used we need only one variety for each of the control signal which obviously increases the readability of the circuit.

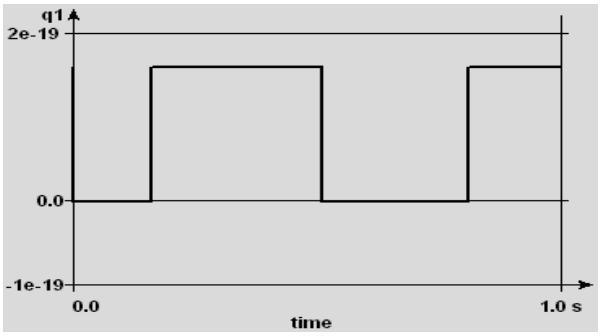


Fig.5: Time variation of the charge at the output node N5 of the designed circuit

The time variation of the charge at the output node N5 is shown in Fig. 5. It can be observed comparing Fig. 4 and Fig. 5 that the output is a logic '1' when there is a positive charge ($1.6*10^{-19}$) at the output node N5 and the output is a logic '0' if there is no charge at the output node. So it is concluded that only one electron is allowed to leave the output node for getting a logic '1' value.

VI. RELIABILITY ANALYSIS

At the time of fabrication random charges are produced as background charges on nodes of single electron devices. These background charges create extra voltage which eventually changes the total voltage across the junction [11], due to which the circuit may not work properly and the circuit becomes unreliable. As the charges produced are random in nature so practically it can take any kind of distribution. Here we have used the mostly used distributions namely uniform distribution and normal distribution to characterize the random charges.

i) Assuming all the nodes in the designed circuit have background charges with uniform probability distribution given by

$$p\left(\frac{z}{q_e}\right)=\begin{cases}\dfrac{1}{2\eta}, -\eta \le \dfrac{z}{q_e} \le +\eta \\ 0, otherwise\end{cases} \qquad (11)$$

where z is the random variable and q_e is the charge of an electron. So the range of the variable z is $\pm\eta q_e$. Here η represents the extent of the variation so it is called variation factor. The random data with uniform distribution has been generated using MATLAB's random number generation toolbox. The distribution of random data corresponding to η =0.04 has been shown in Fig. 6.

ii) It is assumed that the random background charges can take normal distribution with standard deviation σ:

$$p(z1)=1/(\sqrt{2\pi}\sigma)e^{-\frac{z_1^2}{2\sigma^2}} \qquad (12)$$

Where $z1=z/q_e$, and z is the random variable which represents the random background charge value. In case of normal distribution 98% of the area is within two standard deviation and 99.7% of the area is within three standard deviation [21] so the value of the standard deviation is taken as $(\sigma / q_e)=\eta$, where the range of the variable is $\pm\eta q_e$. The normally distributed data corresponding to η = 0.03 has been shown in Fig. 7. The reliability test for the designed circuit has been done as follows.

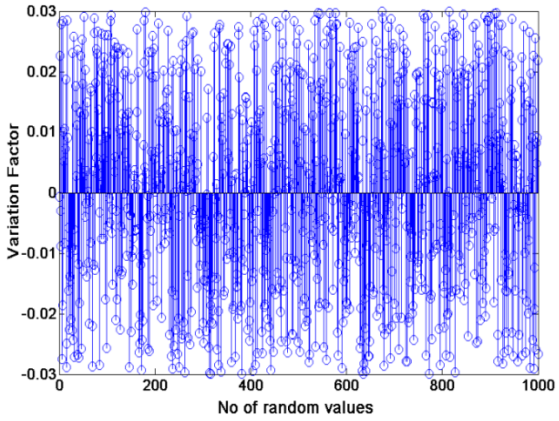


Fig. 6: Uniform distribution of random data

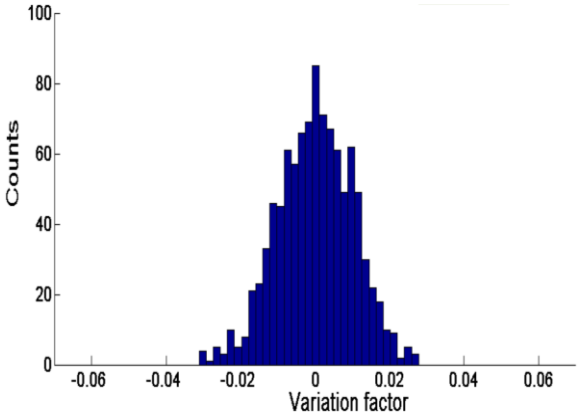


Fig. 7: Normal distribution of random data

1) Following uniform distribution random data are generated using MATLAB with $\eta = 0.01$.
2) The random data are distributed among all the 104 nodes and then the circuit is simulated with SIMON to check the operation.
3) Step 1-2 is repeated T=100 times with new random data.
4) If the no of correct outputs is S then the reliability r of the designed circuit is calculated as
   r = S/T (13)
5) Step 1-4 is repeated with η =0.02, 0.03 and 0.04.
6) Step 1-5 is repeated for normal distribution.

The plot corresponding to uniform and normal distribution of random background charges with different η value has been shown in Fig. 8. It can be analyzed comparing two plots that random background charges with normal distribution gives better reliability compare to uniform distribution. For the value of η =0.01 both distribution gives almost same result. In case of uniform distribution a large fall is noticed after η =0.02 which decreases the circuit reliability from 76% to 25%, and after η =0.035 the circuit becomes almost unreliable. But in case of normal distribution as it can be observed the circuit remains reliable for all the values of η with the lowest value of 40 %. The details data regarding circuit reliability with variation factor for both type of distribution are given in Table 3.

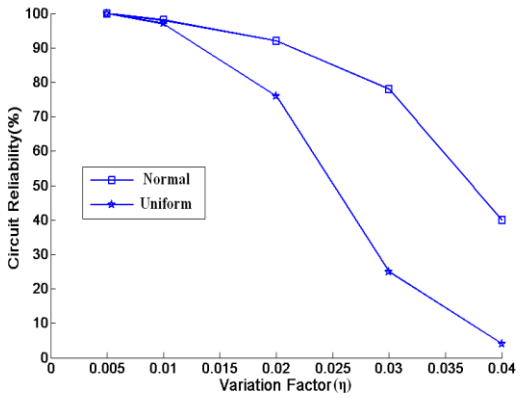


Fig. 8: Reliability of the circuit with normal and uniform distribution of background charges

Table 3
Details of circuit reliability with variation factor

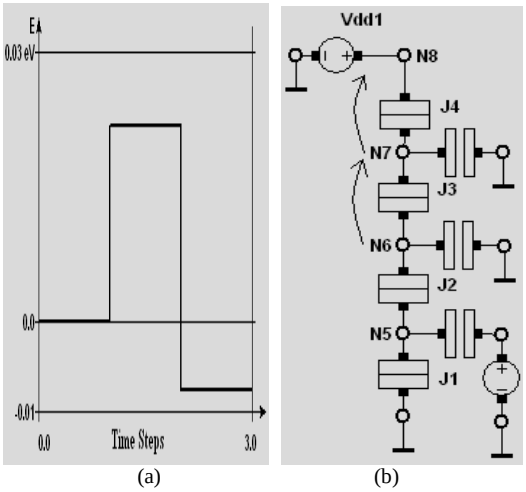
Variation Factor(η)	Circuit reliability (%)	
	Normal Distribution	Uniform Distribution
0.01	98	97
0.02	92	76
0.03	78	25
0.04	40	4

VII. STABILITY ANALYSIS

The free energy history diagram of the circuit for the transition of the output from '0' to '1' is shown in Fig. 9(a). Transportation of electron in the output buffer from node N6 to Vdd1 for this transition is shown in Fig. 9(b). In the first time step no charge is present in the node. In second time step electron tunnels from node N6 to node N7 via J3. Finally the electron is transported from node N7 to Vdd1 through J4 causing the system to reach a local minimum as shown in Fig. 9(a). So absence of electron in the node corresponds to a logic '1' value. The time steps in the Fig 9(a) define the time required for an electron to travel from one node to another. The free energy of the system is calculated as [2].

$$E_f = \sum_{i=1}^{3} E_{t_1} \qquad (14)$$

Where E_{t_i} is the free energy for each time step. The free energy corresponding to these is calculated as 0.044eV.



(a) (b)

Fig. 9: (a) Free energy history diagram, (b) Electron tunneling phenomena in the output buffer

The stable operation of the circuit is tested using SIMON. The stability plot of the designed circuit is shown in Fig. 10. Each point in the stability plot corresponds to a combination of two control signals. SIMON works on the principle of calculating free energy for each point on the stability plot. The local minima of the circuit free energy corresponds to a stable condition and these points are colored in white which also proves that these combinations of control signal vector prohibits electron tunneling, keeping the electrons in the islands. The points correspond to local maxima of the circuit free energy are colored black and considered as unstable points. The rest of the points are colored grey which stands for the justification of the small current that runs through the junctions. The points correspond to the input control signal vectors [0, 0], [0, 1], [1, 0], [1, 1] are presented as A, B, C and D respectively as shown in Fig. 10. It can be observed from the figure that all the four points are in stable regions.

One of the major concerns regarding the stability of the designed circuit is temperature. The charging energy that is the energy required for an electron to tunnel is given as [17]

$$E_c = e^2 / 2C \qquad (15)$$

Now if the available voltage sources couldn't provide this much energy then no electron tunneling takes

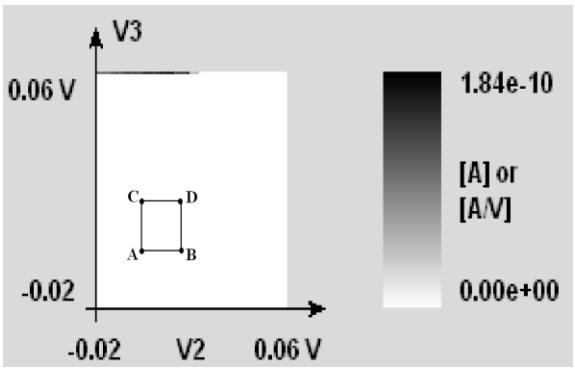


Fig. 10: Stability plot of the circuit with: A= [0, 0], B= [0, 1], C= [1, 0], D= [1,1] and T= 0 K.

place and the situation is known as coulomb blockade. If the available thermal energy is greater than the charging energy then electron tunneling occurs which results in instability of the circuit. So taking the thermal energy into consideration the condition for the stability is [17]

$$E_c = e^2 / 2C > k_B T \qquad (16)$$

To observe the stability dependence on the temperature, the stability of the circuit is again plotted with a increase in temperature as shown in Fig. 11. It can be observed that in Fig. 10 all the four points are colored white, which proves the designed circuit is stable for all the combinations of control input for the used range. But if we increase the temperature circuit becomes unstable. It is observed in Fig. 11 that local maxima of the circuit free energy corresponding to A, B, C, and D are increasing with increase in temperature which implies that with increase in temperature tunneling event increases which in turn increases the free energy of the system. The free energy corresponding to the most black colored points of Fig. 10 (T=0K) is 1.84e-10 which for Fig. 11(T=2K) is 2.76e-08.

.

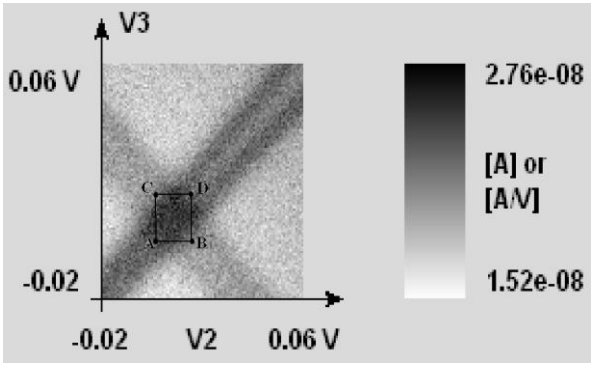


Fig. 11: Stability plot of the circuit with: A= [0, 0], B= [0, 1], C= [1, 0], D= [1, 1] and T=2 K

So it can be concluded that the free energy of the overall circuit is increasing with increase in temperature which implies that the no of tunneling event is increasing with increase in temperature causing the circuit to become unstable.

VIII. CONCLUSION

In this brief the design and simulation of a single electron 4:1 multiplexer is presented. A top down or behavioral approach has been used for designing the circuit. Buffered threshold logic gates have been used in the circuit as a defense for the feedback effect and to increase the stability. For the variation factor of 0.02 the circuit is highly reliable for both uniform and normal distribution of background charges. For values greater than 0.02 the circuit becomes less reliable for uniform distribution, but for normal distribution the circuit remains almost reliable. Circuit's stability is verified through stability plot and free energy history diagram using SIMON. It has been shown that the circuit's stability also depends on temperature and the stability plots related to this issue have been shown in this paper.

References

[1] N. Basanta Singh, Sanjoy Deb, Asish Kumar De and Subir Kumar Sarkar, "Design and Simulation of 2–to-4 Decoder Using Single Electron Tunneling Technology based Threshold Logic Gate" Journal of Electron Devices **9**, 342-351 (2011).

[2] C. Lageweg, S. Cotofana, and S. Vassilidis, "Single Electron Encoded Latches and Flip-Flops", IEEE Trans. On Nanotechnology **3**, 237-248 (2004).

[3] Chaohong Hu, Sorin Dan Cotofana, and Jianfei Jiang, "Single-Electron Tunneling Transistor Implementation of Periodic Symmetric Functions", IEEE Trans. Circuits & Systems-II: Express Briefs, **51**, 593-597 (2004).

[4] R.H Chen, A. N. Korotkov, and K. K.Likharev, "Single-electron transistor logic", Appl. Phys.Lett. **68**, 1954-1956 (1999).

[5] K. Likharev, "Single-Electron Devices and Their Application", Proc. IEEE **87**, 606-632 (1999).

[6] C. Lageweg, S. Cotofana, and S. Vassilladis, "A Linear Threshold Gate Implementation in Single Electron Technology," IEEE Computer Society Workshop on VLSI, pp. 93-98, April 2001.

[7] M. Avedillo, J. M. Quintana, A. Rueda, and E. Jimenez, "Low-power CMOS threshold-logic gate", Electric Letters, **31**, 2157-2159 (1995).

[8] J. Fernandez Ramos, J. A. Hidalgo Lopez, M. J. Martin, J. C. Tejero and A. Gago, "A threshold logic gate based on clocked coupled inverter, International Journal of Electronics **84**, 371-382 (1998).

[9] S. Muroga, Threshold Logic and its Applications, Wiley and Sons Inc. (1971).

[10] C. Chen, "A Statistical Reliability Model for Single Electron Threshold Logic" IEEE Trans. On Electron Devices **55**, 1547-1553 (2008).

[11] C. Chen and J. Mi, "parameter selection for single electron threshold logic with reliability analysis" Proc. IEEE Int. Conf. Nanotechnol., Cincinnati, OH, Jul. 2006, **1**, pp. 371-374.

[12] Santanu Mahapatra. Hybrid CMOS "Single-Electron-Transistor Device and Circuit Design" Artech House Publication (2006).

[13] T. Tsiolakis, N.Konofaos, G.Ph.Alexiou "A complementary single electron 4 bit multiplexer" Quality Electronic Design, 2nd Asia Symp. Patras, Greece, Aug. 2010, pp. 264-271.

[14] S. E. Rehan "The implementation of 2-bit decoder using single electron linear threshold gates" Int. Conf. On Microelectronics (ICN), Mansoura, Egypt, Dec. 2010, pp. 180-183..

[15] G. Zardalidis, I. Karafyllidis: "Design and simulation of a nanoelectronic single-electron control not gate", Microelectron. J., **37**, 94–97 (2006).

[16] Chirstoph Wasshuber, "SIMON-A simulator for single-electron tunnel devices and circuits", IEEE Trans. On Computer Aided Design of Integrated Circuits and Systems, **16**, 937-944 (1997).

[17] C. Wasshuber: "Computational Single-Electronics (Computational Microelectronics)", Springer, New York, (2001).

[18] G. Zardalidis, I. Karafyllidis: "A single-electron full adder", IEE Proc. Circuits, Dev. Syst., **150**, 173–177 (2003).

[19] I. Karafyllidis, "Single-electron OR gate", Electron. Lett., **36**, 407-408 (2000).

[20] T. Tsiolakis, N. Konofaos, G. Ph. Alexiou: "Design, simulation and performance evaluation of a single-electron 2-4 decoder", Microelectronics Journal **39**, 1613-1621 (2008).

[21] Jagdish K. Patel, Campbell B. Read "Handbook of the normal distribution"Taylor and Francis (1996).