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EFFECT OF BURIED OXIDE INTERFACE TRAP DENSITY ON FLICKER NOISE CHARACTERISTICS OF 0.25 μm FULLY DEPLETED SOI MOSFET

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ABSTRACT
In this paper, the effect of the change of trap density at the buried oxide interface on flicker noise in a 0.25 μm fully depleted Silicon on insulator (FD SOI) MOSFET is reported for the first time. The analytical model developed is based on number fluctuations which are caused by interactions between shallow donor type traps in the buried oxide and the holes at the buried oxide interface. It will be shown that the hole concentration at the back interface changes with trap density at the BOX interface. The change in hole concentration results in fluctuations in the drain current by modulating the flat band voltage. Further the fluctuations in the drain current are the measure of the flicker noise. Simulations demonstrate, that the proposed model correctly predicts the dependence of flicker noise on trap density at BOX interface and very little dependence on BOX thickness.
Index words: Donor Traps, Flat Band Voltage, Flicker Noise, Fully Depleted, SOI

I. INTRODUCTION

SOI technology has been widely demonstrated and recognized to be a mature and alternative technology to mainstream bulk silicon for the realization of high-speed, low-power RF and analog CMOS circuits [1]. Enhancement mode MOSFETs fabricated on thin SOI films have received much attention in ULSI applications due to improved isolation, reduced parasitic capacitance, and enhanced radiation hardness as compared to devices fabricated using bulk technology. There is increasing evidence that SOI MOSFETs also provide additional design and circuit flexibility when scaled down to DSM dimensions because of reduced short-channel effects [2].

However SOI device design is challenging, due to various undesired effects coming into play at low frequencies. One of the undesired parameter at low frequency is the role of Flicker Noise (also known as 1/f noise). Flicker noise is of more concern in SOI CMOS due to unfavorable quality of the silicon- buried oxide interface. The flicker noise (FN) is becoming a major concern for continuously scaled down devices, since it increases as the area of the device decreases [3]. The FN is also of paramount importance in RF circuit applications, where it gives rise to phase error or jitter in oscillators and mixers [3]. Therefore the accurate characterization of the noise behavior has to be established. The 1/*f* noise in MOS transistors imposes additional circuit design considerations and necessitates a good understanding of the noise mechanisms.

The modeling of the flicker noise in SOI MOSFETs is relevant in two respects:

(i) Evaluation of the device/circuit performance in terms of output noise level.

(ii) Characterization of interface film which represent the basic source of noise [4].

No flicker noise models till date has been specifically developed for SOI MOSFETs. Models used for flicker noise in bulk MOSFET are also used for SOI MOSFET. The previous work done in analysis and modeling of flicker noise in SOI MOSFET, most relevant to the present work is the study of the flicker noise in thin film fully depleted SOI MOSFETs. From this study, it was found that the flicker noise exhibited a dependence on the corresponding increase in the fraction of inversion charge at surface [5]. It was also found out that the low frequency noise in near FDSOI MOSFETs is dominated by a number fluctuation model [6]. Further in FD and PDSOI MOSFETs they found that 40 nm silicon film is not completely depleted, therefore the floating body effects induce a noise overshoot to the flicker noise [7]. Also the concept of back channel 1/f noise was introduced and showed that if the impurities in the BOX are more, the 1/f noise is increased [8].

As BOX is the only distinguishing feature between bulk MOSFET and SOI MOSFET. Therefore it becomes important to study its influence on the flicker noise characteristics. This helps in creating a marked difference between the bulk MOSFET flicker noise models and the SOI flicker noise models. In the next section origin of flicker noise is described.

II. PHYSICAL MODELING

The theories and models suggesting the origin of flicker noise in MOSFETs differ in details but all are based on either [9]: The McWhorter Model (Number Fluctuations) or The Hooge Model (Mobility Fluctuations). In addition to this the Correlated carrier and mobility fluctuation [9] models have also been developed. The McWhorter model is simple and shows excellent agreement with experiments, especially for NMOS transistors. However, the mobility

fluctuation noise model tends to better explain the 1/*f* noise in PMOS transistors. It was later observed that a trapped carrier also affects the surface mobility through Coulomb interaction. The so-called correlated mobility fluctuations formed the basis for the correlated number and mobility fluctuations model. However, most results are in favor of the number fluctuation theory.

We know the quality of the buried oxide is unfavorable in comparison to front gate oxide, and the aim of the present work is to study the impact of BOX trap density on the flicker noise characteristics in SOI MOSFETs. This work will help in evaluating the influence of BOX quality on the noise performance of SOI based circuits. Section A discusses the physical model and section B presents the analytic model, devised to account for the impact of BOX trap density on flicker noise of FDSOI MOSFET.

II.1 Physical Model

Flicker noise occurs due to fluctuations in the drain current of the SOI MOSFET, whether fully or partially depleted [9, 10]. These fluctuations are due to trapping and de-trapping of free carriers into traps located in the oxide near to the interface [11]. The noise is strongly influenced by the surface electric field or equivalently**,** the fraction of the charge carriers (holes/electrons) concentration lying close to the interface [4]. Thus flicker noise can be expressed in terms of the fluctuations in the charge carrier concentration near to the interface.

The flicker noise has been more often studied in relation to kink for PDSOI MOSFETs [12, 13, and 14]. FDSOI has been considered to be free of visible kink effect, and because of its advantages with regard to short-channel effects it is potentially competitive with bulk MOSFET [15]. The exclusive study of flicker noise for FDSOI has not been reported yet. Therefore, this study focuses on the influence of buried oxide trap density on the flicker noise in FDSOI MOSFETs**.**

In FDSOI there is strong coupling between the front and buried oxide interface and this can lead to fluctuations in the electron concentration near to the front interface due to trapping and de-trapping of holes in the traps in the buried oxide. The coupling between the front and back interface takes place through different capacitive components as shown in Fig.1 which forms the physical model. The trapping of holes at the buried oxide interface give rise to buried oxide trap capacitance which in-turn changes the depletion capacitance itself and this change is then reflected as change in the flat band voltage of the front gate. In section B this model is expressed analytically.

II.2 Analytic Model (quantitative)

In case of Fully Depleted SOI MOSFET there is capacitive coupling between the front and the back gate oxide and the way these capacitive components are coupled is shown in Fig. 1.

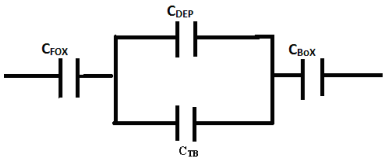

Fig. 1: Capacitive coupling between front and BOX in fully depleted SOI MOSFET

As observed in Fig. 1 the total capacitance, C_{TOTAL} is given as:

$$C_{TOTAL} = \frac{C_{DEP} + C_{TB}}{1 + \left(\frac{1}{C_{BOX}} + \frac{1}{C_{FOX}}\right)(C_{DEP} + C_{TB})} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots (1)$$

with

C_{FOX} for front gate oxide capacitance

C_{BOX} for furied oxide capacitance

C_{DEP} for depletion capacitance

C_{TB} for buried oxide trap capacitance.

C_{FOX}, C_{BOX}, and C_{DEP} have been calculated by using the conventional formulas, whereas C_{TB} is formed due to the capture and emission of hole carriers into the traps located in the buried oxide interface calculated as follows [16]:

$$C_{TB} = \frac{q^2}{kT} N_{TB} f_T (1 - f_T) \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots (2)$$

where

q is the charge on the carrier

k is the Boltzmann constant

T is the temperature in Kelvin

N_{TB} is the *t*rap density at the buried oxide interface

f_T is the *t*rap occupancy function.

Buried oxide trap capacitance has been formed due to trapping of holes in the traps present at the buried oxide interface. The fluctuations in this trapped charge produces fluctuations in the flat band voltage at the front gate as there is coupling between the front and back in case of FD SOI MOSFET. This fluctuation in the flat band voltage is expressed as [17]:

$$\delta V_{FB} = -\left[\frac{\delta Q_{TB}}{WLC_{TOTAL}}\right]\frac{x_0}{t_{BOX}} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots (3)$$

where

δQ_{TB} represents the fluctuations in the trapped charge at the buried oxide interface

x_0 represents the distance from the buried oxide interface at which traps are present

t_{BOX} is the buried oxide thickness.

These fluctuations in the flat band voltage due to fluctuations in the buried oxide trapped charge induce fluctuations in the drain current which are expressed as:

$$\frac{\delta I_D}{I_D} = -\left[\frac{1}{V_{FB}}\frac{\delta V_{FB}}{\delta Q_{TB}}\right]\delta Q_{TB} \ \ldots\ldots\ldots\ldots\ldots\ldots \quad (4).$$

Using equation (3) we have,

$$\frac{\delta V_{FB}}{\delta Q_{TB}} = -\frac{1}{WLC_{TOTAL}}\frac{x_0}{t_{BOX}} \ \ldots\ldots\ldots\ldots\ldots\ldots \quad (5).$$

Substituting equation (5) in equation (4) we have,

$$\frac{\delta I_D}{\delta Q_{TB}} = \frac{I_D}{V_{FB}}\frac{x_0}{WLC_{TOTAL}t_{BOX}} \ \ldots\ldots\ldots\ldots\ldots\ldots \quad (6).$$

As the power of the signal is obtained by integrating its power spectral density to the power spectral density of the fluctuating drain current due to fluctuating trapped charge is given as:

$$S_{I_D} = \left(\frac{\delta I_D}{\delta Q_{TB}}\right)^2 S_{Q_{TB}} \ \ldots\ldots\ldots\ldots\ldots \quad (7)$$

$S_{Q_{TB}}$ is the power spectral density of the fluctuating trapped charge at the buried oxide interface.

The fluctuations in the buried oxide trapped charge are proportional to the fluctuations in the number of occupied traps at the same interface. Mathematically it is expressed as:

$$S_{Q_{TB}} = q^2 S_{N_{TB}} \ \ldots\ldots\ldots\ldots\ldots\ldots \quad (8)$$

where $S_{N_{TB}}$ = Fluctuations in the number of occupied traps at the buried oxide interface, and q= Electronic charge

The fluctuations in the number of occupied traps depends on the trapping and de-trapping time, probability that trap will be occupied and trap density at the interface. These fluctuations in the number of occupied traps over the total area and energy are expressed as:

$$S_{\Delta N_{TB}}(y,f) = \int_0^L \int_{E_V}^{E_C} \int_0^W \int_0^{t_{BOX}} \{4N_{TB}(E,x,y,z)\Delta y f_T(1-f_T)\} \left\{\frac{\tau_T(E,x,y,z)}{1+\omega^2\tau_T^2(E,x,y,z)}\right\} dx dy dz dE \quad \ldots (9)$$

where trap occupancy function

$$f_T = \left[1+\exp\left((E_{Fp}-E_T)/kT\right)\right]^{-1} \ \ldots\ldots\ldots (10).$$

For trap occupancy function the degeneracy is taken to be equal to 1 as only single trap level is assumed.

Here E_{Fp} is the hole quasi Fermi level, L the channel length, and $f_T(1\text{-}f_T)$ is the delta function about the hole quasi Fermi level and reflects that only traps near to this Fermi level contribute to noise or fluctuations. Also $1\text{-}f_T$ corresponds to trapping function and f_T corresponds to the de-trapping function for electron and vice versa for hole trapping and de-trapping.

Simplifying equation (9), we have

$$S_{\Delta N_{TB}}(f) = \mathrm{N_{TB}}(\mathrm{E_{Fp}})\frac{kTWL}{\alpha f} \ \ldots\ldots\ldots\ldots\ldots\ldots \quad (11)$$

where, α is the attenuation coefficient of the electron wave in the oxide, and is given as:

$$\alpha = \left[2m_h^*\varphi_B/\hbar\right]^{1/2} \ \ldots\ldots\ldots\ldots\ldots\ldots \quad (12)$$

with

m_h^* the effective mass of a hole, and $N_{TB}(E_{Fp})$ is the trap density at the buried oxide interface, W the width of the SOI MOSFET, f the frequency of operation, and φ_B the oxide barrier tunneling height.

Using equation (8) and (11), the fluctuations in the buried oxide trapped charge are expressed as:

$$S_{Q_{TB}} = q^2 kTWL(\alpha f)^{-1}\,\mathrm{N_{TB}}(\mathrm{E_{Fp}}) \ \ldots\ldots\ldots\ldots\ldots \quad (13).$$

Using equation (7) and (13), the fluctuations in the drain current due to fluctuations in the front gate flat band voltage which are further due to fluctuations in the buried oxide trapped charge are given as:

$$S_{I_D} = \left(\frac{I_D}{V_{FB}}\frac{x_0}{WLC_{TOTAL}t_{BOX}}\right)^2 \mathrm{S_{Q_{TB}}} \ \ldots\ldots\ldots\ldots\ldots \quad (14)$$

$$\frac{I_D}{V_{FB}} = \frac{I_D}{V_{GS}} = g_m \ \ldots\ldots\ldots\ldots\ldots \quad (15)$$

and transconductance

$$g_m = \left(2I_D\mu WC_{FOX}/L\right)^{1/2} \ \ldots\ldots\ldots\ldots\ldots\ldots \quad (16)$$

$$S_{I_D} = \frac{kT}{WL\alpha f}\left(\frac{qg_m x_0}{C_{TOTAL}t_{BOX}}\right)^2 \mathrm{N_{TB}}(\mathrm{E_{Fp}}) \ \ldots\ldots\ldots\ldots\ldots\ldots \quad (17).$$

Equation (17) represents the drain current fluctuations due to fluctuations in the trapped charge at the buried oxide interface. Further this equation is valid only when there is coupling between the front gate oxide and the buried gate oxide that is for fully depleted SOI MOSFETs.

III. SIMUALTIONS

The model developed in Section III signifies the influence of BOX trap density or the quality of buried oxide on the flicker noise in Fully Depleted SOI MOSFETs. The model was validated, by simulating a typical SOI structure. A prototype device was chosen for model validation. The device design parameters were Channel length is 250 nm, oxide thickness is 3.9 nm, silicon film thickness is 35 nm, and buried oxide thickness was 120 nm. The simulation was carried out for buried oxide trap density of 1E+16 /cm^{3}eV,

1E+18/cm^{3}eV, and 1E+21/cm^{3}eV. The simulations were carried out on a device simulator [19].

We have to assure and verify that the device is FD; it should be free of visible kink. Fig.2 shows the output characteristics of the device. The 35 nm does not show sudden rise in current as there is no visible kink. This proves the fully depleted nature of the device under consideration.

Fig. 2 shows the fluctuations in the drain current with the trap density at the BOX. This figure indicates that there is decrease in the drain current with increase in the trap density of the BOX and these drain current fluctuations are related to flicker noise. This decrease in the drain current is validated by decreases in the electron concentration at the front interface as shown in Fig. 3.

The decrease in the electron concentration and in-turn drain current is due to the change in the gate capacitance as the trap density at the BOX changes as shown in Fig. 4. Fig. 4 indicates there is change in the flat band voltage of the front gate due to change in the depletion capacitance which in-turn is due to the trap capacitance formed in the BOX due to trapping and de-trapping of holes at the BOX. Fig. 5 shows the dependence of the gate capacitance on the thickness of the BOX. This figure indicates small dependence of the flat band voltage of front gate on the BOX thickness.

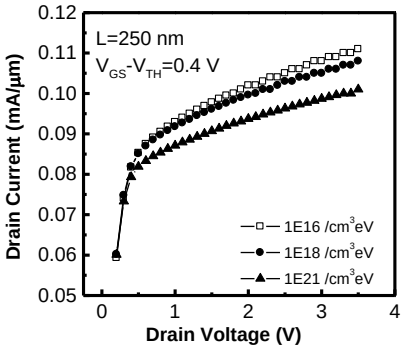

Fig. 2: Dependence of drain current on the trap density at the buried oxide interface for channel length of 250.

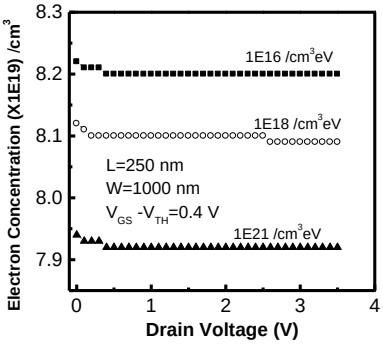

Fig. 3: Variations of electron concentration at the front interface due to the trap density at the BoX for channel length of 250 nm.

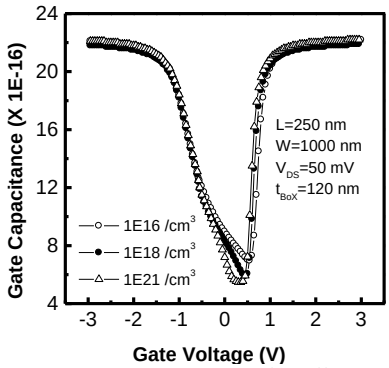

Fig. 4: Fluctuations in the gate capacitance for different trap density at the buried oxide interface for channel length of 250 nm and buried oxide thickness of 120 nm.

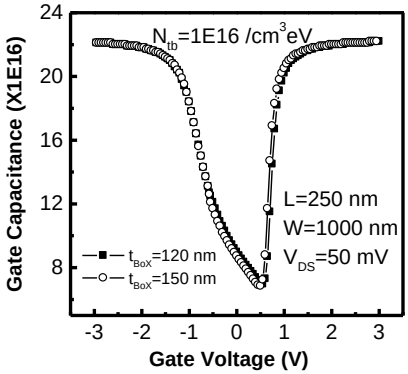

Fig. 5: Dependence of gate capacitance on the buried oxide thickness for buried oxide trap density of 1E16 /cm^{3}eV and channel length of 250 nm.

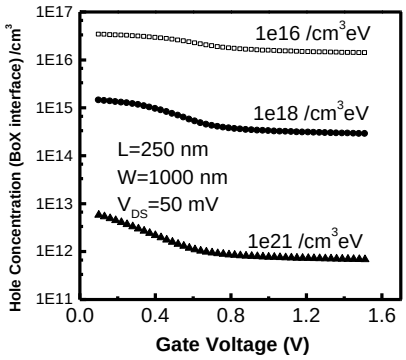

Fig. 6: Dependence of hole concentration at the buried oxide interface on the buried oxide trap density for channel length of 250 nm.

Fig. 6 shows the fluctuations in the hole concentration at the BOX with the trap density at the BoX. This figure indicates hole concentration at the BOX decreases with increase in trap density at the BoX and is due to capture of holes by the traps which in-turn is responsible for the formation of trap capacitance. Fig. 7 shows the fluctuations in the depletion charge with the trap density at the BOX. This figure indicates that the depletion charge changes with the trap density at the BOX interface and this in-turn changes the depletion capacitance which in-turn is reflected as fluctuations in the drain current and these fluctuations corresponds to flicker noise.

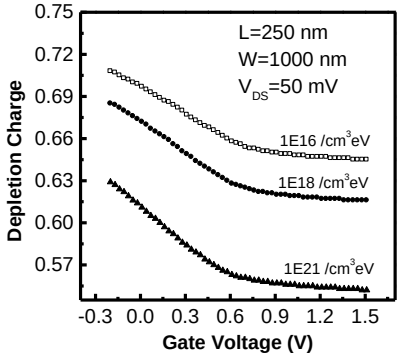

Fig. 7: Fluctuations in the depletion charge for different trap densities in the buried oxide and buried oxide thickness of 120 nm.

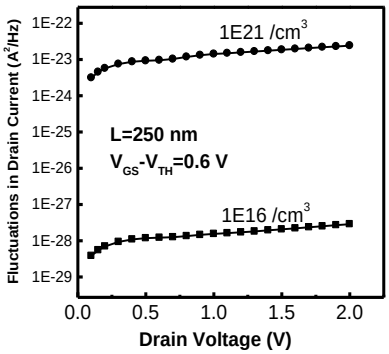

Fig. 8: Dependence of fluctuations in the drain on the Trap densities at the buried oxide interface and drain to source voltage.

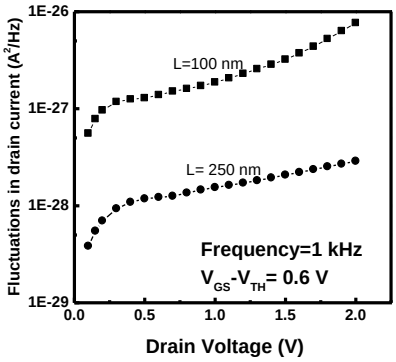

Fig. 9: Dependence of fluctuations in the drain current on channel length and drain to source voltage.

Model equation (13) developed by us has been plotted using the parameter values extracted from the device simulator. These plots are shown in Fig. 8 and Fig. 9 represents the fluctuations in the drain current for different trap densities at the BoX and for different channel lengths. As can be observed the fluctuations in the drain current increases with increase in the buried oxide trap density and decreases with increase in the channel length and this is in accordance with equation (13) of the model developed by us.

IV. CONCLUSION

The results signify that the modeling of flicker noise is not restricted only to the front interface; the back interface must also be taken into account. Flicker noise is now becoming a major concern when using SOI at RF. Therefore modeling the flicker noise with relation to each and every dimension is essential. This work is just a modest attempt towards the understanding of the influence of buried oxide thickness on the flicker noise in fully depleted SOI MOSFETs. There is a need to focus on the implementation of more accurate noise models for SOI. This will help in evaluating the performance of SOI based circuit in a much better way and take advantage of the potential of SOI in the present technology scenario.

References

[1] Jean Pierre Colinge, "Silicon-on-Insulator Technology: Materials to VLSI", 2nd Edition, Kluwer Academic Publishers, Boston, (1997).

[2] J. Jomaah and F. Balestra "Low frequency noise in advanced CMOS/SOI devices", IEE Proceedings Circuits Devices System, **151**, 111-117 (2004).

[3] T. Elewa, B. Boukriss, A. Chovet and S. Cristoloveanu, "Low Frequency Noise Spectroscopy in Thin SIMOX MOS Transistors**",** IEEE SOI Conference, Key West Florida, (1990), pp 103-104.

[4] Jen-Tai-Hsu, Janet Wang, Jason WOO, C.R. Viswanathan, "Flicker noise in thin film fully depleted SOI MOSFETs", IEEE SOI Conference, Rohnert Park, California, (1991), pp 30-31.

[5] J. Babcock, D. K. Schroder, and Y. Tseng, "Low-Frequency Noise in Near-FD TFSOI MOSFET's," IEEE EDL, **19**, 40- 43 (1998)

[6] Dieudonne, F., et al, "A comparative approach of low frequency noise in 0.25 and 0.12 µm Partially and FD SOI N-MOSFETs" IEEE International SOI conference, Virginia (2002) pp 105-106.

[7] H. D. Xiong, et al, "Charge trapping and low frequency noise in SOI buried oxides," IEEE TNucSc, **51**, 3238–3242 (2004).

[8] Tae-Young Oh, "AC and noise analysis of deep-submicron MOSFETs," Ph. D. Thesis, Stanford University, February (2004).

[9] T. Ytterdal, Y. Cheng, T. A. Fjeldly, "Device Modeling for Analog and RF CMOS Circuit Design", John Wiley & Sons, Ltd, (2003).

[10] Wei Jin, Philip C. H. Chan, Samuel K. H. Fung and Ping K. Ko, "Shot-noise Induced excess low frequency noise in floating body partially depleted SOI MOSFETs", IEEE TED, **46**, 1180-1185 (1999).

[11] Martin von Haartman Stockholm, Sweden, "Low-frequency noise characterization, evaluation and modeling of advanced Si- and SiGe-based CMOS transistors", KTH, School of Information and Communication Technology, IMIT Doctoral Thesis, Stockholm, Sweden, (2006).

[12] E. Simoen, et al, "The Kink-Related Excess Low-frequency Noise in Silicon-on-Insulator MOSFET's", IEEE TED, **41**, 330-339 (1994).

[13] Jian Chen, et al, "Noise overshoot at drain current kink in SOI MOSFET", IEEE International SOI conference, Key West, Florida, (1990), pp.40-41..

[14] N. Zamdmer et al," Suitability of Scaled SOI CMOS for high-frequency Analog Circuits," Proceedings of IEEE 32nd ESSDEC, Firenze, Italy (2002), pp 511-514.

[15] Jin-Young Choi, and Jerry G. Fossum, "Analysis and control of floating-body bipolar effects in fully depleted sub micrometer SOI MOSFETs," IEEE TED, **38**, 1384-1391 (1991).

[16] E. H. Nicillian and J. R. Brews, "MOS Physics and Technology," John Wiley & Sons, (1982)

[17] Narain Arora, "MOSFET modeling for VLSI simulations Theory and practice", World Scientific Publishing Company, (2007)

[18] Silvaco TCAD, ATLAS device simulation framework (2006)