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EXPLICIT TIMING ANALYSIS OF DISCONTINUOUS RC GLOBAL VLSI INTERCONNECT LINES UNDER RAMP INPUT

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Abstract In this paper, discontinuous interconnect lines are modelled and analyzed as a cascaded line composed of many uniform interconnect lines. The system transfer functions of respective uniform interconnect lines are determined, followed by its time domain response. Since the time domain response expression is a transcendental form, the waveform expression is reconfigured as an approximated linear expression. The proposed model has less than 5% error in the delay estimation.
Keywords: VLSI Interconnect Modelling, RC Interconnects, Ramp Input, Timing Analysis.

I. INTRODUCTION

Interconnect delay, coupling and crosstalk are important in realizing recent high-performance VLSI's and will become increasingly important as the feature size of the lines is miniaturised and the line length is increased. Thus, signal integrity of the interconnect lines has to be verified in the early stage of circuit design. The problem of wire sizing has not received very much attention until recently. Cong et al. presented some work in the area in [1, 2]. The approach in [1] used a delay model based on an upper bound [3] on the Elmore delay, and minimized the delay of the interconnect under minimum and maximum wire width constraints. This was extended in [2], where the Elmore delay was directly used to perform the timing optimization.

In practical integrated circuits, most of interconnect lines is neither simple uniform nor isolated straight lines but discontinuous lines. That is, the characteristic impedance of the line of the interest may be changed during the signal propagation from a source to a destination because of neighbour lines. Physically, while signal paths near circuit blocks may have narrow routing spaces, the other area may be more enough routing space. Consequently, a signal path may have different line width for suitable layouts. Alternatively, many of the signal lines may be complicatedly coupled with neighbour lines in parts. As an example, an interconnect line from a circuit block to another circuit lock may be coupled in a part as shown in Fig. 1.

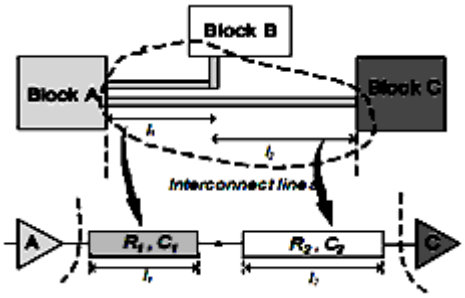

Fig.1: Coupled Transmission Lines

In such case, the signal transient of the line may be significantly affected by neighbour line switching. That means a part of the line may have different characteristics with the remaining part of the line. Thus, existing simple timing models that assume a uniform straight line may not be accurate enough as shown in Fig. 2.

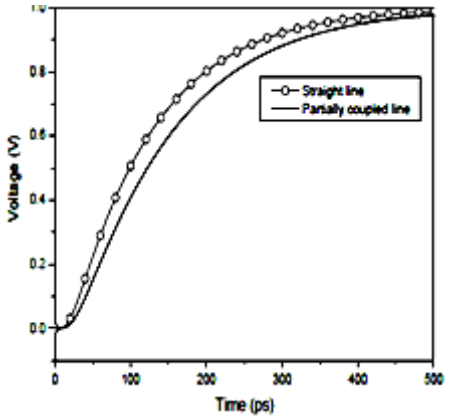

Fig.2: Signal Transient for the interconnect line between the Blocks A and C for fig 1.

In reality, although such complicated line can be accurately evaluated with SPICE simulation, it may not be suitable for the timing verification of practical circuits which has myriad interconnect nets. Thus, a much simpler timing model for such lines is highly required to be incorporated into various circuit design CAD tools. In order to readily determine the delay time of discontinuous lines, previously moment-matching technique have been employed. Although they reduce computation time and guarantee accuracy,

recursive moment calculations may significantly increase computation time since the number of RC segments is increased with technology scaling. Bhavnagarwala et al. [11] derived a simple timing model for tree structure like discontinuous lines. But the results are not so accurate as verified with today's high performance integrated circuits. Taehoon Kim [12] gave the improved results of the timing analysis of discontinuous interconnect using the step input.

In this paper, discontinuous interconnect are modelled as a cascaded line composed of many uniform interconnect lines taking input function as a Ramp.

II. TIME DOMAIN RESPONSE OF DISCONTINUOUS INTERCONNECT LINE

II. 1. System Function of RC Interconnect Line

Assuming one dominant pole, a ramp input response for an RC interconnect line for the fig. 3 can be represented as

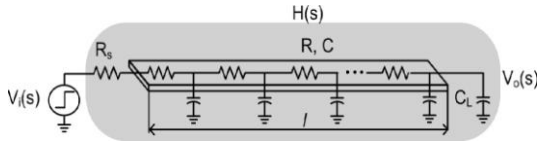

Fig: 3. An RC interconnect line

$$v_o(t) = 1 + K(t + \exp(-t/\tau)) \quad (1)$$

Where,

$$K = -1.01^{(R_T + C_T + 1)/(R_T + C_T + \pi/4)}$$

$$\tau = RC^{(R_T C_T + R_T + C_T + (2/\pi)^2)/1.04}$$

$$R_T = R_S/R, C_T = C_L/C \quad (2)$$

R(C) is the total resistance (capacitance) of the line. It can be represented with R=Ru.L (C=Cu.L), where Ru and Cu are per-unit length (PUL)-resistance and PUL-capacitance, respectively and L is the length of the line. Since the frequency domain response of (1) becomes

$$V_0(s) = \frac{1}{s^2}\frac{\tau(1+K)s+1}{\tau s+1} \quad (3)$$

The system function of the line can be regarded as

$$H(s) = \frac{\tau(1+K)s+1}{\tau s+1} = H'(s) + (1+K)H''(s) \quad (4)$$

Where

$$H'(s) = \frac{1}{\tau s+1} \text{ and } H''(s) = \frac{\tau s}{\tau s+1} \quad (5)$$

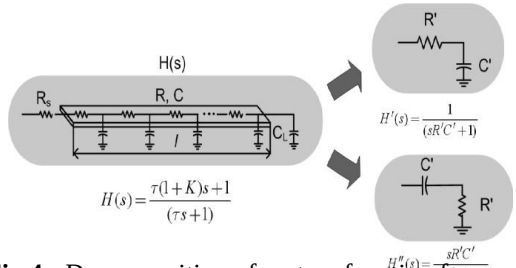

Fig 4: Decomposition of system function for an interconnect line

Thus in this manner the system function is decomposed into function of distributed RC interconnect as shown in Fig 4.

In distributed RC line, the effective time constant is much smaller than that of the lumped model. Thus, defining R′ as the total resistance of the system, C′ can be determined as

$$R' \equiv R_s + R = R(R_T + 1)$$

$$C' \equiv \tau/R' \quad (6)$$

Thus, since the time constant becomes

$$\tau = R'C' \quad (7)$$

H'(s) and H''(s) can be rewritten as

$$H'(s) = \frac{1}{sR'C' + 1} \quad \text{and} \quad H''(s) = \frac{sR'C'}{sR'C' + 1} \quad (8)$$

Therefore, (4) can be represented with the combination of two equivalent circuits as shown in Fig. 4.

II. 2. Time domain response at intermediate node

A discontinuous line can be represented with distributed circuit model as shown in Fig. 5 (a). Since the line is discontinuous, a system function needs to be determined in the discontinuous node (e.g., node-1). Note, unlike the circuit of Fig. 3 that has the lumped capacitance load, the intermediate node (i.e., the node-1) of the circuit of Fig. 5(a) has the interconnect line as a load. Thus, (4) has to be modified a bit.

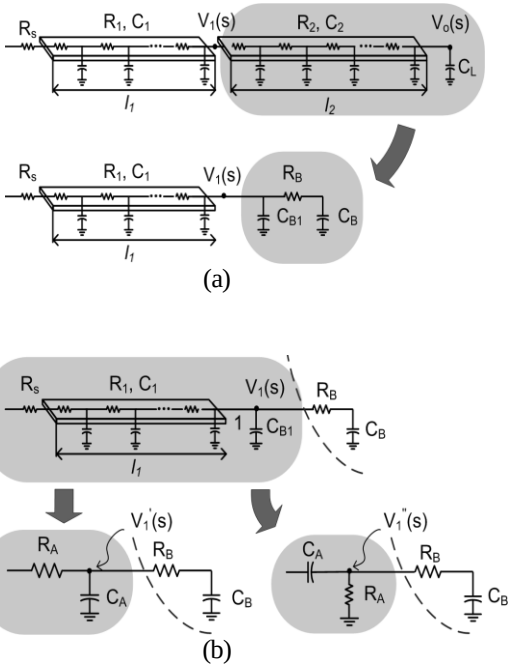

Fig 5: The model simplification of an interconnect chain.: (a) Circuit model of cascaded interconnects and driving point admittance approximation for the second line. (b) Decomposition of the first line.

In order to determine the system function of the node-1, the driving point impedance of the right hand side of the node is represented with an approximated lumped

circuit as shown in Fig. 5 (a) [14]. Defining the input admittance at the node-1 as $Y_1(s)$, $Y_1(s)$ can be represented by its Taylor series expansion around s=0:

$$Y_i(s) = \sum_{n=1}^{\infty} y_n s^n = y_1 s + y_2 s^2 + y_3 s^3 + \ldots \quad (9)$$

Where y_n is the moment of the admittance for node-1. Then, the lumped circuit model parameters can be determined as

$$R_B = \frac{-y_3^2}{y_2^3}, C_B = \frac{y_2^2}{y_3}, C_{B1} = y_1 - \frac{y_2^2}{y_3} \quad (10)$$

Regarding C_{B1} , as the load of the left-hand side line of the node-1, the discontinuous line can be represented as in Fig. 5 (b). Note that R_A and C_A can be determined by using the similar technique as in determining R′ and C ′

$$R_A \equiv R_s + R_1 = R_1(R_{T1} + 1), C_A \equiv \tau_1 / R_A \quad (11)$$

Since the circuit of Fig. 5 (b) is similar to that of Fig. 4, combining (4) with (8), the transfer function of the left hand-side line can be represented as

$$H_1(s) \approx H_1'(s) + (1 + K_1) H_1''(s) \quad (12)$$

with

$$H_1'(s) = \frac{1 + sR_B C_B}{1 + s[R_A(C_A + C_B) + R_B C_B] + s^2 R_A R_B C_A C_B}$$

$$H_1''(s) = \frac{sR_A C_A(1 + sR_B C_B)}{1 + s[R_A(C_A + C_B) + R_B C_B] + s^2 R_A R_B C_A C_B} .$$

Thus, $V_1(s)$ becomes

$$V_1(s) = \frac{1}{s^2} H_1(s) = \frac{1}{R_A R_B C_A C_B} \frac{(1 + sR_B C_B)[1 + sR_A C_A(1 + K_1)]}{s^2(s - p_1)(s - p_2)} \quad (13)$$

with

$$p_{1,2} = \frac{-b \pm \sqrt{b^2 - 4a}}{2a}$$

$$a = R_A R_B C_A C_B, b = R_A(C_A + C_B) + R_B C_B$$

Thus, the time domain counterpart is

$$v(t) = A + Bt + Ce^{p_1 t} + De^{p_2 t} \quad (14)$$

with

$$A = \frac{1}{ap_1 p_2}\left[R_B C_B + R_A C_A(1 + K_1) + \frac{(p_1 + p_2)}{p_1 p_2}\right]$$

$$B = \frac{1}{ap_1 p_2}$$

$$C = \frac{1}{ap_1 p_2(p_1 - p_2)}\left\{p_1 p_2(1 + K_1) - 1 + p_2\left[R_B C_B + R_A C_A(1 + K_1) - \frac{(p_1 + p_2)}{p_1 p_2}\right]\right\}$$

$$D = -(A + C) .$$

II. 3. Time Domain response at output node

Since $H_1(s)$ was determined, only if $H_2(s)$ is known, the response of the discontinuous line $V_0(s)$ can be readily determined from the circuit of Fig. 5 (a),

$$V_o(s) = \frac{1}{s^2}[H_1'(s) + (1 + K_1) H_1''(s)] H_2(s) \quad (15)$$

Since the circuit of Fig. 5 (b) is similar to that of Fig. 4, from (1) and (4), $H_2(s)$ can be determined follows

$$H_2(s) = \frac{\tau_2(1 + K_2)s + 1}{\tau_2 s + 1} \quad (16)$$

Thus, from (12), (15), and (16), $V_o(s)$ becomes

$$V_o(s) = \frac{1}{R_A R_B C_A C_B} \frac{(1 + sR_B C_B)[1 + sR_A C_A(1 + K_1)]}{s^2(s - p_1)(s - p_2)} \cdot \frac{\tau_2(1 + K_2)s + 1}{\tau_2 s + 1} \quad (17)$$

The time domain response becomes

$$v_o(t) = A_1 + B_1 t + C_1 e^{p_1 t} + D_1 e^{p_2 t} + E_1 e^{p_3 t} \quad (18)$$

with

$$p_3 = -\frac{1}{\tau_2}$$

$$A_1 = \frac{\tau_2}{ap_1 p_2}[R_A C_A(1 + K_1) + R_B C_B + \frac{(p_1 + p_2)}{p_1 p_2} - \frac{K_2}{p_3}]$$

$$B_1 = \frac{\tau_2}{ap_1 p_2}$$

$$C_1 = \frac{(p_3 - p_2)(F - Gp_1)}{p_1^2(p_3 - p_2) + p_2^2(p_3 - p_1) + p_3^2(p_2 - p_1)}$$

$$D_1 = \frac{(p_1 - p_3)(F - Gp_2)}{p_1^2(p_3 - p_2) + p_2^2(p_3 - p_1) + p_3^2(p_2 - p_1)}$$

$$E_1 = \frac{(p_2 - p_1)(F - Gp_3)}{p_1^2(p_3 - p_2) + p_2^2(p_3 - p_1) + p_3^2(p_2 - p_1)}$$

and

$$F = \frac{1}{a}\{[R_B C_B + R_A C_A(1 + K_1)][\tau_2(1 + K_2)] + R_A R_B C_A C_B(1 + K_1)\}$$

$$- A(p_1 p_2 + p_2 p_3 + p_3 p_1) + B(p_1 + p_2 + p_3)$$

$$G = B - \frac{1}{a}[\tau_2 R_A R_B C_A C_B(1 + K_1)(1 + K_2)] - A(p_1 + p_2 + p_3) .$$

The above equations (14) and (18) are the proposed closed form expression for the time domain response of the interconnect lines at both intermediate and output node under ramp input excitation.

III. SIMULATION RESULTS

The configuration of circuit for simulation is shown in figure 3. The distributed parameters are given in the table1. We use 180 nm standard cell libraries [13]. Other parameters such as R_S, C_L and the length of the interconnect (L) are subject to change.

Table1: RC Parameters for 180nm Technology.

Parameter(s)	Value/m
Resistance(R)	120 kΩ/m
Capacitance(C)	240 pF/m

The voltage at each node of the circuit is computed using (14) and (18) and compared with SPICE simulation for different value of C. As shown in figure 6 and figure 7, our model is able to capture the voltage at any node along the interconnect circuit.

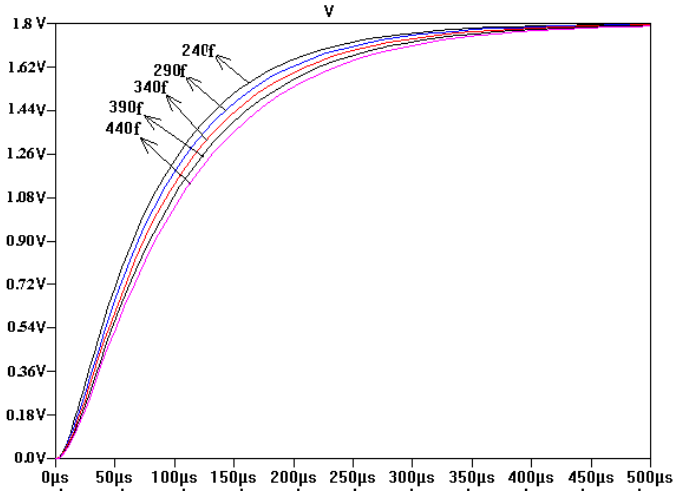

Fig 6: Voltage Profile obtained for output Node

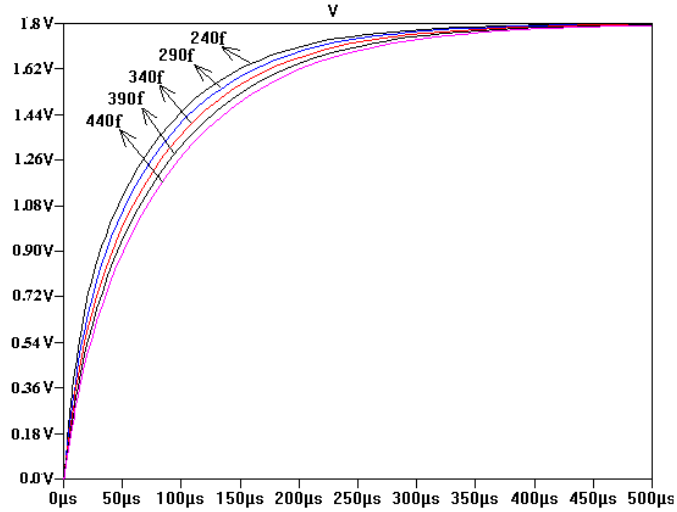

Fig 7: Voltage Profile obtained for Intermediate Node

Table2: Comparison of Results with those of SPICE values for intermediate node

S.N.	R_S (KΩ)	C_L(fF)	SPICE Value (V)	Proposed Value (V)
1	1	10	0.2391	0.2123
2	2	50	0.4567	0.5628
3	5	750	0.8353	0.8976
4	10	1000	1.0810	0.9986
5	50	1500	1.2716	1.2517
6	100	1500	1.4335	1.4176

The comparative result of the proposed models for output node as well as arbitrary node with SPICE values and proposed values for the different values of C is illustrated in Tables 2 and Table 3 respectively. From the tables, it is evident that the proposed models for both cases results in an error of as low as 5% when compared with that of SPICE simulations.

Table 3: Comparision of Result with those of SPICE values for Output node

S. N.	R_S (KΩ)	C_L(fF)	SPICE Value (V)	Proposed Value (V)
1	1	10	0.1867	0.1680
2	2	50	0.3854	0.3923
3	5	750	0.7153	0.7948
4	10	1000	0.9884	0.9597
5	50	1500	1.1534	1.1265
6	100	1500	1.2876	1.3153

IV. CONCLUSION

Interconnect now dominates a number of design metrics. Various interconnect models have been presented over the last several decades. In this work, an accurate voltage profile for discontinued RC interconnect is presented, that computes the voltage to any arbitrary point on the waveform at any point along the interconnect. It is based on the first three moments of the impulse response. Proposed model is applicable to any type of interconnect as this approach is not based on the analogy of the impulse response to a particular Probability Distribution Function (PDF). Verification with measurement data from various test structures demonstrates the validity of this model. Since all elements are frequency independent, it is fully compatible with transient analysis and wide-band design.

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