Journal of Electron Devices, Vol. 15, 2012, pp. 1282-1284

© JED [ISSN: 1682 -3427]

Journal of Electron Devices
www.jeldev.org

DRIVING CURRENT IMPROVEMENT BY $\delta_N^{\ +}$ LAYER IN P-CHANNEL TUNNEL FIELD EFFECT TRANSISTOR

Apurba Chakraborty, P. N. Kondekar
Electronics and Communication Department, PDPM IIITDM-Jabalpur, Pin-482005 India.
apurba.chakraborty86@gmail.com

Received 5-09-2012, online 21-09-2012

ABSTRACT

Tunnel Field Effect Transistor (TFET) is considered as alternative Nano scale device for future technology. In this paper we have shown that a $\delta_N^{\ +}$ layer between the drain and channel region can raise driving current by two order of magnitude in p channel operation compare to simple TFET device structure. This highly doped layer creates the peak electric field notch at the drain-channel junction and increases the tunneling current at that junction as the band to band tunneling is exponential function of electric field. The on-current recorded as 55 μA/μm for the modified silicon TFET device in the p-channel operation at V_{GS}= -1.4 V and V_{DS} = 0.3 V. The average subthreshold swing as low as 56 mv/dec is recorded and an improved point slope of 28 mv/dec is calculated. Also the I_{ON}/I_{OFF} current ratio is increased approximately by three orders of magnitude compare to normal silicon TFET device structure.

Keywords : Double gate Tunnel field effect transistor (DGTFET), band to band tunneling tunneling (BTBT) .

I. INTRODUCTION

Tunnel field effect transistor is one of the promising candidates for low power and high speed application due to its immune to low subthreshold swing and high I_{ON}/I_{OFF} current ratio. But low driving current of TFET is the main obstacle in the way of commercialization. To improve the drive current many structures like duel high-K spacer TFET, double gate material structure and hetero gate material structure has been studied [1-3]. But all the study has been done to improve the n-channel characteristic of TFET.

Here we have proposed a modified structure of Double gate TFET (DGTFET) with highly n type doped $\delta_N^{\ +}$ layer between the drain and channel region and by simulation approach is shown that this structure can give best p channel operation of silicon DGTFET. We compared the results with a conventional DGTFET structure without $\delta_N^{\ +}$ layer.

II. DEVICE STRUCTURE AND SIMULATION MODELS

II.1 Device Structure

The schematic diagram of device structure has been shown in Fig. 1. The length of drain, channel and source region is 200 nm, 50 nm and 200 nm respectively. SiO_2 is used as dielectric and the thickness is 2 nm. A 3 nm thick layer is placed between drain and channel region. Doping of the n type drain, p type source, n type $\delta_N^{\ +}$ layer and intrinsic channel is 10^{19}, 10^{18}, 10^{20} and 10^{14} cm^{-3}respectively. P polysilicon is used as gate electrode and metal is used for drain and source contact.

II.2 Simulation models

MEDICI 2D simulator is used for the simulation of the device. For calculating the band to band tunneling current KANE's band to band tunneling (BTBT) model is used. To consider the high doping profile band gap narrowing model and fermidirect statics are used.

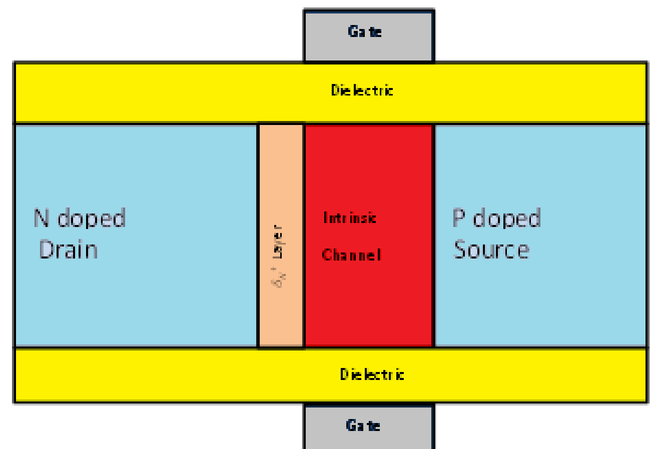

Figure 1: Schematic diagram of Double gate tunnel field effect transistor (DGTFET).

III. SIMULATION RESULTS AND EXPLANATION

III.1 Electric Field Profile and Band Diagram

Electric field profile across the channel near to Si-SiO_2 is shown in Fig. 2. In the figure the comparative profile of DGTFET and DGTFET with $\delta_N{}^+$ is shown.

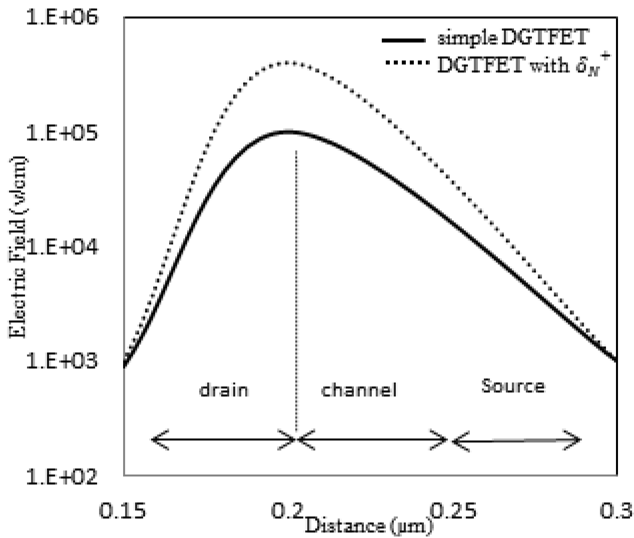

Figure 2: Thermal equilibrium electric field profile near to Si-SiO_2 interface along the channel region.

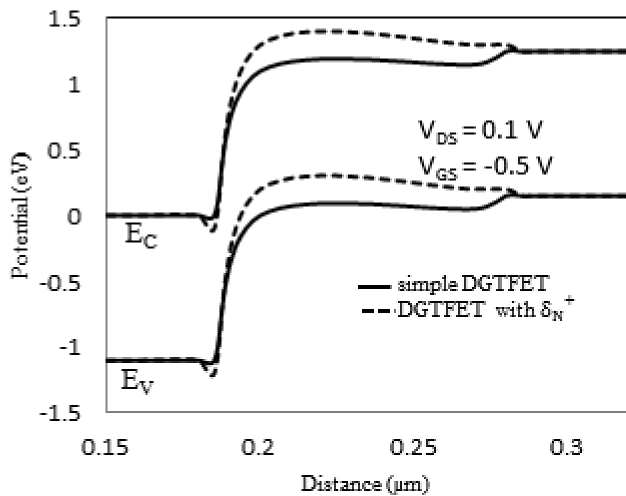

Figure 3: Energy band diagram near to Si-SiO_2 interface for DGTFET and DGTFET with layer. Drain and gate bias remain same for both the device structure.

From the figure we can see that peak electric field at the drain-channel junction is more in DGTFET with $\delta_N{}^+$ compare to simple DGTFET structure. It is known that in p channel DGTFET, electron tunnel from valance band of channel to conduction band of drain region [4]. So to extract more tunneling current it is easier in DGTFET with structure compare to conventional DGTFET, as the tunneling current is a strong function of electric field.From comparative electric field profile, we can say that thermal equilibrium electric field for DGTFET with $\delta_N{}^+$ layer at the channel-drain junction is approximately 5 times larger in magnitude compare to simple DGTFET.

The simulated conduction band (E_C) and valance band (E_V) near to Si-SiO_2 interface of simple DGTFET and DGTFET with $\delta_N{}^+$ for V_{DS} = 0.2 V and V_{GS} = -0.5 V is shown in Fig.3. Here we can see that band banding near to tunneling junction for DGTFET with $\delta_N{}^+$ is more compare to simple DGTFET. Hence tunneling probability is more for DGTFET with $\delta_N{}^+$ structure. Also a notch is created in band diagram for DGTFET with $\delta_N{}^+$ which increases the no of electron can tunnel as electrons see extra vacant space in conduction band.

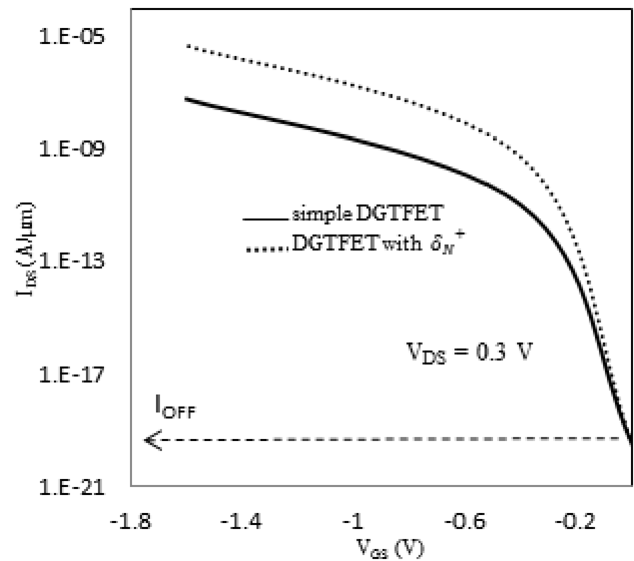

Figure 4: Comparative input characteristic of simple DGTFET and DGTFET with layer for same V_{DS}= 0.3 V. Off current is labeled in the plot.

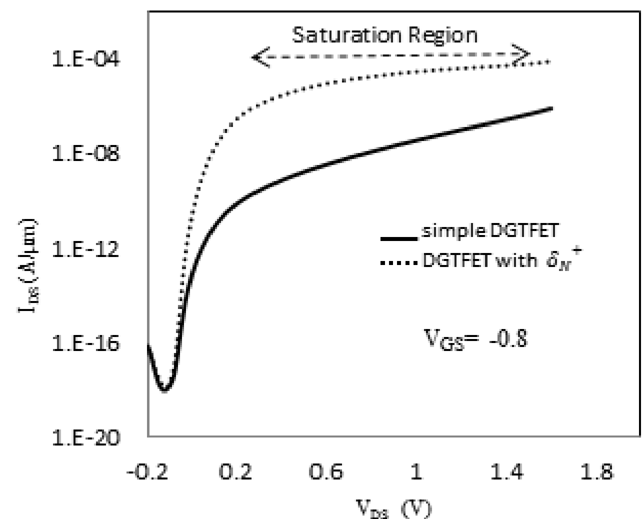

Figure 5: Output characteristics are compared between DGTFET and modified DGTFET.

III.2 Input-Output Characteristic.

Input characteristic of DGTFET with $\delta_N{}^+$ layer and conventional DGTFET are compared in Fig. 4. From the figure we can say tunneling current starts early in DGTFET with $\delta_N{}^+$ layer structure. Off current (I_{OFF}) remains same for both the device structure as it is only the reverse biased p-i-n leakage current. We calculated threshold voltage as the level of gate V_{GS} when drain current reaches at 10^{-8} A/ µm. Then from input characteristic we have seen that threshold voltage for DGTFET with $\delta_N{}^+$ layer is -0.7 V whereas that for conventional DGTFET is -1.5 V. The on current I_{ON} at V_{GS}= -1.4 V and V_{DS}= 0.3 V is 55 µA/µm in DGTFET with $\delta_N{}^+$ layer, which is two order higher compare to simple DGTFET and almost satisfying the ITRS requirement for low power devices. The I_{ON}/I_{OFF} current ratio increases from 10^7 to 10^{10}, which will help to increase the response of the device. The point subthreshold swing is defined at any point on the input characteristic with minimum swing value whereas the average subthreshold swing is calculated between the gate voltage tunnel current increases and the threshold voltage [5]. By this definition, we found DGTFET with $\delta_N{}^+$ shows average subthreshold swing as low as 56 mv/dec and a minimum point slope of 28 mv/dec, whereas for simple DGTFET, values are 88mv/dec and 66 mv/dec respectively. So it can be said that device performance parameters are well optimized by using the high doped delta layer.

In the Fig. 5, the comparative output characteristic is shown. It is seen that at the same V_{GS}, DGTFET with $\delta_N{}^+$ layer is driving more drain current than simple DGTFET. It is also seen that DGTFET with $\delta_N{}^+$ layer showing saturation behavior. As the tunneling width at the drain-channel junction is saturated, drain current also saturated and as a result drain bias dependent behavior is not seen.

IV. CONCLUSION

Double gate tunnel field effect transistor with $\delta_N{}^+$ layer can increase the drive current by two order of magnitude compare to conventional DGTFET in p channel operation. Due to high electric field at the tunneling junction the subrhresholdswing has been lowered which helps in high speed device application. So we can say that device performance can be improved by modifying the structure in such a way that more electric field can be generated by less gate bias at the tunneling junctions. Further improvement of driving capability is expected if high dielectric gate and other kind of $\delta_N{}^+$ layer material are used.

References

[1] Woo Young Choi and Woojun Lee, "Hetero-gate-dielectric tunneling field-effect transistors", *IEEE Trans. Electron Devices* **57**, 2317-2320 (2010).

[2] Sneh Saurabh and m. Jagadesh Kumar, "Novel attributes of a dual material nanoscale tunnel field-effect transistor", *IEEE Trans. Electron Devices* **58**, 404-410 (2011).

[3] Hasanali G. Virani, Rama Bhadra rao Adari and Anil Kottantha, "Dual-κ spacer device architecture for the improvement of performance of silicon n-channel tunnel fets", *IEEE Trans. Electron Devices* **57**, 2410-2417 (2010).

[4] Krishna K Bhuwalka, Stefan Sedlmaier, Alexandra Katherina Ludsteck, Carolin Tolkdorf, Joerg schulze and Ignaz Eisele, "Vertical tunnel field effect transistor", *IEEE Trans. Electron Devices* **54**, 279-282 (2004).

[5] Kathy Boucart and Adrian Mihai Ionescu, "Double-gate tunnel FET with High-K gate dielectric", *IEEE Trans. Electron Devices* **54**, 1725-1733 (2007).