Journal of Electron Devices, Vol. 14, 2012, pp. 1186-1189

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Journal of Electron Devices
www.jeldev.org

NEW REALIZATION OF CURRENT COMPARATOR AND ITS APPLICATION AS CURRENT MODE ADC

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Received 12-06-2012, revised 19-06-2012, online 02-07-2012

ABSTRACT

In this paper, two new high speed low power current comparators are proposed. The first comparator uses resistive load amplifiers in gain stage which is modified by including a resistive feedback in the gain stage for better speed. Simulations have been carried out on SPICE using TSMC 0.18um CMOS technology. The results show a resolution of ± 50 nA for both the comparators and an improved delay of 2.68 ns at ±1 μA for second comparator. A 2 bit current mode ADC was designed using the aforementioned comparator and was found to work satisfactorily.

Keywords: current mode; comparators; ADC; resistive feedback; DCCII

I. INTRODUCTION

The current-mode circuits find extensive use in ADCs, VLSI neural networks and other signal processing applications [2] which can be attributed to their potential features like high speed, large bandwidth and lower power consumption [1]. In practice, there are many sensors such as temperature sensors, photo sensors, APS sensors, CMOS sensors [4-6] that provide current signal. The circuits operating in current mode eliminate the need for current to voltage converter for further processing of the signal leading into area reduction. The current comparator is an integral part of the outlined applications and is a limiting component for accuracy, noise and power consumption reasons thus current mode solutions is highly desirable [6]. The basic features of a current comparator are high speed, low input impedance, low power and low supply voltage. A detailed study of the available current comparators shows that these circuits can be categorized as current mirror based [7], Traff based [8-16], active elements based [17-18] and Threshold Inverter Quantisation based [19].

The underlying principle of current mirror based current comparators [7] is amplification of input current difference, using high output resistance current mirrors and representing it in terms of output voltage. However, this high output resistance deteriorates the frequency performance when the inverter stages are added at the output to achieve rail-to-rail slewing and short transition times. These comparators can however be used in the applications where requirement of higher speed is not stringent. The next generation of current comparator are based on Traff's approach [8] and have significant improvement in performance due to feedback which restricts the input node from slewing rail to rail. Many improvements of the Traff based current comparator have been put forth [9-16] in the literature. Active elements such as current conveyor (CCII) [17] and differential current conveyor (DCCII) [18] based structures is yet another class of current comparators which is based on Traff concept [8]. The Traff [8] and subsequent circuits [9-16] accept input current as the difference between the current to be compared and the reference current. Thus, additional circuitry is required to perform the subtraction operation [9-16]. This suggests that the contribution of the current differencing stage in propagation delay and power dissipation is not included. Though a number of comparator circuits are available in the literature the quest for improving the performance parameters of the comparator is ever open.

In this paper, two new high speed low power current comparators current comparator structures are proposed which employ a current differencing stage, a gain stage comprising of resistive load amplifiers and an output stage comprising of CMOS inverters. The suitability of the proposed comparator is tested by designing a 2 bit current mode Flash ADC. The theoretical proposition is validated through SPICE simulations using TSMC 0.18 μm CMOS technology at supply voltage of 1.8V. The paper is organized as follows: Section 2 introduces current comparator concept followed by the detailed description of the proposed architectures and a design application as 2-bit current mode ADC. Section 3 presents the simulation results of the proposed current comparators and 2 bit current mode ADC. Performance parameters of the same

have been calculated. Finally, conclusions are presented in section 4.

II. BASICS OF CURRENT COMPARATOR

Current comparator provides a voltage output by comparing the input current with reference current. The block diagram of the current comparator is depicted in Fig. 1 which comprises of three stages. The first stage is the current difference stage and accepts input current (Iin) and reference current (Iref) and gives current difference (Idiff = Iin - Iref) as output. The gain stage senses the current difference and produces a corresponding amplified voltage. The output stage is used to provide the rail to rail voltage swing. The available current comparators in the literature [7-19] use different implementation in one or more stages (Fig. 1) for achieving better performance such as propagation delay, resolution and power dissipation. In the following section two current comparator structures are proposed.

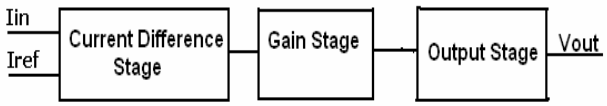

Figure 1. Block diagram of current comparator

II. 1 Proposed Current Comparator I

The proposed current comparator is based on the general scheme shown in Fig. 1. The first stage that is the current difference stage is shown in Fig. 2. It accepts two input currents namely Iin and Iref and uses current mirrors [18] to generate the output difference current, Idiff.

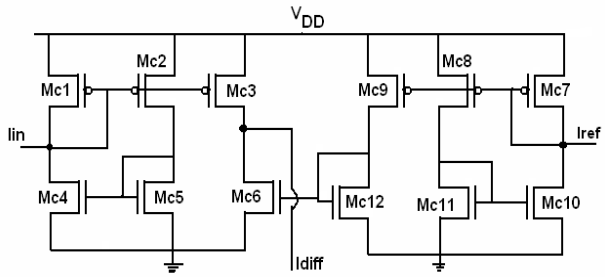

Figure 2. Current Difference stage

The second stage or the gain stage consists of a cascade of two resistive load amplifiers as shown in Fig. 3. The first amplifier senses the input difference current and generates corresponding voltage. This voltage is further amplified by second resistive load amplifier (Mr3-Mr4) of the gain stage. Thus, the gain stage, in total acts as a transimpedance gain stage. Both resistive load amplifiers are designed to operate as Class A amplifier i.e. switching point is kept in the middle of the voltage swing at amplifiers input. Two CMOS inverters are used in the output stage, marked in Fig. 3, to ensure full swing.

II. 2 Proposed Current Comparator II

In the proposed current comparator of Fig. 3, the gain stage employs two resistive load amplifiers. Each resistive load amplifier increases the voltage swing with respect to the previous one and also the charging/discharging time of the respective parasitic capacitances. A modified version which introduces a resistive feedback around Mr3-Mr4 of Fig. 3 is shown in Fig 4. This reduces the impedance at node 'A' and node 'B' and the voltage swing thereby leading to an overall reduction in the comparator's delay.

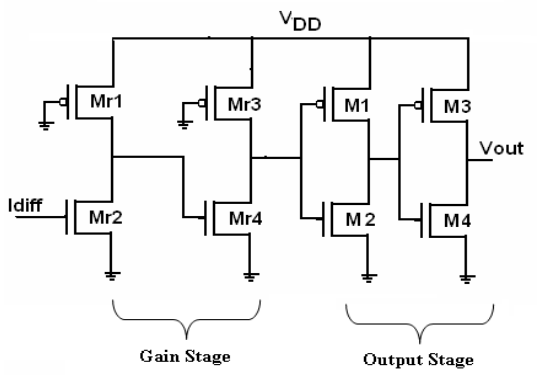

Figure 3. Gain and Output stage

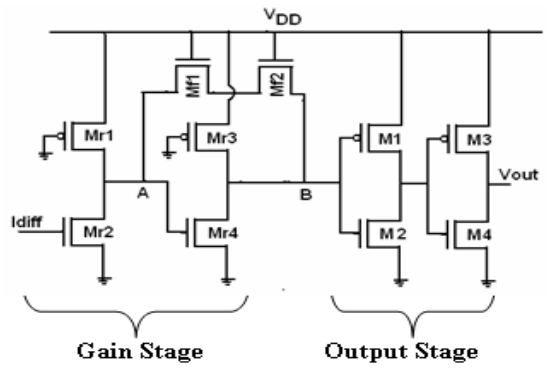

Figure 4. Gain and Output stage

II. 3 Design Example

A promising feature of the proposed comparator is it's application in current mode ADC which plays an important role in front end signal processing. The design of a current mode ADC is presented in this section. The general schematic of a 2-bit current mode flash ADC is shown in Fig. 5. It comprises of three comparators and a thermometer to binary encoder. The circuit of Fig. 4 is used to implement comparators which generate thermometer code (C1, C2 and C3); $B_0 = \overline{C_3}(\overline{C_1} + C_2)$, $B_1 = C_2$.

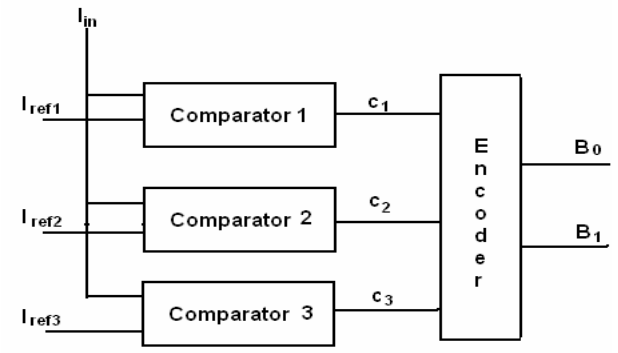

Figure 5. 2 bit Flash ADC

The ADC was designed to work in the current range 0-3µA with the reference currents Iref1, Iref2, Iref3 set at 0.5µA, 1.5µA and 2.5µA. The performance of the ADC is generally characterized by the parameters resolution, sampling rate, INL and DNL. The above mentioned parameters were measured through simulations and presented in the simulation section.

III. SIMULATION RESULTS

To validate the theoretical formulation, the proposed current comparators I and II are simulated under simulation conditions are reported in Table I.

TABLE I. SIMULATION CONDITION FOR PROPOSED CURRENT COMPARATORS I AND II

Temperature	27°C
Technology	TSMC 0.18µm CMOS
Power Supply	1.8 V
Iref	1µA

The performance of the comparators is compared on the basis of propagation delay, power dissipation and power delay product. The propagation delay, power dissipation and power delay product (PDP) of the proposed comparators is shown in Figs. 6, 7, and 8 respectively. The results show that the resolution (minimum current difference that can be detected by the comparator) is equal ± 50 nA. It is observed that the propagation delay of the second comparator is better than the first comparator. This supports our argument that reducing the voltage swing at node 'A' in Fig. 4 results in faster charging/ discharging of the associated parasitic capacitances, leading to a corresponding speed up in the comparator operation. A 2 bit ADC is also simulated and the corresponding results are shown in Fig.9 along with the ideal ADC transfer characteristic. It may be noted that ADC doesn't suffer from missing codes. The DNL was calculated as -0.073 LSB. The INL error is zero.

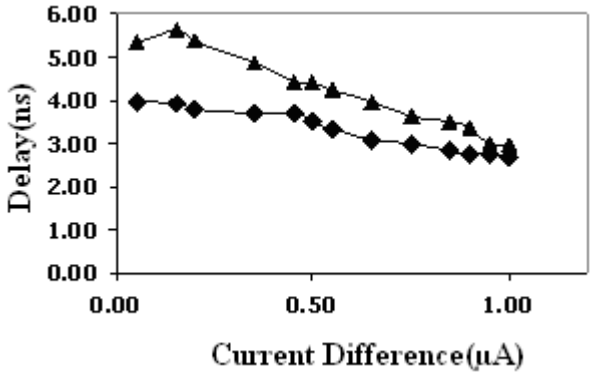

Figure 6. Delay versus current difference for Comparator I (▲) and II (◆)

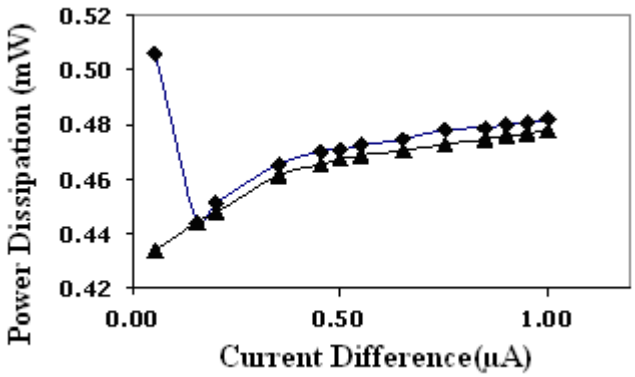

Figure 7. Power Dissipation versus current difference for Comparator I (▲) and II (◆)

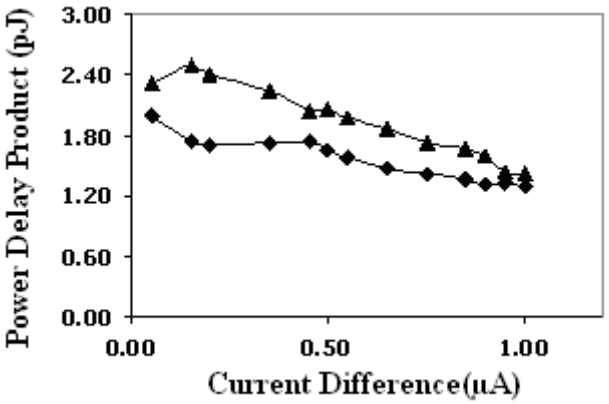

Figure 8. Power Delay Product versus current difference for Comparator I (▲) and II (◆)

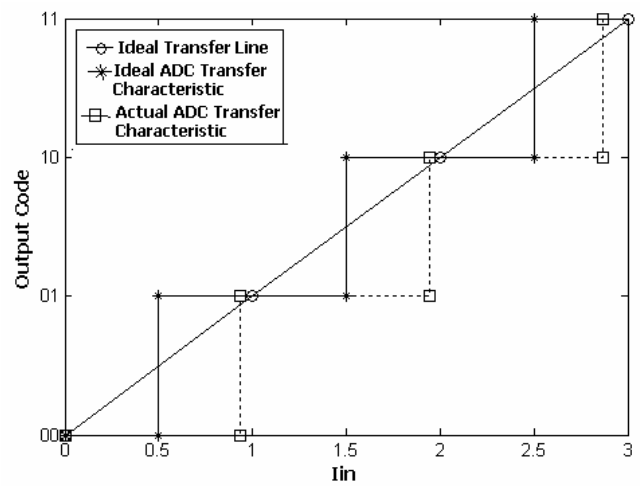

Figure 9. Ideal and simulated ADC characteristics

IV. CONCLUSION

Two new current mode comparators are presented in the paper. Both the comparators use resistive load amplifiers as gain stage. A resistive feedback is introduced in the gain stage of second comparator for improvement in speed, which is supported by simulation results. A maximum of about 30% speed improvement is observed for the comparator with resistive feedback. Both the comparators have a resolution of ±50 nA. The current mode ADC is also designed using the resistive feedback comparator which shows satisfactory performance.

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