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A REFERENCE GENERATING INVERTER-SWITCHING-THRESHOLD-VOLTAGE BASED CURRENT COMPARATOR

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ABSTRACT
A simple and novel design for a current comparator is proposed. The proposed current comparator utilizes the concept of adjustment of switching threshold voltage of an inverter employed in the circuit design to develop a reference current for the purpose of current comparison. The proposed circuit was simulated using 0.18 µm TSMC CMOS technology and satisfactory results were obtained.

Keywords: Current comparator; current mode; switching threshold voltage; CMOS inverter.

I. INTRODUCTION

In last few years, current-mode circuits have become extremely popular in analog design industry. This is attributed to high speed, larger bandwidth and low supply voltage requirements in contrast to the voltage-mode circuits [1]. Current comparator, a popular current mode circuit, finds extensive use in current-mode systems such as ADCs, VLSI neural networks and other signal processing applications [2]. The desirable features of a current comparator are high speed, low input impedance, low power and low supply voltage. The current comparators proposed so far can be categorized as current-mirror based [3-4], Traff based [5-11] and active elements based [12-14].

Current mirror based current comparators [3-4] are commonly used in applications where there is no requirement of higher speed. The operation of these comparators are based on the amplification of input current difference, using high output resistance current mirrors and representing this difference in terms of output voltage. However, this high output resistance causes the deterioration of the frequency performance when the inverter stages are added at the output to achieve rail-to-rail slewing and short transition times.

Traff [5] proposed a current comparator having a significant improvement over current mirror based current comparator design. It employs feedback operation to restrict the input node from slewing rail to rail. Following the structure proposed by Traff [5], many improvements to its structure have been put forth [6-11].

Another class of comparator using active elements such as current conveyor (CCII) [12] and differential current conveyor (DCC) [13] based on Traff concept [5] has recently been proposed in the literature. The Traff [5] and subsequent circuits [6-12] accept input current as the difference between the current to be compared and the reference current. Thus, additional circuitry is required to perform the subtraction operation [6-12]. The implementations require reference current generation [5-13] and a current subtraction circuitry in addition to the one given therein.

In this paper, a simple high speed and low input impedance high resolution CMOS current comparator based on inverter threshold is proposed. The proposed comparator does not require reference current generation and current subtraction circuits, thereby resulting in a compact circuit in comparison to the reported ones [3-14]. The proposed comparator consists of three stages namely a voltage to current converter, a switching-threshold adjustable inverter followed by an output stage. The paper is organized as follows: Section II elaborates the operation of the three stages. The performance of the theoretical proposition is verified through simulations using 0.18µm TSMC CMOS

technology parameters and results are presented in section III. Finally, in Section IV, conclusions are drawn.

II. INVERTER-SWITCHING-THRESHOLD-VOLTAGE BASED CURRENT COMPARATOR

Figure 1 illustrates the proposed scheme of current comparator. The circuit consists of three stages- an NMOS transistor M1, a switching-threshold adjustable inverter (M2-M3) and an output stage inverter (M4-M5).

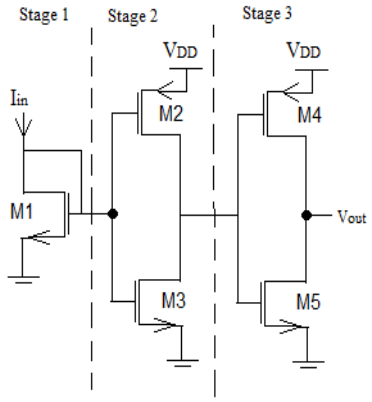

Figure 1. Proposed Current Comparator

The stage-wise procedure adopted for the proposed current comparator is as follows.

In Stage 1, the voltage across transistor M1 for various input currents is computed. The input current, I_{in}, is applied to the gate-drain connected terminal of transistor M1 in stage 1. The variations in I_{in} are reflected in the corresponding gate voltage of M1.

The stage 2 is a switching-threshold adjustable inverter. As the current through an inverter is maximum at its switching threshold voltage so it can be regarded as reference current. For a given reference current, the value of reference voltage (V_{GSref}) is determined from Stage I. Thereafter, the inverter (comprising M2-M3) of Stage II is designed with the switching threshold voltage value equal to V_{GSref} and maximum current of value I_{ref}. At this point, the input voltage and the output voltage across the inverter are equal so both the transistors M2 and M3 operates in saturation, thus,

$$I_{ref} = \frac{k_n}{2}\left(V_{GS,n} - V_{T0,n}\right)^2 = \frac{k_p}{2}\left(V_{GS,p} - V_{T0,p}\right)^2 \quad (1)$$

In terms of V_{GSref}, eqn. (1) may be expressed as

$$I_{ref} = \frac{k_n}{2}\left(V_{GSref} - V_{T0,n}\right)^2 = \frac{k_p}{2}\left(V_{GSref} - V_{DD} - V_{T0,p}\right)^2 \quad (2)$$

or ,

$$V_{GSref} \bullet \left(1 + \sqrt{\frac{k_p}{k_n}}\right) = V_{T0,n} + \sqrt{\frac{k_p}{k_n}} \bullet \left(V_{DD} - \left|V_{T0,p}\right|\right) \quad (3)$$

Finally, the inverter switching threshold voltage V_{th} is,

$$V_{th} = V_{GSref} = \frac{V_{T0,n} + \sqrt{\frac{k_p}{k_n}} \bullet \left(V_{DD} - \left|V_{T0,p}\right|\right)}{\left(1 + \sqrt{\frac{k_p}{k_n}}\right)} \quad (4)$$

The aspect ratios of the transistors in stage 2 (M2-M3) are obtained by V_{GSref} of stage 1 for a given input current I_{in} and the reference current I_{ref}, using the following relation-

$$\sqrt{\frac{k_p}{k_n}} = \frac{V_{th} - V_{T0,n}}{\left(V_{DD} - \left|V_{T0,p}\right| - V_{th}\right)} \quad (5)$$

Once this is calculated, we can calculate aspect ratios as-

$$\frac{k_n}{k_p} = \frac{\mu_n C_{ox} \bullet \left(\frac{W}{L}\right)_n}{\mu_p C_{ox} \bullet \left(\frac{W}{L}\right)_p} \quad (6)$$

Or

$$\frac{\left(\frac{W}{L}\right)_n}{\left(\frac{W}{L}\right)_p} = \frac{k_n \bullet \mu_p}{k_p \bullet \mu_n} \quad (7)$$

The aspect ratio of M2 and M3 are determined by (3) and (7).

$$\left(\frac{W}{L}\right)_n = \frac{2I_{ref}}{\mu_n C_{ox}(V_{GS,ref} - V_{T0,n})^2} \quad (8)$$

$$\left(\frac{W}{L}\right)_p = \frac{2I_{ref}}{\mu_n C_{ox}(V_{GS,ref} - V_{DD} - |V_{T0,p}|)^2} \quad (9)$$

In Stage 3, the output voltage of Stage 2 is amplified through an inverter (comprising M4-M5) to provide rail-to-rail swing.

The merit of the proposed current comparator is faster speed and area efficiency along with the elimination of an additional reference current source. Secondly, the output stage inverter being the replica of switching threshold adjusted inverter offers regularity of structure. Further, the proposed circuit is capable of performing complete comparison of currents without requiring any additional subtraction circuitry in contrast to the proposed comparators in [5-12]. The performance of the proposed current comparator is comparable to the one proposed in [11], additionally, our structure offers the advantage of being a completely active component based circuit in contrast to the one in [11] which uses R and C elements. This makes proposed circuit fully integrable.

III. SIMULATIONS AND RESULTS

The performance of the proposed current comparator is studied through pre and post layout simulations using 0.18µm TSMC CMOS technology parameters and supply voltage of 1.8 V. The current comparator of Fig. 2 has been designed for reference current of 5 µA. The aspect ratios of various transistors are given in Table 1.

Figure 2 shows the time domain behavior of the proposed circuit with a current pulse input of amplitude 200 nA (4.9 µA to 5.1 µA as I_{ref} = 5 µA). The circuit exhibits a propagation delay of about 6.6 ns and power dissipation of 17.2 µW. The power delay product (PDP) is calculated as 0.113 pJ. The circuit gives the maximum slew rate of 0.33 V/ns.

Table 1 MOSFET W/L settings of various transistors

Transistor	Aspect ratio
M1	0.27µm/0.77µm
M2	0.27µm/0.60µm
M3	0.27µm/0.77µm
M4	0.27µm/0.60µm
M5	0.27µm/0.77µm

.

To see the behavior of the circuit for larger current pulse inputs, simulations were also carried out. Figure 3 and 4 show the results for power dissipation and propagation delay dissipation respectively.

It is observed that propagation delay as well as power dissipation decrease with increase in input current amplitude. This is a direct consequence of faster switching for larger values of input current amplitude. Simulations were also carried out for 1.2 V supply and satisfactory performance was achieved.

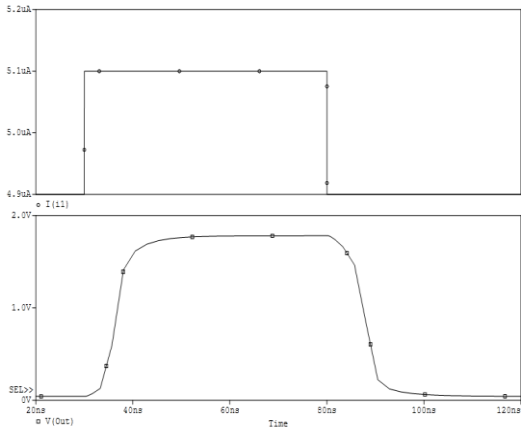

Figure 2 Simulation results for the proposed Current Comparator

The comparator [11] performance is better than those reported in [6-10] in terms of speed and area, so simulations were carried out to compare its delay performance with the proposed current comparator. The same has been illustrated in Figure 4. It was observed that at lower input current amplitudes of the order of 100-200nA, the delay performance of the proposed current comparator and the one reported in [11] are almost comparable. There is significant improvement for higher input current amplitudes in the proposed current comparator.

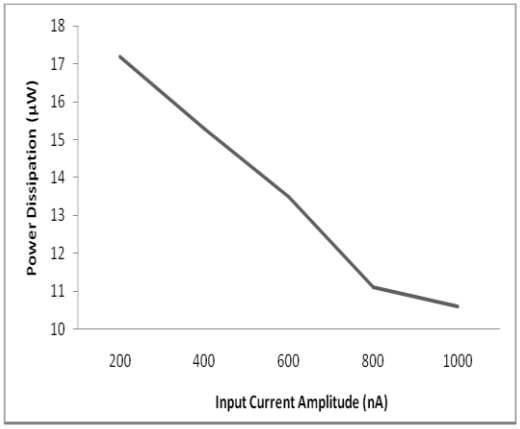

Figure 3. Variation in power dissipation with input current amplitudes

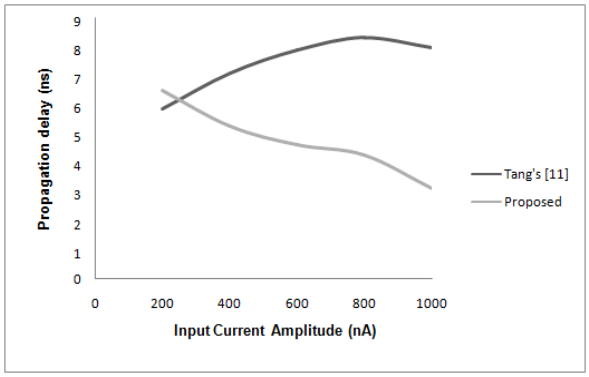

Figure 4. Variation of propagation delay with input current amplitudes

IV. CONCLUSION

A novel CMOS current comparator based on the switching threshold voltage of the inverter is proposed in this paper. The proposed structure is simple, fast and area efficient. This makes it suitable for a vast variety of current mode applications.

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