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PERFORMANCE OF A TWO INPUT NAND GATE USING SUBTHRESHOLD LEAKAGE CONTROL TECHNIQUES

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ABSTRACT

This paper presents performance comparison analysis of a two input NAND gate using conventional CMOS, stack, sleep and sleepy keeper techniques. Performance characteristics of a two input NAND gate were analysed in 45 nm technology using BSIM4 model. Sleepy Keeper technique dissipated lesser static power and lesser static power delay product (PDP_{static}) in comparison with the other techniques. An improvement of 1.4 X and 1.3X were observed in static power dissipation and static power delay product respectively by using the Sleepy keeper technique in comparison with the conventional CMOS technique. Sleepy keeper technique lowers the subthreshold leakage power dissipation while maintaining the logic state of the digital circuit.

Keywords: static power, propagation delay, static power delay product, subthreshold current.

I. INTRODUCTION

The increasing demand for portable electronic appliances has triggered numerous research efforts in low power VLSI circuit design. The operating time of an electronic system powered with batteries is heavily restricted by its limited battery backup time [1]. With the improvement in scaling of MOS transistors, more numbers of transistors are packed into a chip. Scaling in size of MOS transistor causes an increase in the integration capacity of VLSI chips. The increase in integration capacity in a chip increases its functionality and its processing capacity. This results in the overall increase in the power dissipation by the VLSI chip. It has been observed that the electronic component failure rate roughly doubles with an increase in the operating temperature by 10 °C [2]. Reliability of an electronic device decreases with the rise in the operating temperature. Also high power dissipation accelerates the silicon failure mechanism in MOS transistors.

The need for reducing power dissipation in electronic systems varies from application to application. In battery operated portable systems, such as mobile phones and personal digital assistants, power dissipation should be reduced because of the use of limited backup time batteries. For high performance non battery operated systems, such as workstations and multimedia digital signal processors, the main objective in reducing the power dissipation is to reduce the overall system costs that include system cooling cost, cost due to expensive packaging technique and high electricity bill. These different requirements for reducing the overall power dissipation can be achieved through proper research initiatives in designing efficient and effective low power digital circuit design techniques.

Power dissipation is becoming widely recognized as a top-priority issue in VLSI circuit design. One of the most challenging problems faced by the VLSI designer in present scenario, is to find out new and effective circuit design techniques to reduce the overall power dissipation without compromising the performance of the device.

II. SOURCES OF POWER DISSIPATION

Power dissipation in VLSI circuits can be broadly divided into two categories: Dynamic or switching power, and Static or leakage power dissipations. Dynamic power dissipation results due to charging and discharging of internal capacitances in the circuit. Leakage power dissipation occurs during the static input state of the device. Leakage power dissipation is much more noticeable in low threshold voltage MOS transistors. This power dissipation arises because of the presence of subthreshold and gate oxide leakage currents. Gate oxide leakage current occurs because of the desire to increase the performance characteristics of MOS transistor by decreasing the thickness of the gate

oxide layer while subthreshold leakage current occurs between the source and the drain region of a MOS transistor in weak inversion state. The subthreshold leakage current occurs even when the applied gate voltage, V_{GS}, is less than the threshold voltage, V_{TH}, of the MOS transistor. A general formula for the total power dissipation in a VLSI circuit can be expressed as [3]

$$P_T = P_{dynamic} + P_{static} . \quad (1)$$

$$P_T = \alpha C V_{DD}^2 f_{clk} + N(1-\alpha) V_{DD} I_S + N(1-\alpha) V_{DD} I_{ox} . \quad (2)$$

where α is the switching activity factor which represents the probability of the output switching, C is the sum of all load capacitance in the design, V_{DD} is the supply voltage, f_{clk} is the clock frequency, N is the number of gates, I_S is the average subthreshold leakage current of a gate, and I_{OX} is the average thin-oxide leakage current of a gate.

Subthreshold leakage current is the main component of leakage power dissipation in VLSI circuits in Deep Submicron and nanoscale technologies. Hence P_T may be approximated as

$$P_T = \alpha C V_{DD}^2 f_{clk} + N(1-\alpha) V_{DD} I_S . \quad (3)$$

III. SUBTHRESHOLD LEAKAGE POWER REDUCTION TECHNIQUES

Fig. 1 [4] shows that subthreshold leakage current (power) is the most dominant component of leakage current (power) in short channel MOS transistors. This leakage current is caused by the inability to completely turn off a MOS transistor. In long channel MOS transistors, the threshold voltage is considered as the boundary between the cutoff and active inversion region. However, in short channel MOS transistor, this boundary is not abrupt and the transistor conducts even in weak inversion region below the threshold voltage of the MOS transistor. Fig. 2 shows the flow of subthreshold leakage current when the applied gate voltage, V_{GS}, is less than the threshold voltage, V_{TH} , of an nMOS transistor.

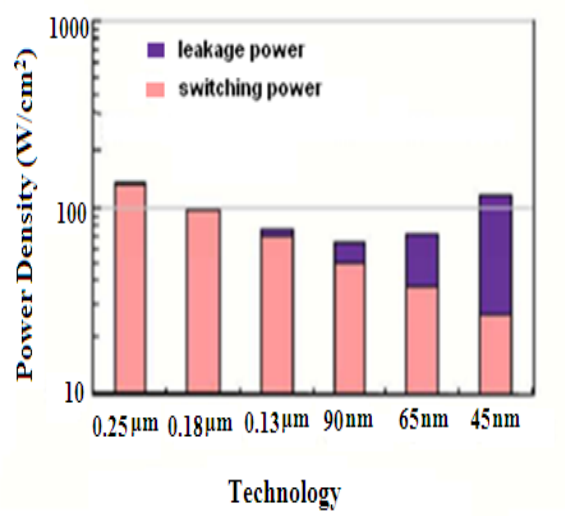

Figure 1: Leakage Vs Switching power dissipation trends

According to BSIM4 MOSFET model, the equation governing this subthreshold leakage current can be expressed as [5]

$$I_{SB} = I_0 e^{\{(V_{GS} - V_{TH0} - \eta V_{DS} + \gamma V_{SB})/nV_T\}} \{1 - e^{(-V_{DS}/V_T)}\} \quad (4)$$

where

$$I_0 = \mu C_{OX} (W/L) V_T^2 e^{1.8} \quad (5)$$

$$V_T = KT/q \quad (6)$$

here V_{GS}, V_{DS} and V_{SB} are the gate to source, drain to source, and source to bulk voltages respectively of a MOS transistor, μ denotes the carrier mobility, Cox is the gate oxide capacitance per unit area, W and L denote the width and length of the channel of the transistor, K is the Boltzmann constant, T is the absolute temperature, q is the electrical charge of an electron, V_T is the thermal voltage, V_{TH0} is the zero biased threshold voltage, γ is body effect coefficient, η denotes the drain induced barrier lowering coefficient, and n is the subthreshold swing coefficient.

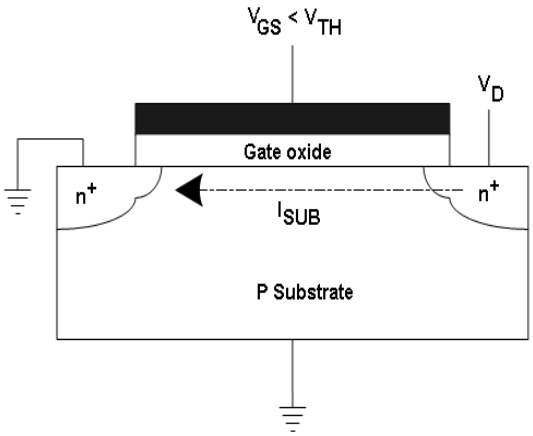

Figure 2: Subthreshold leakage current in an nMOS transistor

It is evident from (4) that the subthreshold leakage current is a strong function of the threshold voltage of a MOS transistor. This leakage current is highly undesirable in a digital circuit in deep submicron and nanoscale technologies. Fig. 3 [6] shows the subthreshold leakage power dissipation trends according to the International Technology Roadmap for Semiconductors.

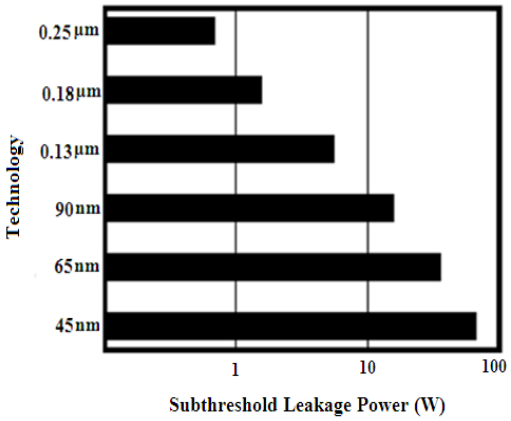

Figure 3: Subthreshold leakage power dissipation trends

In order to reduce power dissipation in digital circuits, its supply voltage is scaled down. However, with the reduction in the supply voltage, circuit propagation delay increases. In order to reduce this increase in the propagation delay, threshold voltage of the MOS transistor is reduced. The reduction in the threshold voltage leads to increase in subthreshold leakage current in short channel MOS transistors. This leakage current is the most dominant source of leakage power dissipation in deep submicron and nanoscale technologies.

Subthreshold leakage current increases exponentially with the decrease in the threshold voltage of the MOS transistor. So, increasing the threshold voltage of the transistor is an effective way to reduce subthreshold leakage current. Portable battery operated systems such as mobile phones and electronic pagers, that remain idle for most of the times, are severely affected by this leakage power loss.

Circuit level design techniques for subthreshold leakage power reduction can be grouped into two categories: state preserving and state destructive techniques. In a state preserving technique, the present state of the circuit is retained even in sleep mode while in a state destructive technique, the circuit present state is lost in sleep mode as this technique cuts off the pull up and the pull down networks from the power supply and the ground using sleep transistors of high threshold voltage when sleep signal is activated [7].

III.1 Conventional CMOS Technique

Fig. 4 shows the block diagram of a digital circuit using conventional CMOS technique. In this approach, pull up network is designed using pMOS transistors and pull down network by nMOS transistors. Pull up network is connected to the power supply, V_{DD} while the pull down network is connected to the ground, GND.

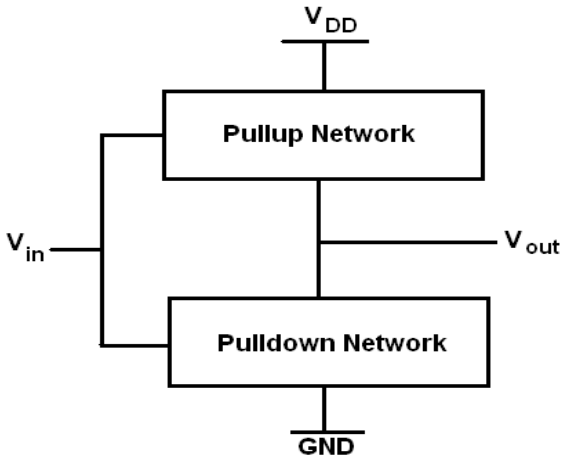

Figure 4: Digital Circuit using conventional CMOS technique

III.2 Stack technique

Fig. 5 shows the block diagram of a digital circuit using Stack technique. A MOS transistor in the circuit is divided and stacked into two half width size transistors. When two half size stacked MOS transistors are turned off together, induce reverse bias between them results in the reduction of the subthreshold leakage power [8]. However, increase in the number of transistors increases the overall propagation delay of the circuit.

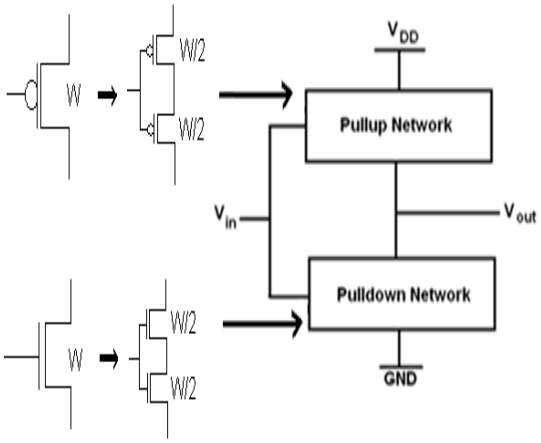

Figure 5: Digital circuit using Stack technique

III.3 Sleep Technique

Sleep transistors of high threshold voltages are used in the Sleep technique [9]. Fig. 6 shows the block diagram of a digital circuit using sleep technique. A sleep pMOS transistor is placed between the supply voltage, V_{DD} and the pullup network and a sleep nMOS transistor is placed between the pulldown network and the ground, GND. These sleep transistors are turned ON when the circuit is in active state and turned OFF when the circuit is in sleep state. This technique reduces the subthreshold leakage current by cutting off the logic circuitry from the power supply voltage and ground in the sleep state. These sleep transistors are driven by sleep signals. Using this technique the present state of the circuit is lost and thus results in destruction of the present logic state.

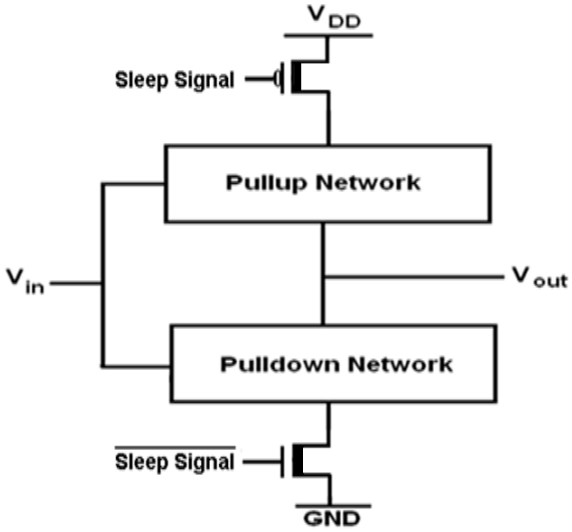

Figure 6: Digital circuit using Sleep technique

III.4 Sleepy Keeper Technique

Sleepy keeper technique [10] is an improved version of the sleep technique. Fig. 7 shows the block diagram of a digital circuit using Sleepy keeper technique. In this technique, an additional high threshold voltage nMOS transistor is connected in parallel with the sleep pMOS transistor and an additional high threshold voltage pMOS transistor is connected in parallel with the sleep nMOS transistor. In sleep mode, the sleep transistors are in cutoff state. So, when sleep signal is activated, then the high threshold voltage nMOS transistor connected in parallel with the sleep pMOS transistor is the only source of power supply to the pullup network and the high threshold voltage pMOS transistor connected in parallel with the sleep nMOS transistor provides the path to connect the pulldown network with ground. The major advantage in using Sleepy keeper technique is that it reduces the significant subthreshold leakage current and also retains the circuit present state in sleep mode.

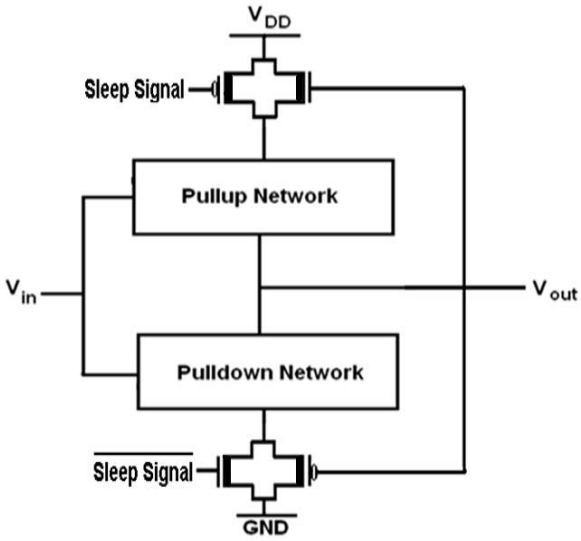

Figure7: Digital circuit using Sleepy keeper technique

IV. SIMULATION RESULTS

Microwind EDA tool was used for the layout and simulation of a two input NAND gate using BSIM4 MOSFET model in 45 nm technology. Performance characteristics such as static power dissipation, dynamic power dissipation, propagation delay and power delay products in static and dynamic conditions were observed using conventional CMOS, Stack, Sleep and Sleepy keeper techniques at a temperature of 27 ^{0}C and a Supply voltage, V_{DD} of 0.40 V.

Tables 1 to 4 show the physical aspects of MOS transistors used to design a two input NAND gate using various techniques. The threshold voltage of a MOS transistor increases with the increase in its channel length. So, the channel lengths of high threshold voltage transistors and sleep transistors were chosen greater than the normal threshold voltage transistors in Sleep and sleepy keeper techniques. Fig. 8 to 11 show the layout diagrams of a two input NAND gate using Conventional CMOS, stack, sleep and sleepy keeper techniques respectively. Table 5 shows all possible static input combinations for measuring static power dissipation in a two input NAND gate. Fig. 12 shows the waveform to measure the dynamic power dissipation in the logic gate using conventional CMOS and stack techniques. Similarly Fig. 13 shows the waveform to measure the dynamic power dissipation in the two input NAND gate using sleep and sleepy keeper techniques.

Static power dissipation was obtained by combining all possible static input combinations. The overall static power dissipation was calculated as the average of power dissipation in all possible static input combinations. In the case of Sleepy Keeper technique, Sleep and high V_{TH} transistors were turned OFF when the sleep signal was activated while they were turned ON when the sleep signal was deactivated. This static power was measured for 50 ns time interval.

Dynamic power dissipation was obtained by applying two dynamic clock inputs A and B of same frequency of 200 MHz and at a temperature of 27 ^{0}C. The supply voltage, V_{DD} was fixed at 0.40 V. In the case of Sleepy Keeper technique, sleep and high V_{TH} transistors were turned ON during the measurement of dynamic power dissipation. This power dissipation was also measured for 50 ns time interval.

Propagation delay of the logic gate was measured from the trigger input edge reaching 50 % of V_{DD} to the circuit output edge reaching 50 % of V_{DD}.

Power delay product is measured to determine the efficiency of a circuit in terms of both power dissipation and propagation delay. Power delay product of a digital circuit is the product of its power dissipation and its propagation delay. Static and dynamic power delay products were obtained for the logic gate using various techniques.

Table 1: Physical aspects of MOS transistors using CMOS technique

Physical Aspect	nMOS transistor	pMOS transistor
Channel width (μm)	0.15	0.30
Channel Length (μm)	0.05	0.05
Aspect ratio	3.00	6.00

Table 2: Physical aspects of MOS transistors using Stack technique

Physical Aspect	nMOS transistor	pMOS transistor
Channel width (µm)	0.08	0.15
Channel Length (µm)	0.05	0.05
Aspect ratio	1.50	3.00

Table 3:.Physical aspects of MOS transistors using Sleep technique

Physical Aspect	Normal nMOS transtr.	Normal pMOS transtr.	Sleep nMOS transtr.	Sleep pMOS transtr.
Channel width (µm)	0.15	0.30	0.21	0.42
Channel Length (µm)	0.05	0.05	0.07	0.07
Aspect ratio	3.00	6.00	3.00	6.00

Table 4: Physical aspects of MOS transistors using Sleepy keeper technique

Physical Aspect	Norm. nMOS transtr	Norm. pMOS transistr	Sleep nMOS and high V_{TH} transistr	Sleep pMOS and high V_{TH} transistr
Channel width (µm)	0.15	0.30	0.21	0.42
Channel Length (µm)	0.05	0.05	0.07	0.07
Aspect ratio	3.00	6.00	3.00	6.00

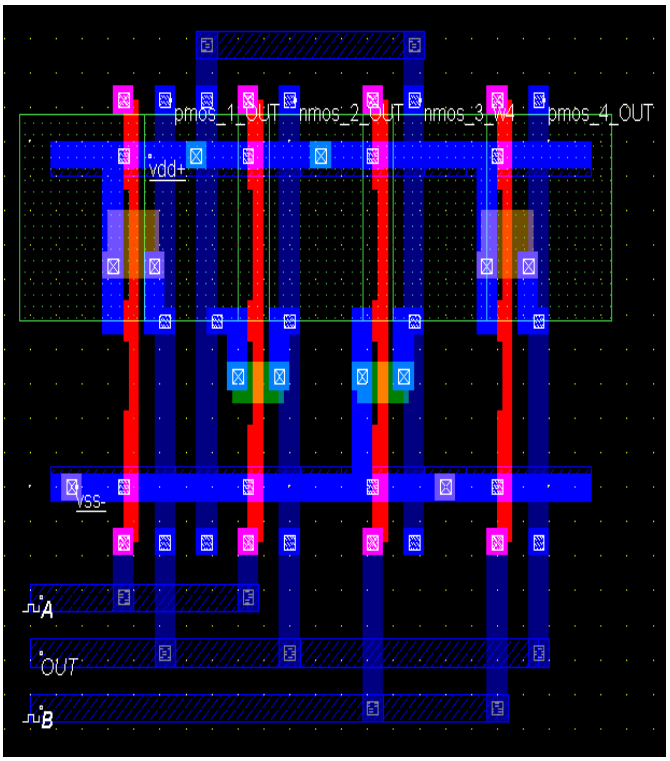

Figure 8: Layout of a two input NAND gate using conventional CMOS technique

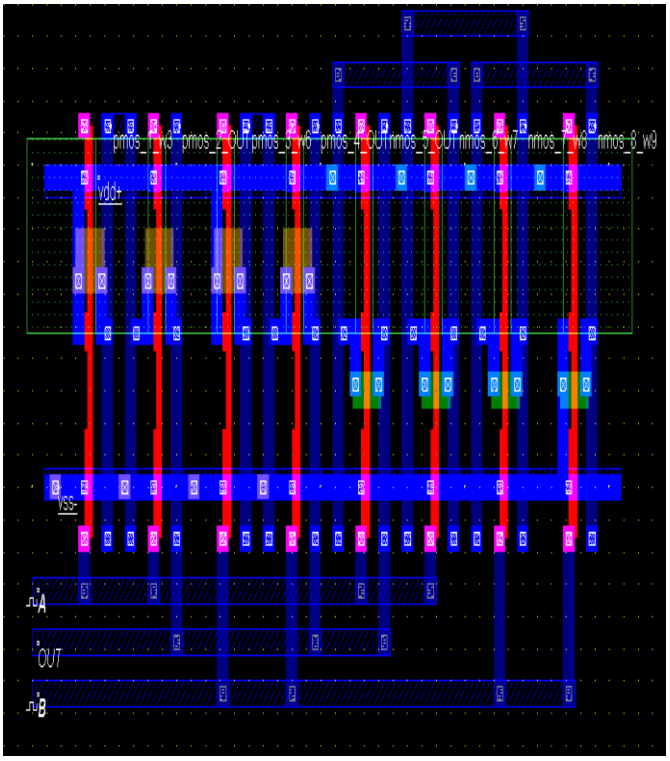

Figure 9: Layout of a two input NAND gate using Stack technique

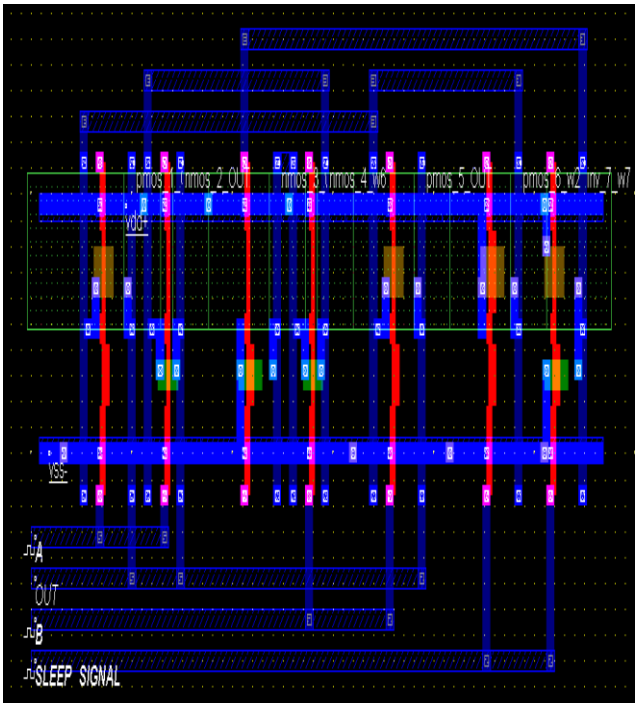

Figure10: Layout of a two input NAND gate using Sleep technique

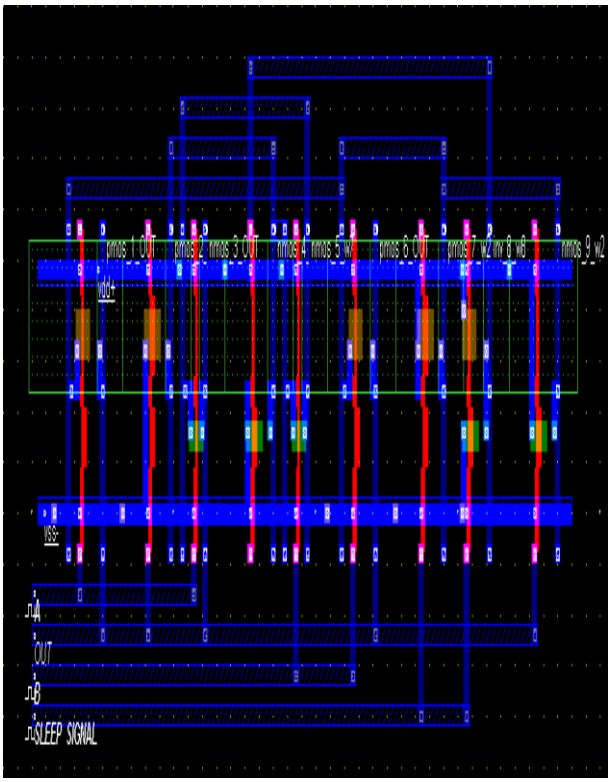

Figure 11: Layout of a two input NAND gate using Sleepy Keeper technique

Table 5:. Static input combinations for measuring static power dissipation

Static input A	Static input B	Output Y
0	0	1
0	1	1
1	0	1
1	1	0

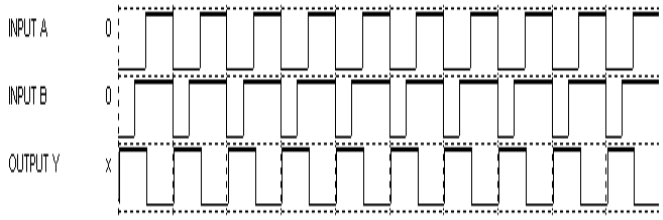

Figure 12: Waveform to measure the dynamic power dissipation using conventional CMOS and Stack techniques

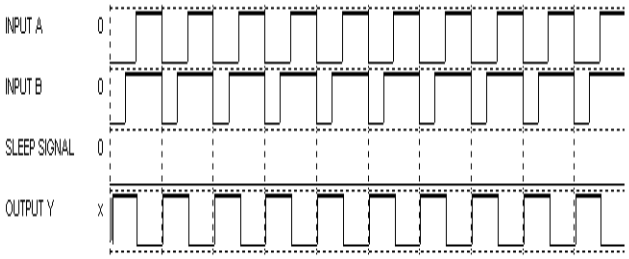

Figure 13: Waveform to measure the dynamic power dissipation using sleep and sleepy keeper techniques

V. PERFORMANCE COMPARISON

Tables 6 and 7 show the performance characteristics comparison of a two input NAND gate using various techniques in 45 nm technology. Fig.14 shows Static power dissipation comparison of the logic gate using various techniques. Static power dissipation of the logic gate was 0.052 µW using the conventional CMOS technique while only 0.037 µW static power was dissipated using the Sleepy keeper technique. Fig. 15 shows the Static power delay product (PDP_{static}) of the logic gate using various techniques. Static power delay product of the logic gate using conventional CMOS and sleepy keeper

techniques were 0.5304 x 10^{-19} J and 0.4218 x 10^{-19} J respectively. Dynamic power dissipation using the sleepy keeper technique increased because of the use of additional high threshold voltage transistors.

Table 6: Performance characteristics of a two input NAND gate

Techniques	Static power dissiptn. (μW)	Dynamic power dissiptn. (μW)	Delay (ps)	State saving
Conventional CMOS	0.052	0.102	12.8	Yes
Stack	0.046	0.098	19.6	Yes
Sleep	0.041	0.109	14.8	No
Sleepy keeper	0.037	0.114	16.0	Yes

Table 7: Static and Dynamic Power Delay Products

Techniques	Static power delay product (E-19 J)	Dynamic power delay product (E -18 J)
Conventional CMOS	0.5304	1.8972
Stack	0.4508	2.5872
Sleep	0.4469	2.4198
Sleepy keeper	0.4218	2.6904

VI. CONCLUSION

Performance characteristics such as static power dissipation, dynamic power dissipation, propagation delay and power delay products in static and dynamic conditions of a two input NAND gate were analyzed using various techniques. Performance characteristics of the logic gate were compared using conventional CMOS, Stack, Sleep and Sleepy keeper techniques in 45 nm technology. Sleepy Keeper technique provided lesser static power dissipation and lesser static power delay product in comparison with the other techniques. The main advantage of using Sleepy Keeper technique is that it retains the logic state and also lowers the subthreshold leakage power dissipation. In deep submicron and nanoscale technologies, this technique can be utilized for designing digital circuits with improvement in the overall static power dissipation, which is mainly due to subthreshold leakage power dissipation. Also efficiency in terms of static power delay product can be improved by using this technique.

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