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AN SOI LDMOS FOR BETTER SWITCH APPLICATION INCREASING THE DRIFT REGION OF AN N-MOS: A COMPARATIVE STUDY

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ABSTRACT

In this paper we propose to develop an SOI (Silicon on Insulator) LDMOS in which a drift region of 1-μm is added to a conventional n-MOS and compare them on various aspects. The drift region utilizes the RESURF effect that is utilized to distribute the electric field into the LDD region. It is found using two dimensional simulations that the addition of a drift region of 1-μm in LDMOS improves the performance of the device in terms of breakdown-voltage and switching-speed over the conventional MOSFET. We demonstrate that the proposed devise show an improvement in the breakdown voltage by 280%, reduction of transconductance by 84% and switching speed improves by 198%**.** However, as for the disadvantages, it increases on-resistance (R_{on}) and causes higher power dissipation. This LDMOS can be effectively used as a powerful switch.

Keywords: LDMOS, Switch Application, Drift Region, n-MOS.

I. INTRODUCTION

Faster and high frequency data-transfer wireless communication has necessitated the demand for high-voltage [1,2], cost-effective, linear Silicon-on-Insulators (SOI), that is known as Laterally Double Diffused Metal-Oxide Semiconductors (LDMOS). The LD-MOSFET as a novel technology has started to challenge silicon transistor because of reduced distortion while being more competitive than the gallium arsenide device due to significantly lower cost**.** Recently they have gained a surging interest for potential application in wireless communication, such as power amplification at microwave/RF frequencies for base-station transmitters.

This is because of its ease in integration to standard CMOS technology, high input impedance at high drive current and thermal stability. Especially, SOI LDMOS is more attractive due to its inherent dielectric isolation, high frequency performance and reduced parasitic. Improvements in its efficiency and linearity provided significant cost performance benefit to the end user**.** For high-

voltage application, the breakdown phenomenon in the transistor must be restrained. Conventional n-MOS are prone to breakdown phenomenon at high voltage application. In addition the switching speed for n-MOS is not congenial for high data-rate applications such as GHz frequency applications, which are necessary for 3G and its higher version implementation.

An LDMOS is based on the principle of increasing breakdown-voltage by incorporating a drift region (a lightly doped drain region**)** between the gate and drain of a conventional n-MOS. This enables the electric field to be distributed between the drift-region and the gate to sustain this vulnerable breakdown phenomenon. Due to the incorporation of this region, the on-resistance is increased giving rise to comparatively higher power dissipation. As per a non-exhaustive literature survey, much work on model development [3-5], retrograded doping profile [6], hot-electron effect [7-10], circuit-optimization [11] is already done, but a numerical comparison between the n-MOS and LDMOS based on the physics of semiconductor devices is still needed.

Therefore, we carried out a numerical experiment based on the applicable data on n-MOS and LDMOS by fixing certain parameters. In this paper, a numerical comparison based on the elementary physics of semiconductor devices [12] between the conventional n-MOS and LDMOS is carried out. The LDMOS device is characterized by 1-μm drift region for 38-V applications, which seems to fulfill the requirement for 3G applications [13].

II. SIMULATION RESULTS AND DISCUSSION

Two dimensional numerical simulations of the LD-MOSFET structure was performed using Silvaco TCAD - ATLAS software [14] with various layers and concentrations of as discussed below.

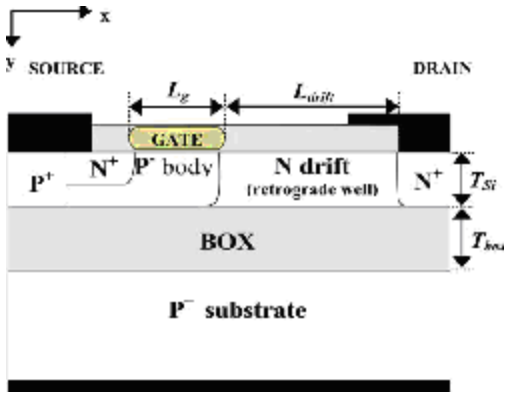

Fig. 1: Cross-section of a 38V LDMOS transistor.

Fig. 1: shows the cross-section of a 38-V n-channel LDMOS transistor in SOI. The gate oxide thickness is $500\,\overset{0}{A}$. S/D, substrate and drift region doping are10^{20} /cm^3, 10^{17}/cm^3 and 10^{16}/cm^3 respectively. Drift region and channel length are both taken as 1-μm for this simulation work.

ATLAS is a physically-based two and three dimensional device simulator. It predicts the electrical behavior of specified semiconductor structures and provides insight into the internal physical mechanisms associated with the device operation. ATLAS can be used as standalone or as a core tool in Silvaco's "virtual wafer fab" simulation environment. In the sequence of predicting the impact of process variables on circuit performance, the device simulation fits between process simulation and SPICE model extraction.

The most important aspect is that it simulates a device in Atlas to generate the grid and mesh of the device. At the junction, the grid should be highly dense for precision, whereas for the other part of the device, it should be sparse to avoid high calculation and simulation time.

II.1 Current-Voltage Characteristics

II.1.1 On-resistance

When a positive bias above the threshold voltage is applied to the gate of LDMOS, an inversion layer is formed at the surface of the base region. This provides a path between the drain and

the source terminal and current flows from the source to the drain.

LDMOS on-resistance is a vital parameter to study. On-resistance for a conventional n-MOS [15] can be written as:

$$R_{on}=R_s+R_{ch}+R_D \quad . \qquad (1)$$

For LDMOS, the resistance of the drift region is added to it. Now the expression becomes:

$$R_{on}=R_s+R_{ch}+R_D+R_{drift} \quad . \qquad (2)$$

Hafyene et al utilizes the on-resistance using the drain voltage (V_D) and the intrinsic drain voltage (V_K) as [16]:

$$R_{ON}=R_{MOS}+R_{Drift}=\frac{V_K}{I_D}+\frac{V_D-V_K}{I_D} \qquad (3)$$

Kyungho et al modeled a nonlinear drift resistance for large-signal RF LDMOS **[17].** They modeled nonlinear drift-resistance as:

$$R_{dn}(V_{GS1},V_{DS,B1})=\frac{V_{DS,B1}-V_{DS,A1}}{I_{DS1}}\times K_{L_{ldd}} \quad (4)$$

So, a higher on-resistance curve is derived for LDMOS. At V_{DS}=5 Volts, there is a 75% increase in on-resistance for LDMOS as shown in Figure 2a.

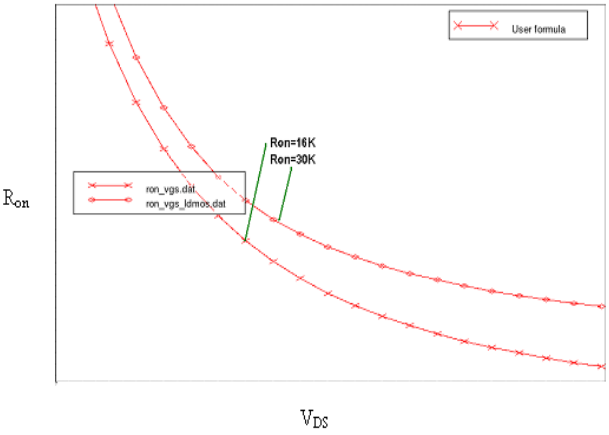

Fig2a: R_{on} vs. V_{DS} for n-MOS and LDMOS.

The on-resistance optimization is a key area of research in the field of HV-devices [1,2]. A dynamic study of V_K needs to be done using a powerful mathematical technique such as finite element method to get full control on such devices, which is subjected to our future research work.

II.1.2 Transfer Characteristics

Transfer characteristics shows the relation of the drain current (I_D) with the variation of the gate voltage (V_{GS}) keeping the drain voltage (V_{DS}) fixed. The drain-current flows only if the gate voltage exceeds the threshold V_{th} following the relation:

$$I_D=I_{DSS}(V_{GS}-V_{th})^2 \qquad (5)$$

However, for LDMOS after the threshold voltage the current of LDMOS is lower than that of conventional MOS. This is due to the fact that it has higher on-resistance [18]. R_{on} is higher due to the addition of the drift region.

At V_{DS}=0.1 Volt, the drain current I_D is plotted against gate voltage V_{GS} (Fig.2b).

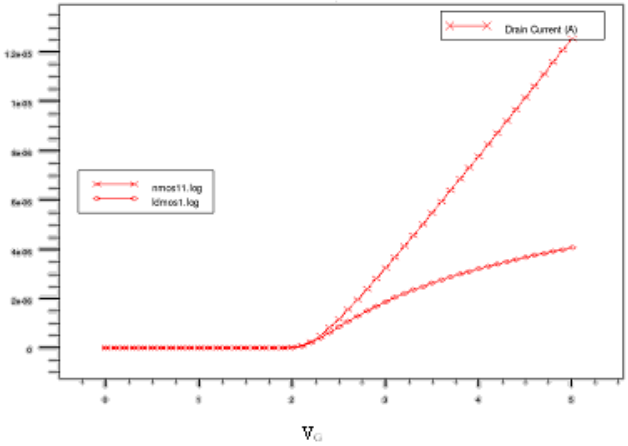

Fig. 2b: Drain characteristics (V_{GS} vs I_D).

As both substrate doping concentration and oxide thickness are same for both the devices, the threshold voltage is same (2.1 Volt). Theoretically also, the calculated threshold voltage is 2.08 Volt for the given parameters. Here, after the threshold voltage, the current of LDMOS is lower than that of conventional MOS. It is due to the fact that it has a higher on-resistance (R_{on}).

II.1.3 Transconductance

Another behavior derived from this curve is the transconductance curve. Transconductance is given by:

$$g_m = \frac{\partial I_D}{\partial V_{GS}}\Big|_{V_{DS}} = cons\tan t \qquad (6)$$

As output of the amplifier is directly proportional to that of transconductance, it is very important that it is of high value. However, LDMOS shows a low transconductance due to the higher on-resistance. The g_m value gradually decreases after the peak due to the mobility of the electrons that gets reduced after the drain voltage gets saturated (V_{DS}). The peak transconductance of the conventional device improves by approximately 84 % as compared to that of LDMOS, as shown in Fig.3.

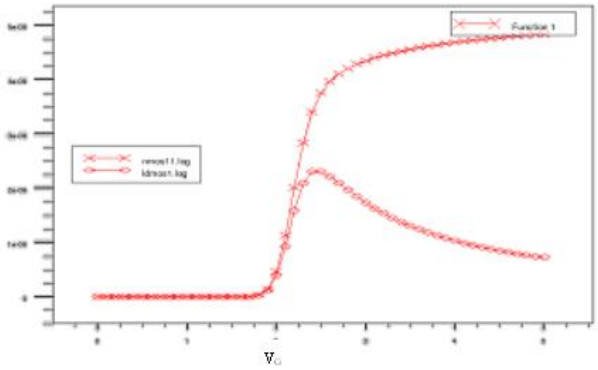

Fig. 3: Transconductance (g_m) vs gate voltage (V_G) curve.

From the simulation, it is also evident that conventional MOS shows a flat peak as compared to a sharp peak of LDMOS

II.1.4 Breakdown Voltage

In MOSFET when V_{DS} exceeds a certain value, the drain current abruptly increases. As V_{DS} increases, the peak electric field at drain end of the channel also increases. When the peak electric field approaches the middle of 10^5 V/cm range, the impact ionization takes place at the drain junction leading to sharp increase in I_D. The high-energy electrons, which have gained energy from electric field, have sufficient kinetic energy to generate secondary electrons and holes by impact ionization. The generated electrons are collected at the drain and then added to I_D, while the holes flow to the substrate contact resulting in substrate current.

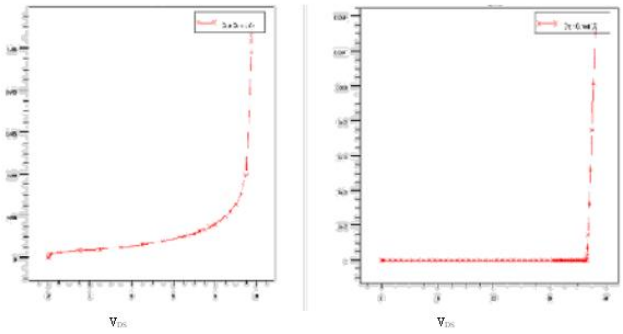

Fig. 4: I_D vs V_{DS} curve showing breakdown voltage.

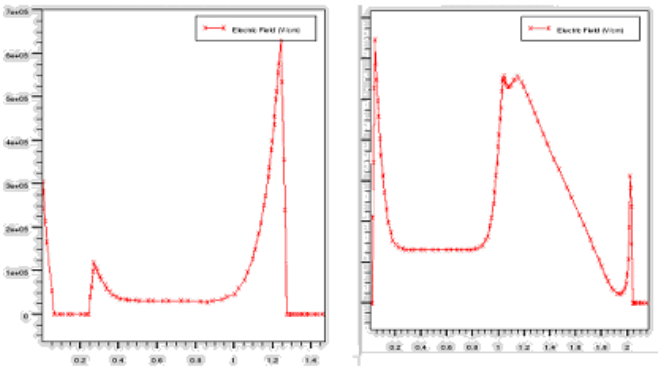

Fig. 5: Electric Field distribution for n-MOS and LDMOS.

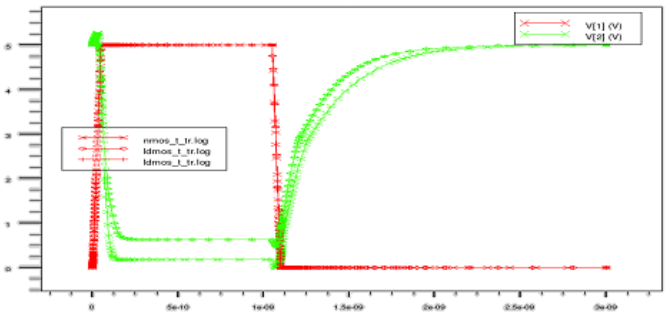

Fig. 6: Transient Analysis of Inverter circuit

In LDMOS the drift region supports the applied voltage and protects the channel region from high voltage. The drift utilizes the RESURF [19] concept. At the applied potential, the depletion stretches along the lateral length or surface over a much longer distance. Therefore, the electric field is far below the critical field (E_c) and hence more voltage can be applied before breakdown occurs. It can also be seen from impact ionization rate that it is shifted from the drain (Fig.6).

Due to the addition of drift region, the breakdown voltage increases to 280% (Fig.4), which is a remarkable improvement of the device. The electric field in the junction near the drain shift to the drift substrate junction (Fig.5) and permits a higher drain voltage before breakdown occurs.

II.1.5 Drain Characteristics

Drain current is plotted again drain voltage for V_{GS}=3 Volt and V_{GS}= 10 Volt. For lower V_{GS} values, the difference between the two curves is not very distinct, but for greater V_{GS} values, the drain current for LDMOS is low due to the on-resistance.

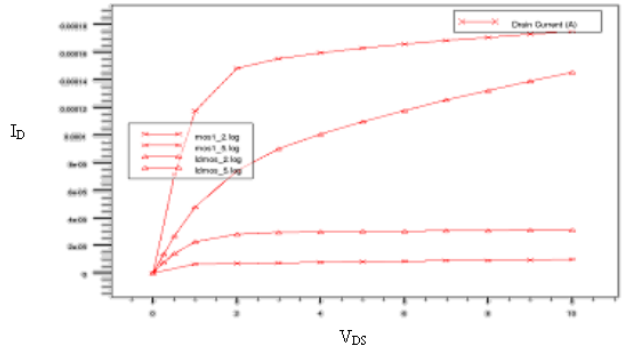

Fig. 7: Drain characteristics.

It can be seen that the output resistance decreases at high drain voltage due to the onset of impact-ionization. The non-linear increase in drain current is due to the channel length modulation.(Fig.7)

II.2 Mixed Mode Analysis

II.2.1 Switching Speed

The switching speed is given by:

$$f_m = \frac{g_m}{2\pi C_G} \qquad (7)$$

The switching speed [20] is expected to improve in the LDMOS device due to its smaller Q_{GD} as compared to the conventional device. The improvement of switching speed in the LDMOS has been calculated using an inverter configuration using mixed-mode simulation of the ATLAS device simulator. The device width has been kept at 15 μm for both the devices. This feature can be seen from the transient analysis of both the inverters (Fig.6).

II.2.2 Power Dissipation

As the threshold voltages are same for both the devices (2.1 Volt), the output voltages change from higher logic level to lower logic level at the same input voltage. The only difference between these two curves is that LDMOS curve shows a higher low logic value at the on-state. It is due to the higher on-resistance of the device and causes high power dissipation [21] at the on-state .The power dissipation is given by:

$$P = I^2 R \ . \qquad (7)$$

R_{on} increases due to the drift-region giving rise to higher power-dissipation as shown in Fig. 8.

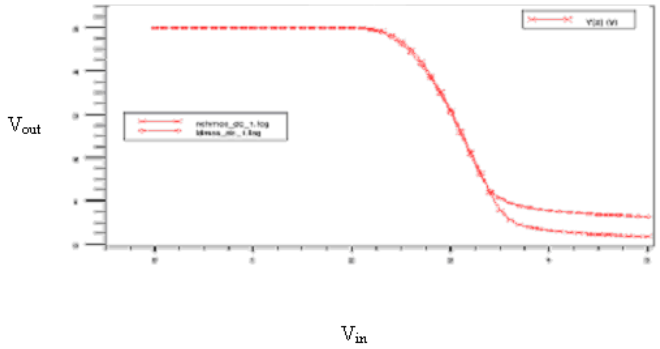

Fig. 8: Inverter output in DC analysis

II.2.3 Gate-Charging Transient

The total gate capacitance (C_G) plays an important role in deciding the maximum switching speed as it decides the time required to turn on and off the transistor.

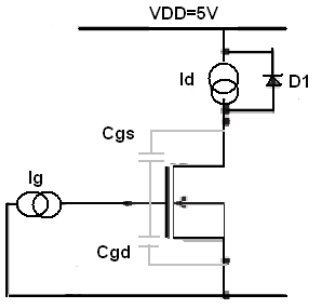

Fig. 9: Test Circuit.

The C_G is constituted of the gate-to-source capacitance (C_{GS}) and the gate-to-drain capacitance (C_{GD}). The capacitive coupling of the gate with the source, i.e., C_{GS}, should be high to get high transconductance, as it is indicative of the gate control of the channel charge. On the other hand,

the capacitive coupling of the gate with the drain, i.e., C_{GD} should be small for improving switching speed as C_{GD} works as miller capacitance .In this simulation both the devices show same C_{GS}, but LDMOS shows lower C_{GD} as compared to the conventional device (Fig.10).

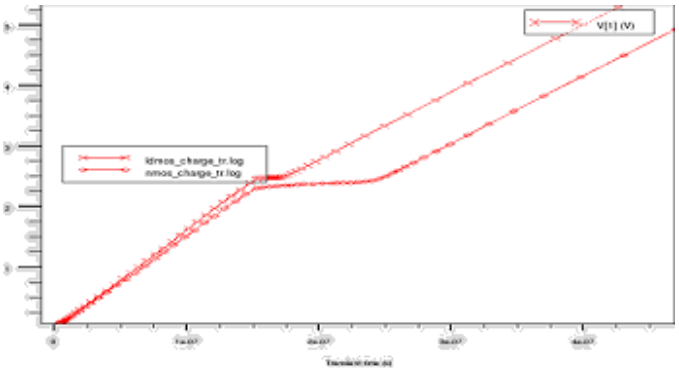

Fig. 10:Overlay of both the curves for comparison.

Here, C_{GS} can be expressed as [22]

$$C_{GG} = \frac{dQ_G(V_G,V_K,V_S,V_B)}{dV_{GS}}$$

$$= \frac{\partial Q_G(V_G,V_K,V_S,V_B)}{\partial V_G} + \frac{\partial Q_G(V_{GS},V_K,V_S,V_B)}{\partial V_K}\frac{dV_K}{dV_G}$$

$$= C_{GG(LDMOS)} - C_{GD(LDMOS)}\frac{dV_K}{dV_G} \qquad (8)$$

Here V_K is the intrinsic drain potential (the point where LDMOS meets the drift region in high voltage devices). To study these effects, we have performed the gate-charging-transient analysis using mixed-mode simulations in ATLAS device simulator. We have connected a 100-μA constant current source at the gate of both the devices and studied the resulting changes in the gate-to-source voltages (V_{GS}) as shown in Figs. 11 and 12.

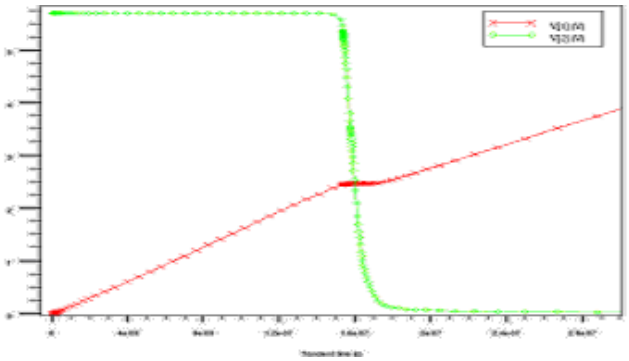

Fig. 11: Gate charging Transient for LDMOS.

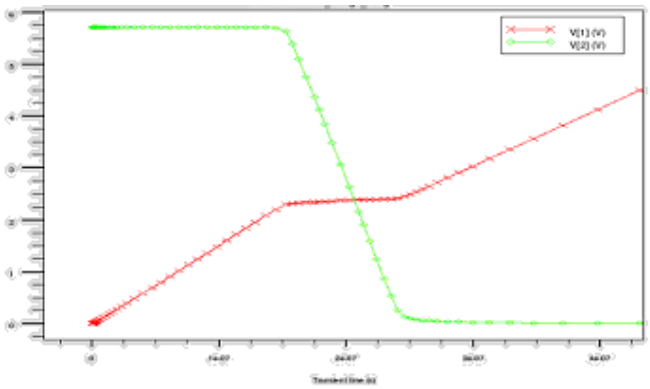

Fig. 12: Gate charging Transient for conventional MOS.

The circuit configuration used in our simulation is also shown in of Fig. 8. The device width has been kept at 10,000 μm for both the devices in this simulation. The initial part of the curve (until the slope changes) represents the charging time of C_{GS}. The subsequent smaller slope region indicates the time required to charge C_{GD}. The charging time multiplied by the constant current forced into the gate terminal gives the amount of charge being injected into the gate.

The LDMOS device, which amounts to about 33% of the Q_{GD} in the conventional device, shows a 198% improvement over the switching speed as compared to that of the conventional device.

II.3 Hot Electron Effect

Device degradation [23-29] is a severe constraint for the long-term stability of modern VLSI circuits. Keeping the power supply at 5 Volt and continuously shrinking the device feature size leads to an increase in the electrical fields in the device. This gives extremely high fields for certain bias conditions in the drain region of the MOSFET (metal-oxide-semiconductor field-effect transistors) and, for special structures, in the source region. There is in general agreement that the observed drain current degradation is due to some localized charges caused by hot-carrier injection in the high-field regions.

In the past decade, the dimensions of devices used in modem integrated circuits have been scaled aggressively to meet the demands for

higher densities and faster operation. However, the power-supply voltages have not scaled proportionately due to restrictions placed by issues such as compatibility with previous technologies, physical limits on the threshold voltage, noise margins, and manufacturability constraints. This disproportionate scaling gives rise to high lateral electric fields in MOSFETs under normal circuit operation. Such high fields result in energetic carriers that can overcome the Si-$Si0_2$ energy barrier and be injected into the gate oxide. The injected carriers can be trapped at defect sites in the oxide and /or create interface traps that cause a change in the electrostatic potential and field distribution in the device under normal operation. This can result in significant changes in the electrical characteristics of the device such as the threshold voltage, transconductance, and the drain current.

Atlas device simulation is performed to gain insight into device degradation characteristics under stressed condition for different time period for both Laterally double-diffused MOS (LDMOS) transistors and MOS, and the hot-electron stress effects have been studied.

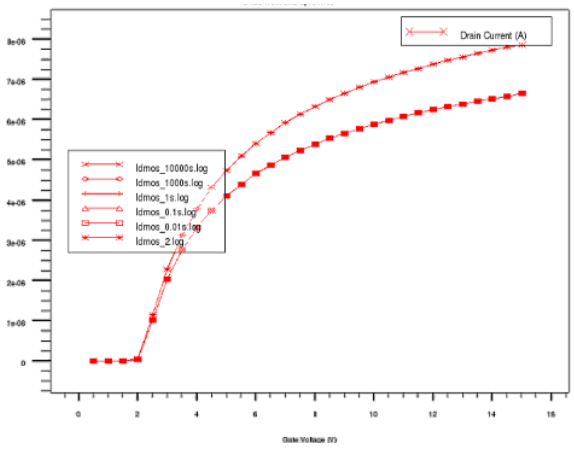

Fig. 13: Hot electron effect on LDMOSFET showing minimal change on threshold voltage.

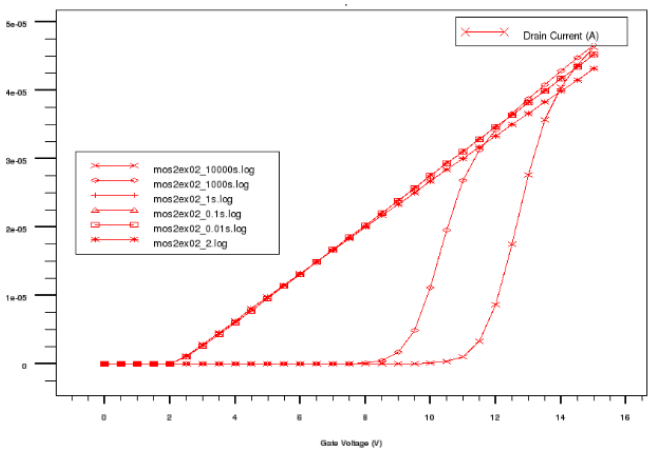

Fig. 14: Hot electron effect on MOSFET showing drastic change on threshold voltage.

The measured threshold voltage of LDMOS transistors is changing much less compared to that of MOS, as shown in Fig.13 and Fig.14. This shows that under the same stress condition, the degradation is much less for LDMOS.

II.4 Impact Ionization

Impact ionization [29] is the process in a material by which one energetic charge carrier can lose energy by the creation of other charge carriers. For example, in semiconductors, an electron (or hole) with enough kinetic energy can knock a bound electron out of its bound state (in the valence band) and promote it to a state in the conduction band, creating an electron-hole-pair.

If this occurs in a region of high electrical field then it can result in avalanche breakdown. In a device the original charge carrier is created by the absorption of a photon. In some sense, the impact ionization is the reverse process to Auger recombination. For n-channel MOSFET, the impact ionization takes place at the junction of substrate and drain region. As voltage is applied at the drain region, the avalanche breakdown occurs for a very low voltage.

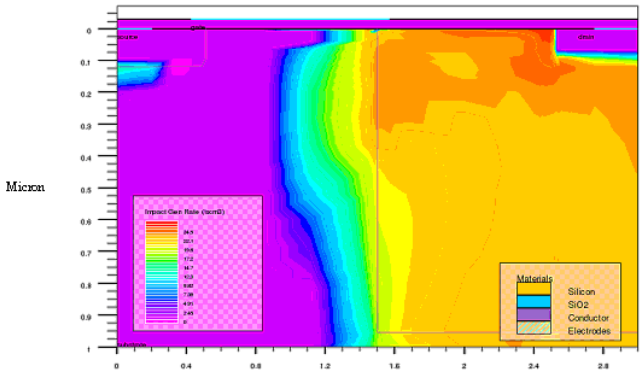

Fig. 15: Impact ionization at n-drift=1.1e-16.

However, for LDMOS, the impact ionization occurs at the junction of drift region and substrate, which is away from the drain region (as shown in Fig.15). For this reason, this device shows a higher breakdown-voltage.

III. CONCLUSION

A numerical comparison of both the devices shows that LDMOS device is better than conventional nMOS device in terms of breakdown voltage and switching speed but at the expense of higher on-resistance and lower g_m. The breakdown voltage increases by 280%. On-resistance also increases by 75%. Value of Transconductance gets reduced by 84%. Switching speed improves by 198%.

It has been observed that there is a remarkable improvement in breakdown voltage and switching speed of the device as compared to the small degradation in on-resistance. Hence, this device can be used as a good switch. However, to be used as an amplifier, the conventional LDMOS device should require further modification, as transconductance value is low.

Acknowledgements

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