Journal of Electron Devices, Vol. 14, 2012, pp. 1118-1121

© JED [ISSN: 1682 -3427]

Journal of Electron Devices
www.jeldev.org

100 nm-GATE LATTICE-MATCHED InAlN/AlN/GaN HEMT FOR HIGH POWER Giga Hertz FREQUENCY APPLICATION

Shah Mohammad Bahauddin*, Md. Akhlak Bin Aziz, Zahid Hasan Mahmood
Department of Applied Physics, Electronics & Communication Eng., University of Dhaka, Dhaka-1000, Bangladesh.
Bahauddin_omar@hotmail.com

Received 01-05-2012, online 09-05-2012

ABSTRACT

The InAlN/GaN heterojunction appears to be a promising alternative both in technology and performance to its common AlGaN/GaN configuration. The heterostructure opens up possibility of scaling down to 7 nm barrier with submicron gate length while maintaining higher power and frequency performance as well. In this paper, we have reported 100-nm gate configuration to reach record performance from polarization induced InAlN lattice-matched heterostructure. Simulation results show that maximum drain current of 2.5 A/mm with a transconductance of approximately 600 mS/mm and gain cut-off frequency of 154 GHz can be achieved from the designed HEMT.

I. INTRODUCTION

Increasing demand for high power amplification at GHz frequency in communication, weapon detection and other commercial applications has lead AlGaN/GaN heterostructure under an extensive study which was considered ideal option for high frequency high power application [1]. However, theoretical predictions suggested that InAlN/(In)GaN HEMT performance can be superior compared to AlGaN/GaN, mainly because of its lattice matched strain-free interfacial channel which has significantly higher spontaneous polarization induced two dimensional electron gas with an attractive 2DEG mobility [1].

Despite the outstanding performance demonstrated by AlGaN/GaN HEMTs in the last decade, a serious lack of reliability issue of AlGaN-GaN HEMT arises as the lattice defects introduced by the stress resulting from the piezoelectric effect worsens interfacial electron gas mobility and crystal stability [2]. It is seen from the composition diagram in fig. 1 that by replacing AlGaN barrier with InAlN on GaN, the stress and its resulting piezo-polarization can be obliterated. Other than piezo-polarization, due to the higher polarization discontinuity, the 2DEG-channel sheet charge density induced by the difference in spontaneous polarization is larger in InAlN/GaN than AlGaN/GaN heterostructure; resulting in a higher output current density along with channel mobility [1]. Furthermore, gate length lower than 0.2 μm is not possible in conventional AlGaN/GaN based structures without exploiting short channel effects [3] while high Al content (83%) in InAlN pushes InAlN closer to AlN that results a surface potential pinned at a level of 0.4 eV[3] which is very favourable to grow extremely thin barrier (<20 nm) while keeping a very high sheet carrier density. Unlike AlGaN/GaN devices, the lattice matched InAlN/GaN heterostructure is chemically extremely stable showing no degradation of Ohmic or Schottky contact even at 1000°C[3]. The material properties thus promises that HEMTs based on lattice matched InAlN/GaN should provide more robustness and thermal stability and exhibit record performance superior to its AlGaN counterpart.

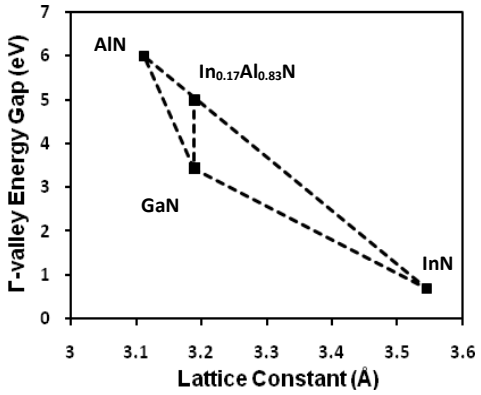

Figure 1: Variation of Energy Bandgap with Lattice Constant for (Al,In)GaN based heterostructure matrix.

Significant advancements have been achieved in past few years of the InAlN/GaN heterostructure growth technology by MOCVD demonstrating expected high sheet carrier density with high mobility[4]. Initial reports for AlInN/GaN HEMTs on sapphire or SiC substrates have confirmed the high current derivability of the device [3]. In principle, the use of thin barrier layer while maintaining high L_G/d channel aspect ratios should enable the device to operate at high power high frequency region while minimizing short-channel affects. To date, the highest published f_T for InAlN/GaN HEMT was 144 GHz [5] with 8 nm barrier and fully passivated 100 nm gate on semi-insulating SiC. Recently Han Wang et al. have demonstrated HEMT structures with drain-current density 2.5 A/mm with 100 nm gate length and a transconductance of 690 mS/mm with 150 nm of gate length on SiC substrate after

recessing the gate to achieve 3 nm gate-to-channel separation [6].

In the present work, we have theoretically studied the scaling behavior on the performance of 100-nm-gate InAlN/GaN HEMTs grown on SiC substrate for RT operation. Numerical simulation was performed to investigate maximum drain-current-density with operational bandwidth as well as transconductance which exhibited potential results for higher power density in GHz frequency regime.

II. DEVICE STRUCTURE

The gate length of reported HEMT structure is 100 nm with gate width Z = 50 μm and source-to-drain distance L_{DS} = 1 μm. For contact metal, conventional Ti/Al/Ni/Au is used with a Schottky barrier height of 0.63 eV. 7.5 nm thick InAlN barrier layer is grown to attain high drain current and transconductance with an optimum breakdown voltage. Surface passivation is used to remain the contact resistance less than 0.5 Ω.mm using Al_2O_3 atomic layer deposition. The structure possesses a 1-nm AlN spacer layer as the insertion of interlayer dramatically reduces the scattering of 2DEG and alloy related interfacial roughness [7]. Conventional AlN nucleation layer on SiC substrate is used as it is ideal for such device fabrication[13]. Technological and material parameters used for hypothetical device modeling is shown in table 1[8].

Table 1: Material parameters

Material Parameters	$In_{0.17}Al_{0.87}N$
Effective Mass, $m^*(z)$	0.3
Energy band gap, E_g(eV)	5.1
Cond. band discontinuity ΔE_C(eV)	0.3
Dielectric Const. ε_0	9.8
Mobility, μ (cm^2/Vs)	1300
Saturation Velocity, v_s (cm/s)	1.2 x 10^7

Performance of reported HEMT structure is verified by numerical solutions which account the polarization-induced charge to calculate the HEMT current-voltage characteristics. First polarization-induced charge is integrated into the calculation of threshold voltage by using the analytical expression,

$$V_T = \varphi_B - \Delta E_C - qdP^{SP}_{total} \Big/ \varepsilon_{InAlN} \quad (1)$$

where φ_b is the Schottky contact barrier height, d is the barrier thickness and ΔE_C is the conduction band discontinuity. Since InAlN layer is considered to be undoped, there is no voltage required for depleting the doped part and hence such terms are not present in above equation. In order to quantify V_T, we need to calculate the spontaneous polarization of barrier material using the numerical interpolation of GGA values [8] which is given by,

$$P^{SP}_{Al_xIn_{1-x}N} = -0.09x - 0.042(1-x) + 0.071x(1-x) \quad (2)$$

Now by neglecting diffusion contributions, the drain-source current is given by

$$I_{DS} = qZv(x)n_s(x) \quad (3)$$

where v(x) is the electron mean velocity assumed to be independent on z-direction. The dependence of the drift velocity on the longitudinal electric field is empirically given by[8]

$$v = \frac{\mu F(x)}{1 + \mu F(x) \Big/ v_{sat}} = \frac{\mu F(x)}{1 + \frac{F(x)}{F_C}} \quad (4)$$

Next the output characteristics of the HEMT can be calculated by the numerical solution in InAlN/AlN/GaN region. The simulation is based on the finite discretization of the current-voltage expression and solving iteratively for all the sections at x-direction.

$$I_{DS} = qZ \frac{\mu F_i}{1 + \frac{F_i}{F_C}} n_s(V_G - V_{i-1} - F_i h) \quad (5)$$

For suitable range of values of I_{DS}, a set of corresponding values of V_{DS} is obtained by calculating the sheet charge density with corresponding electric field. The 2DEG density is also numerically derived from the self-consistent Schrödinger-Poisson iteration method

$$n(V_G, z) = \frac{m^*(z)k_BT}{\pi\hbar^2} \sum_{i=0}^{m} \left|\psi_m(V_G, z)\right|^2 \ln\left[1 + e^{\frac{E_F - E_m}{k_BT}}\right] \quad (6)$$

The sheet charge concentration in the channel is obtained by integrating the 2DEG density distribution along the z-direction,

$$n_s(V_G) = \int n(V_G, z)dz \quad (7)$$

The quasi-2D Self-consistent finite difference charge control model presented above is performed for several gate biases to obtain HEMT DC characteristics.

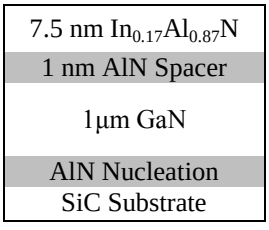

Figure 2: 100-nm gate-InAlN/GaN HEMT with AlN interlayer as spacer and nucleation. The growth direction is along z-axis.

III. DEVICE PERFORMANCE

The output and transfer characteristics of the modeled HEMT using the material and geometrical values are given in fig 3 and fig 4. The calculations were performed from $V_{GS(threshold)}$=-3.3V to V_{GS} = +2V. We have assumed that the maximal reachable drain current will be achieved at V_{GS} = +2V and further channel opening should be avoided which will cause thermal runaway resulting large power dissipation. Calculated I-V characteristics show a maximum drain current of 2.5 A/mm with a transconductance of approximately 600 mS/mm. However the characteristic curve at saturation shows no sign of negative resistance or current collapse phenomena since our analytical model does not cover all practical aspects such as gate leakage current, self-heating on HEMT performance.

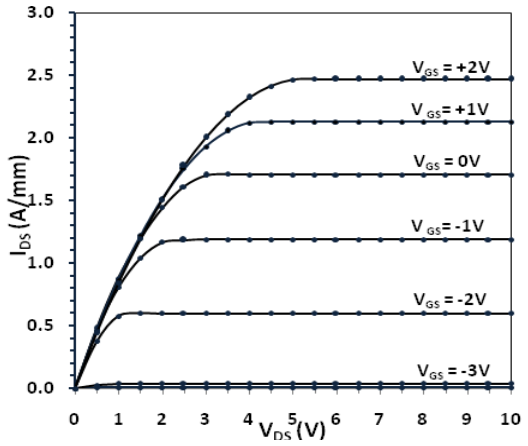

Figure 3: Simulated Drain current characteristics of proposed HEMT measured from V_{GS} = -3 V to +2 V, in steps of +1 V.

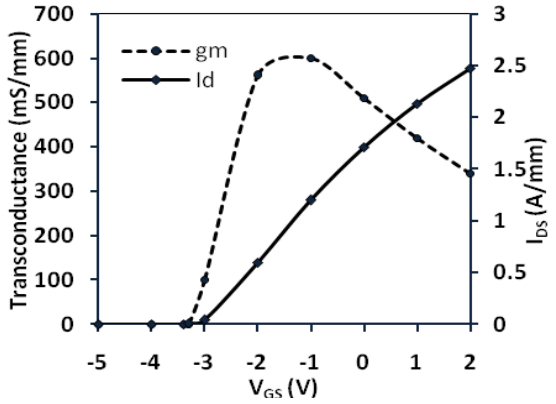

Figure 4: Transfer characteristics of simulated structure showing a maximum transconductance of 600 mS/mm.

The transit time under the gate of a submicron HEMT is a crucial parameter for HEMT microwave performance as the current gain cut-off frequency is the figure of merit to gauge the expected high frequency performance. It is defined as the frequency, at which the current gain goes to unity and conventionally expressed as,

$$f_T = \frac{g_m}{2\pi(C_{GS} + C_{GD})} \approx \frac{v_{sat}}{2\pi L} \quad (8)$$

where C_{GS} and C_{GD} are the gate-source capacitance and gate-drain feedback capacitance respectively. We have neglected feedback capacitance and used the extrinsic transconductance which lead us to a gain cut-off frequency of 154 GHz, which is by far, the highest f_T for any reported submicron (In,Al)GaN-GaN HEMT.

IV. CONCLUSION

In summary, we have investigated the design space of submicron InAlN/GaN HEMT with 7.5 nm barrier layer and numerical modeling shows that the new structure should exhibit drain-to-source current of 2.5 A/mm as well as transconductance of 600mS/mm. Theoretical calculation also predicts that a record cutoff frequency greater than 150 GHz is potentially possible with this structure. Recent experimental reports have concurred with our theoretical design leading InAlN/GaN HEMT to an attractive alternative for high power high frequency application.

References

1. J. Kuzmik, "Power Electronics on InAlN/(In)GaN: Prospect for a Record Performance," IEEE Electron Device Letters, **22**, 510-512, (2001)
2. J. Joh and J. A. del Alamo, "Mechanism for Electrical Degradation of GaN High Electron Mobility Transistor," International Electron Device Meeting (IEDM '06), 1-4, (2006)
3. F. Medjdoub, J. F. Carlin, C. Gaquiere, N. Grandjean and E. Kohn, "Status of the Emerging InAlN/GaN Power HEMT Technology," The Open Electrical and Electronic Engineering Journal, **2**, 1-7, (2008)
4. D. Xun, L. Zhong-Hui, L. Zhe-Yang, Z. Jian-Jun, L. Liang, L. Yun, Z. Lan, X. Xiao-Jun, X. Xuan and H. Chun-Lin, "Effects of AlN and AlGaN Interlayer on Properties of InAlN/GaN Heterostructures," Chin. Phys. Lett. **27**, 037102 (2010)
5. H. Sun, A. R. Alt, H. Benedickter, E. Feltin, J. F. Carlin, M. Gonschorek, N. Grandjean, C. R. Bolognesi "100-nm-Gate (Al,In)N/GaN HEMTs Grown on SiC with F_T=144 GHz," IEEE Electron Device Letter, **31**, 293-295 (2010)
6. H. Wang, J. W. Chung, X. Gao, S. Guo and T. Palacios, "High Performance InAlN/GaN HEMTs SiC Substrate," The International Conference on

Compound Semiconductor Manufacturing Technology (CSManTech 2010) (2010)
7. D. D. Koleske, R. L. Henry, M. E. Twigg, J. C. Culbertson, S. C. Binari, A. E. Wickenden and M. Fatemi, "Influence of AlN Nucleation Layer Temperature on GaN Electronic Properties grown on SiC," Appl. Phys. Lett, **80**, 4372 (2002).
8. C. Wood and D. Jena, "Polarization Effects in Semiconductors," Springer Science, 2008.