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MATHEMATICAL MODELING OF BANDWIDTH AND POWER IN HIGH SPEED VLSI RLC INTERCONNECT WITH SKIN EFFECT

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ABSTRACT As the interconnect technology is shrinking into nanometres regime the bandwidth of long interconnects reduces. Hence an accurate modelling of bandwidth is essential for the estimation of performance of VLSI interconnects. With the increase in frequency towards the giga hertz range, the analysis of high frequency effects like skin effect etc. are becoming extensively predominant and important for high speed VLSI design. Skin effect attenuates the high frequency components of a signal more than that of the low frequency components. This paper strives to reflect the need for considering skin effect while modelling bandwidth for any interconnect segment. This paper presents a mathematical modelling of the bandwidth and power in an RLC interconnects with and without skin effect. In this paper noise dependence on the temperature is also discussed in VLSI on-chip RLC interconnect under the influence of ramp input.

Keywords: VLSI, RLC line, Interconnects, Skin effect, Power, Bandwidth.

I. INTRODUCTION

System designers of high-end integrated circuits face complex designs involving tens or hundreds of millions of transistors and the enormous task of connecting these circuits seamlessly together. As integrated circuit feature sizes continue to scale well below 0.18 microns, active device counts are reaching hundreds of millions [1]. The amount of interconnect among the devices tends to grow super linearly with the transistor counts, and the chip area is often limited by the physical interconnect area. Several factors bound to the technology contribute to the bandwidth problems. Bandwidth has a key role in the performance of any circuit basically used for data transmitting applications. Each on-chip memory controller found to be effective in reducing interconnects delays also supports outstanding transactions to complete out-of order with respect to the original request order. This feature enables the memory banks in the system to service requests as soon as a bank is available, maximizing bandwidth utilization. Because most accesses to memory are predominantly reads, the memory interface also gives priority to reads over writes, another feature that maximizes bandwidth utilization. A higher bandwidth reduces the total time required to transmit a certain amount of data, thereby increasing the performance of the system. A bit period can be divided into two parts [2]. In most available electronic design automation (EDA) tools, interconnects are modeled as RC components [3]. However, many high frequency effects of the interconnects, such as the inductive effect, skin effect, distributed effect, substrate effect, etc., have become non-negligible in gigahertz applications [4]. Therefore, the existing RC model becomes insufficient. Hence RLC models have been exploited. As the technology has started working on the high frequencies high frequency effect like skin effect and proximity effects has become significant. The reason behind the importance of considering such effect is that, these effects affects the system integrity at large scale. For integrated circuits in the deep submicron (DSM) technology, interconnects play an important role in determining the performance and signal integrity [5,6]. An efficient on-chip interconnect analysis is critical to interconnect optimization at high-level design, logic synthesis and physical design, as circuit simulation is overkill and not affordable at these design stages. Closed-form formulae are particularly efficient and effective for these design stages. Previous works include formulae for delay, noise [7, 8].

II. BASIC THEORY

As the number of transistors per GSI chip increases, the total length of wires on chip also increases. For high-performance chips, these wires are routed in several different tiers. Based on their length (and pitch sizes), the wires can be separated into local, intermediate, and global wires. Local wires connect gates and transistors within a functional block and are usually routed in the minimum pitch and occupy the first two metal levels of a multilevel interconnect network. The lengths of these wires are usually less than a few gate pitches so their length scales down with the technology. Intermediate wires provide clock and signal distribution within a functional block or inter-module communications between adjacent blocks with typical lengths up to $3\sim4$ mm. Global wires provide clock and signal distribution between functional blocks and deliver power/ground to all functions on a chip. Global wires that are

routed in the top metal levels are longer than 4mm and can be as long as the chip size. As the length of global wires does not scale down with the technology, the overall performance of the interconnect network can become dominated by global wires. The insertion of repeaters can mitigate this problem but is not enough. In addition, reverse scaling of global and intermediate wires is necessary [9]. Typical interconnect length distribution and a chip cross-section using reverse scaling for its multi-level interconnect network are shown in Figure 1.3. Knowing the wiring distribution to estimate the interconnect lengths a priori [10,11], the reverse-scaled multilevel interconnect networks can be optimized to reduce the logic macro-cell area, cycle time, power consumption, or number of metal levels [12].

High frequency interconnects for data and clock distribution and RF applications are a crucial component of all high performance electronic circuits. In recent years, increasing bandwidth requirements have led to research into low-loss on-chip interconnects, which theoretically can achieve very high bandwidth [13]. However, in the multi-gigahertz frequency range, skin effect causes current to flow only at the surface of conductors, leading to a decrease of wire inductance and an increase of resistance. The latter effect causes a signal attenuation which increases with frequency, thus limiting the available interconnect bandwidth. Despite the technological impact of the skin effect, published models are mostly limited to traditional wire structures such as coaxial cables. For on-chip and on-board applications, it is important to be able to estimate the effect for single wires rather than complete transmission lines, and with a rectangular rather than circular cross-section. In particular, wires with high aspect ratios (width-to-height) are employed to reduce losses when the metal thickness is limited by technological considerations. Several numerical codes have been developed to compute current distributions in wires of any shape and arrangement [14,15, 16, 17, 18]. Empirical fits of the frequency-domain wire resistance have also been presented [19], but their use in time-domain simulation requires an additional network realization step.

This is a well know fact that propagation delay increases with the skin effect in an on-chip interconnect. Skin effect will also affect the optimality of the system. The skin effect can be represented at the circuit level as a combination of frequency dependent resistance and inductance. However, frequency dependent circuit elements are not suitable for time-domain analysis, therefore a circuit representation based on frequency independent elements is desirable [20]. When a transmission line model is necessary, either a Spice-compatible distributed RLC model is used or else a full transmission line model is needed. Which is chosen depends on the accuracy needed and also the capability of an available circuit simulation program[21]. A range of models are used for interconnects depending on:

1) The accuracy required nets carrying analog signals need to be modelled more
2) The amenability of the net to modelling.
3) The frequency of operation.

Short on-chip interconnects are commonly modelled as RLC networks where the inductor and capacitor networks are arrived at separately using static calculations of the effect of very small segments of interconnect on other small segments. Uniform interconnects (with regular cross-section) can be modelled by determining the characteristics of the transmission line, e.g. Z_0 and y versus frequency, or arriving at a distributed lumped element circuit.[21].Since the frequency dependent behaviour is easy to compute and observe, in any circuit ,consisting of frequency dependent components skin effect modelling can be performed.

The "Skin Effect" is the tendency of high frequency current to concentrate near the outer edge, or surface, of a conductor, instead of flowing uniformly over the entire cross sectional area of the conductor. The higher the frequency, the greater the tendency for this effect to occur. There are three possible reasons we might care about skin effect. The resistance of a conductor is inversely proportional to the cross sectional area of the conductor. If the cross sectional area decreases, the resistance goes up. The skin effect causes the effective cross sectional area to decrease. Therefore, the skin effect causes the effective resistance of the conductor to increase. The skin effect is a function of frequency. Therefore, the skin effect causes the resistance of a conductor to become a function of frequency (instead of being constant for all frequencies.) This, in turn, impacts the impedance of the conductor. If we are concerned about controlled impedance traces and transmission line considerations, the skin effect causes trace termination techniques to become much more complicated. If the skin effect causes the effective cross sectional area of a trace to decrease and its resistance to increase, then the trace will heat faster and to a higher temperature at higher frequencies for the same level of current [22]. There are a number of approaches available where the on-chip interconnect is modelled as distributed RLC segments for accurate performance parameters modelling [23-27]. But these models do not consider the high frequency skin effect phenomena.

This paper is divided into three sections. First section provides a mathematical modelling of bandwidth with and without considering the skin effect. Hence a closed formula for bandwidth calculation is obtained. In the second section mathematical modelling of power is done under ramp input. Third section provides the noise produced in the influence of the temperature which is raised due to the working of the interconnect with and without skin effect.

III. PREVIOUS WORK

III.1 Crosstalk modelling of RLC interconnect analysis without skin effect

In the previous paper we have analyzed the delay and crosstalk formula under ramp input response. This analysis considers the following interconnect coupling circuit Fig 1. The noise analyzed in the previous paper is given below [7]

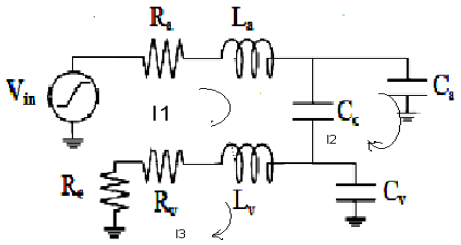

Figure 1: Analytical Model of RLC interconnect

Now applying the simple loop analysis, the following equations are obtained in terms of RLC:

For first loop:

$$V_{in}(t) = I_1(t).R_a + L_a.\left(\frac{d}{dt}I_1(t)\right) + \frac{1}{C_c}\left[I_1(t) - I_2(t)\right] \quad (5)$$

For second loop:

$$\frac{1}{C_c}[I_2(t) - I_1(t)] - \frac{1}{C_a}I_2(t) = 0 \quad (6)$$

For third loop:

$$R_e I_3(t) + R_v \cdot I_3(t) + L_v \cdot \frac{d}{dt}(I_3(t)) + \frac{1}{C_c} \cdot I_3(t) = 0 \quad (7)$$

Taking Laplace Transform of (5)- (7), the following equations are obtained:

$$V_{in}(s) = I_1(s)R_a + sL_aI_1(s) + \frac{[I_1(s) - I_2(s)]}{sC_c} \quad (8)$$

$$\frac{1}{sC_c}[I_2(s) - I_1(s)] - \frac{1}{sC_a}I_2(s) = 0 \quad (9)$$

$$R_eL_3(s) + R_vI_3(s) + sL_vI_3(s) + \frac{1}{sC_v}.I_3(s) = 0 \quad (10)$$

From (9), the following can be derived:

$$\left[\frac{1}{sC_c} - \frac{1}{sC_a}\right]I_2(s) = \frac{1}{sC_c}I_1(s) \quad (11)$$

Or (12)

$$I_2(s) = \frac{I_1(s)}{sC_c\left(\frac{1}{sC_c} - \frac{1}{sC_a}\right)}$$

So, (13)

$$I_2(s) = I_1(s)\left(\frac{C_a}{C_a - C_c}\right)$$

From equation (8),

$$V_{in}(s) = I_1(s).R_a + sL_aI_1(s) + \frac{1}{C_c}I_1(s) - \frac{1}{C_c}I_1(s).\frac{C_a}{C_a - C_c} \quad (14)$$

Or, (15)

$$V_{in}(s) = I_1(s)\left[R_a + sL_a + \frac{1}{C_c}\left(1 - \frac{C_a}{C_a - C_c}\right)\right]$$

So, (16)

$$I_1(s) = \frac{V_{in}(s)}{R_a + sL_a + \frac{1}{C_c}\left(1 - \frac{C_a}{C_a - C_c}\right)}$$

With the simple loop analysis it can be found that

$$I_3 = |I_1 - I_2| \quad (17)$$

Therefore, using I_1 and I_2 , the third current can be derived which is given as:

$$I_3(s) = \frac{V_{in}(s)C_c}{R_a + sL_a + \frac{1}{C_c}\left(1 - \frac{C_a}{C_a - C_c}\right)(C_a - C_c)} \quad (18)$$

Applying the current divider rule, the current in the victim line capacitor may be found. This finally yields to,

$$I_x = I_3\frac{R_2}{R_1 + R_2} \quad (19)$$

where $R_1 = (R_e + R_v + sL_v) or, R_2 = \frac{1}{sC_v}$

$$I_x = \frac{V_{in}(s)C_c}{R_a + sL_a + \frac{1}{C_c}\left(1 - \frac{C_a}{C_a - C_c}\right)(C_a - C_c)} \times \frac{R_e + R_v + sL_v}{R_e + R_v + sL_v + \frac{1}{sC_v}} \quad (20)$$

The output voltage is given as,

$$V_{co}(s) = I_x \times \frac{1}{sC_v} \quad (21)$$

From (20) and (21) we have,

$$V_{co}(s) = \frac{V_{in}(s)}{sC_v}\left[\frac{C_c(R_e + R_v + sL_v)}{\left(R_a + sL_a + \frac{1}{C_c\left(1 - \frac{C_a}{C_a - C_c}\right)}\right) \times \left(R_e + R_v + s\left(L_v + \frac{1}{s^2C_v}\right)\right) \times (C_a - C_c)}\right] \quad (22)$$

Some important assumptions that have been made in this paper are as follows:

$$R_e + R_v = A$$

$$R_a + \frac{1}{C_c}\left[1 - \frac{C_a}{C_a - C_c}\right] = B \quad (23)$$

For ramp input, $V_{in} = \frac{V_0}{s^2}$ (24)

Hence the crosstalk is given as:

$$V_{co}(t) = \frac{V_0}{(C_a - C_c)}(\alpha_1 + \beta_1 + \chi_1 + \kappa_1 + \zeta_1) \quad (25)$$

where,

$$\alpha_1 = \left(\frac{C_c\left(A - \frac{B}{L_a}.L_v\right).L_v}{\left[A + 1 - \frac{B}{L_a}.L_v\right] \cdot \left[-\frac{B}{L_a}\right]^3} + \frac{C_c.L_a}{\left[B - (A+1).\frac{L_a}{L_v}\right] \cdot \left[\frac{1+A}{L_v}\right]^3}\right)u(t)$$

$$\beta_1 = \left[\frac{C_c.L_v}{B.(A+1)} - \frac{C_c.A(B.L_v + L_a + A.L_a)}{[(1+A).B]^2}\right]t.u(t)$$

$$\chi_1 = \frac{1}{2}\left[\frac{C_c.A}{(1+A).B}.t^2\right].u(t)$$

$$\kappa_1 = \frac{C_c\left(A - \frac{B}{L_a}L_v\right)}{\left[(A+1) - \frac{B}{L_a}L_v\right]\left(-\frac{B}{L_a}\right)^3}e^{-\frac{B}{L_a}t}$$

$$\zeta_1 = -\frac{C_c}{\left[B - (1+A)\frac{L_a}{L_v}\right]\left[\frac{A+1}{L_v}\right]^3}e^{-\frac{(1+A)}{L_v}t}$$

Skin effect on resistance can be calculated by using the following equations [7]:

$$R_{total} = R_{DC} + \sqrt{f}\,R_{AC}, \tag{26}$$

where, $R_{DC} = \frac{\rho L}{W.t}$ (27)

$$R_{AC} = \frac{\rho L}{A_{current\_densityar\_area}} = \frac{L\rho}{\omega\sqrt{\frac{2}{\omega\sigma\mu}}} = \frac{L\sqrt{\rho}}{\omega\sqrt{2}}\sqrt{\mu f} \tag{28}$$

Therefore,

$$R = R_{total} = \frac{\rho L}{Wt} + \frac{L\sqrt{\rho}}{\omega\sqrt{2}}.\sqrt{\mu f} \tag{29}$$

.

III.2 Cross talk voltage and delay with skin effect

Thus equation (32) can be used to find the closed form expression of the cross talk noise with skin effect.

$$V_{co}(t) = \frac{V_0}{(C_a - C_c)}\left(\alpha_2 + \beta_2.t + \chi_2.t^2 + \kappa_2.e^{-\frac{B_{skin}}{L_a}t} + \zeta_2.e^{-\frac{(1+A_{skin})}{L_v}t}\right) \tag{30}$$

Where,

$$\alpha_2 = \left(\frac{C_c\left(A_{skin} - \frac{B_{skin}}{L_a}.L_v\right).L_v}{\left[A_{skin} + 1 - \frac{B_{skin}}{L_a}.L_v\right]\cdot\left[-\frac{B_{skin}}{L_a}\right]^3} + \frac{C_c.L_a}{\left[B_{skin} - (A_{skin}+1).\frac{L_a}{L_v}\right]\cdot\left[\frac{1+A_{skin}}{L_v}\right]^3}\right)u(t)$$

$$\beta_2 = \left[\frac{C_c.L_v}{B_{skin}.(A_{skin}+1)} - \frac{C_c.A_{skin}(B_{skin}.L_v + L_a + A_{skin}L_a)}{\left[(1+A_{skin}).B_{skin}\right]^2}\right].u(t)$$

$$\chi_2 = \frac{1}{2}\left[\frac{C_c.A_{skin}}{(1+A_{skin}).B_{skin}}\right].u(t)$$

$$\kappa_2 = \frac{C_c\left(A_{skin} - \frac{B_{skin}}{L_a}L_v\right)}{\left[(A_{skin}+1) - \frac{B_{skin}}{L_a}L_v\right]\left(-\frac{B_{skin}}{L_a}\right)^3}$$

$$\zeta_2 = -\frac{C_c}{\left[B_{skin} - (1+A_{skin})\frac{L_a}{L_v}\right]\left[\frac{A_{skin}+1}{L_v}\right]^3}$$

IV. MODELING OF BANDWIDTH

IV.1 Section one

IV.1.1 Without skin effect

In order to model bandwidth [28]

$$H(S) = \frac{V_2(s)}{V_{in}(s)} = \frac{1}{\sqrt{2}} \tag{31}$$

From equation (22)

$$\left|\frac{1}{\sqrt{2}}\right| = \frac{1}{j\omega C_v}\left[\frac{C_c(R_e + R_v + j\omega L_v)}{(B + j\omega L_a)\left[A + j\omega\left(L_v - \frac{1}{\omega^2 C_v}\right)\right].(C_a - C_c)}\right] \tag{32}$$

$$\left|\frac{1}{\sqrt{2}}\right|^2 = \left(\frac{1}{j\omega C_v}\right)^2\left[\frac{C_c^2\left(\sqrt{(R_e+R_v)^2 + \omega^2 L_v^2}\right)^2}{\left(\sqrt{(B^2 + \omega^2 L_a^2)}\right)^2\left(\sqrt{\left[A^2 + \omega^2\left(L_v - \frac{1}{\omega^2 C_v}\right)^2\right]}\right)^2.(C_a - C_c)^2}\right] \tag{33}$$

$$\omega^2 C_v^2 = \left[\frac{2.C_c^2\left((A)^2 + \omega^2 L_v^2\right)}{\left(B^2 + \omega^2 L_a^2\right)\left(\left[(A^2 + L_v^2) + \frac{1}{\omega^4.C_v^2} - \frac{2L_v}{\omega^2 C_v}\right]\right).(C_a - C_c)^2}\right] \tag{34}$$

$$1 = \left[\frac{2.C_c^2\left((A)^2 + \omega^2 L_v^2\right).\omega^2}{\left(B^2 - 2\omega^2.C_v L_v\right).(C_a - C_c)^2}\right]$$

$$\left(B^2 - 2\omega^2.C_v L_v\right).(C_a - C_c)^2 = 2C_c^2.A^2\omega^2$$

$$\omega^2 = \frac{B^2(C_a - C_c)^2}{2\left[C_c^2 A^2 + C_v L_v\right]}$$

$$f_{-3db} = \frac{B^2(C_a - C_c)^2}{2\pi\sqrt{\left[C_c^2 A^2 + C_v L_v\right]}} \tag{35}$$

IV.1.2 With skin effect

$$(R_e + R_v).\sqrt{f} = A_{skin}$$

$$R_a\sqrt{f} + \frac{1}{C_c}\left[1 - \frac{C_a}{C_a - C_c}\right] = B_{skin}$$

$$f_{-3db}(skin) = \frac{B_{skin}^2(C_a - C_c)^2}{2\pi\sqrt{\left[C_c^2 A_{skin}^2 + C_v L_v\right]}}$$

IV.2 Section two

This section provides the closed form expression for the power in the RLC interconnect under the influence of ramp input.

In order to calculate power such methodology is used [29]

$$V_{out}(x,s) = V_{in}(x,s).A.B \tag{36}$$

where

$$A = \frac{Z_0\sqrt{\left(s + \frac{r}{l}\right)}/s}{\sqrt{\frac{\left(s + \frac{r}{l}\right)}{s}}Z_o + R_v}$$

$$B = e^{-x\sqrt{lc}\sqrt{s\left(s + \frac{r}{l}\right)}}$$

and

$$Z_0 = \sqrt{\frac{l}{c}}$$

is the characteristics impedance. is the characteristic impedance of the transmission line, where r, l, and c are resistance, inductance, capacitance per unit length respectively, $R_{tr}=Z_s=r$ is the driver resistance.

For ramp input

$$V_{out}(s)=\frac{1}{s^2}\left[\frac{Z_0\sqrt{\left(s+\frac{r}{l}\right)/s}}{Z_o\sqrt{\frac{\left(s+\frac{r}{l}\right)}{s}}+R_v}e^{-x\sqrt{lc}\sqrt{s\left(s+\frac{r}{l}\right)}}\right] \quad (37)$$

The current equation [30] in the time domain is given by

$$I(x,t)=-\frac{1}{r}\frac{\partial v(x,t)}{\partial x} \quad (38)$$

$$I(x,s)=-\frac{1}{r}\left[\frac{\sqrt{\frac{l}{c}}\sqrt{(s+\frac{r}{l})/s}}{s^2\left(\sqrt{\frac{l}{c}}\sqrt{\frac{(s+\frac{r}{l})}{s}}+r\right)}e^{-x\sqrt{lc}}(\sqrt{s(s+\frac{r}{l}}(-\sqrt{lc})\sqrt{s\left(s+\frac{r}{l}\right)}\right] \quad (39)$$

Now put the denominator equal to zero in order to find the poles:

$$P_1=0$$

$$P_2=-\frac{r}{lr^2-l}$$

We can consider the second pole because it is in second half of the s-plane.

$$I(x,-P_2)=\left[\frac{\sqrt{lc}.\sqrt{(\frac{r}{lr^2-l}+\frac{r}{l})/\left(\frac{r}{lr^2-l}\right)}}{r\left(\frac{r}{lr^2-l}\right)^2\left(\sqrt{\frac{(\frac{r}{lr^2-l}+\frac{r}{l})}{\frac{r}{lr^2-l}}}\right)+r^2\left(\frac{r}{lr^2-l}\right)^2}e^{-x\sqrt{lc}}(\sqrt{\left(\frac{r}{lr^2-l}\right)\left(\left(\frac{r}{lr^2-l}\right)+\frac{r}{l}\right)}\right] \quad (40)$$

From the above equation the residue of I(x,-pole) can be find out.

$$\hat{r}_2=\lim_{s\to p_2}(s-p_2)I(x,s) \quad (41)$$

And then the closed form for the power dissipation can be find out using the following formula

$$E(x)=r\times residue\times I\left(x,-P_2\right) \quad (42)$$

Under the influence of the skin effect the resistance r will increase with a factor of square root of the frequency. Hence if the frequency increases the power dissipation will increase.

$$E(x)=r_{skin}\times residue\times I\left(x,-P_2\right) \quad (43)$$

IV.2 Section three

This section presents the output noise observed. Circuit shown in the figure 2 is simulated and by performing the temperature analysis the change in the noise level at the output is observed with and without skin effect. The values of R,L,C are taken from the semiconductor roadmap for .18 µm technology.

Table 1: RLC parameters for a minimum- sized wires in a0.18µm technology.

Parameter(s)	Value/m
Resistance(R)	120 kΩ/m
Inductance(L)	270 nH/m
Capacitance(C)	240 pF/m
Coupling Capacitance(C_c)	682.49 fF/m

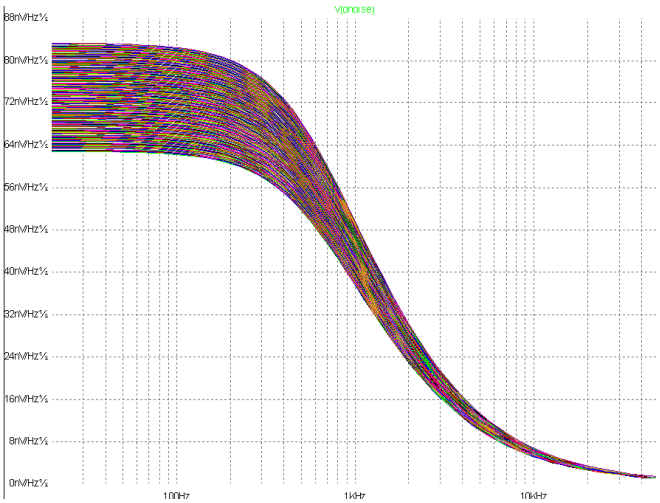

Figure 2: Output noise considering temperature variations without considering skin effect.

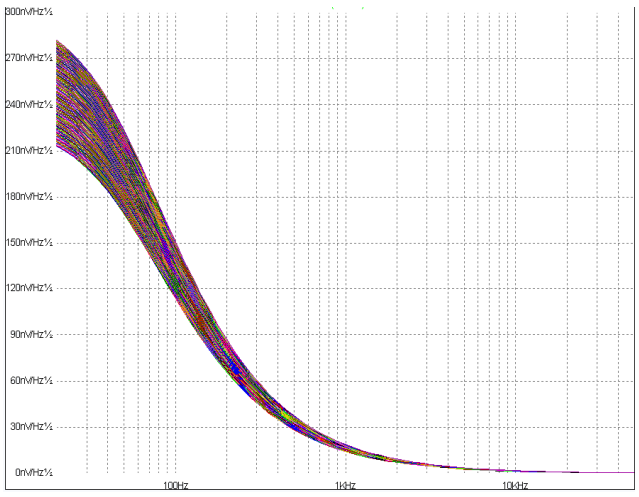

Figure 3: Output noise considering temperature variations considering skin effect.

V. SIMULATION RESULTS AND DISCUSSIONS

The motive of this paper is to make model the bandwidth and power mathematically under the influence of the skin effect under ramp input. In this paper we have successfully

model the bandwidth closed form expression as well as power under the influence of skin effect. Under the influence of the skin effect the power dissipation in the on-chip interconnects will increase with a factor of the square root of the frequency. Along with the mathematical modelling we have also proposed the simulation results for the output crosstalk noise at the output when the temperature variation is considered, It can be analyzed by the simulation result that the noise increases with increase in the temperature during the working of the interconnect. Figure 2 and figure 3 shows the noise variations with temperature.

VI. CONCLUSIONS

We proposed a new mathematical model for bandwidth calculation with and without the skin effect under ramp input response. The methodology allows arbitrary accuracy in the modelling of the skin effect, and can be adapted to different situations and modelling requirements. We propose a method for the calculation of power with and without skin effect in RLC interconnects. It is shown that skin effect can be computed efficiently in the s-domain using an algebraic formulation, instead of the improper integration in the time domain. The proposed method of computing bandwidth and power with and without skin effect relies on the poles and residues of the transfer function and can be used in any kind of model order reduction technique. Compact expressions that describe the skin effect on a single distributed RLC interconnect are rigorously derived. The derived expression along with the analysis can serve as a convenient tool for skin effect without much computation during design. In this paper, we have also proposed simulation results for the output noise obtained while considering the temperature variations. This paper reflects that during the working of the interconnect temperature increases and the noise at the output node increases.

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