



DESIGN OF RF FRONT-END LOW NOISE AMPLIFIER FOR AN ULTRA WIDEBAND RECEIVER

Pankaj Jha, Prof. V. K. Pandey, Pradip Vishwakarma
Electronics & Communication Department, NIET, Greater Noida, India, 201308.
pankaj.maahi@gmail.com

ABSTRACT

Many active academic and industrial works have been dedicated to the implementation of UWB transceivers, however, a monolithic UWB radio expanding across full 3.1–10.6 GHz UWB spectrum is yet to be accomplished. Targeting Multi-Band Orthogonal Frequency Division Multiplexing (MB-OFDM) UWB, one of the two major competing industrial UWB standards, this Paper focuses on system and circuit co-design of a fully integrated CMOS direct-conversion Low Noise Amplifier, with emphasis on architectural issue, and circuit topologies of its RF front-end.

In this paper a CMOS Ultra-wideband (UWB) Low noise Amplifier (LNA) designed and simulated. In the design, specific architecture has been selected for LNA implementation of an Ultra-wideband communication system. The basic architecture of the LNA designed herein exhibits a resistive feedback amplifier followed by single to differential amplifier with passive input and output impedance matching, reducing the number of expensive space consuming passive inductors necessary for passive impedance matching networks and also minimizing the noise figure that is generated by active input matching. The LNA maintains a gain of 15dB over the band of 3.1-10.2GHz. The LNA achieves a noise figure ranging from 1.6-1.7dB over the same band of operation.

Keywords: UWB, CMOS, LNA, GAIN

I. INTRODUCTION

One of the latest words in research and technology today is “Ultra wideband” or UWB for short. Numerous universities and companies have been trying to develop novel architectures that expand the capabilities of UWB while developing cost effective systems that take advantage of the unique features of UWB. Most of the concerns that surround the implementation of high-speed, UWB wireless technologies in a standard CMOS process are the analog front-end [1]. It is one of the most crucial stages in determining overall system performance in terms of Signal-to-Noise Ratio (S/N). We know that signal exists in

nature in analog form. There is no use of expensive DAC and ADC for analog front-end. Hence overall cost reduces by using analog front end for UWB wireless system. A lot of research has been done to develop CMOS Low Noise Amplifiers (LNA) and Mixer with exceptional performance characteristics suitable for the analog front-end of a UWB wireless system [2]. However, to the author’s knowledge, none of the CMOS ultra-wideband LNAs already developed utilizes a resistive feedback architecture followed by differential architecture that gives noise figure of 1.6 - 1.7 dB over frequency range of 3.1-10.3GHz. . One important merit of this

architecture is that it can easily integrated mixer at output of LNA due to differential architecture of mixer. Differential architectures reject large amounts of common-mode noise which would inevitably be present in a mixed-signal environment (such as in a SOC) thereby increasing the robustness of the analog circuitry and enhancing the ability of the LNA to survive in a mixed-signal environment. However, one of the drawbacks associated with differential circuits is the fact that the circuit implementation essentially doubles the usage of very costly chip die area [3]. Therefore, given the necessity of the differential architecture for the survival of the LNA in a SOC implementation, significant design measures must be taken elsewhere to curtail the increase in size associated with differential circuits compared to their single-ended counterpart. For integrated circuit design, it is a challenge to implement a UWB low noise amplifier (LNA) due to requirements of UWB communication systems. According to these requirements of UWB communication systems, LNA should provide the following:

- 1) Provide the wideband input matching network,
- 2) Good linearity, sufficient and flat gain and low noise figure,
- 3) Low power consumption and small chip area.

Conventional narrowband source inductor degeneration LNA as shown in figure 1 has been the most popular topology for LNA in RF receiver. However, it is difficult to adopt this structure for ultra wideband system because it cannot achieve input impedance matching in a band range of 3.1-10.6 GHz. [4].

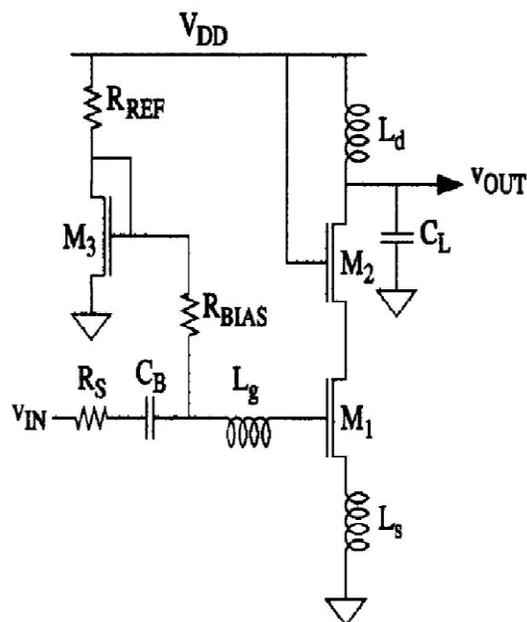


Figure1: Source Degenerated LNA

II. PROPOSED UWB LNA

This paper proposes a 3.1-10.6 GHz low noise amplifier (LNA) for ultra-wideband (UWB) applications. The proposed wideband amplifier comprises a single-ended resistor feedback LNA with wideband input matching and a single-to-differential voltage buffer which improves the power gain of the amplifier. The LNA achieves a 15.2 dB voltage gain and input return loss below -13 dB from 3.1-10.6 GHz, 1.6 dB and 1.8 dB minimum and maximum noise figure (NF), and 11.9 dBm IIP3 at 5.6 GHz. The proposed LNA is realized in $0.13 \mu\text{m}$ CMOS technology. The power consumption is 9 mW with 1.2 V supply. Here in figure 2 author is presenting the proposed LNA and the design issues associated with it.

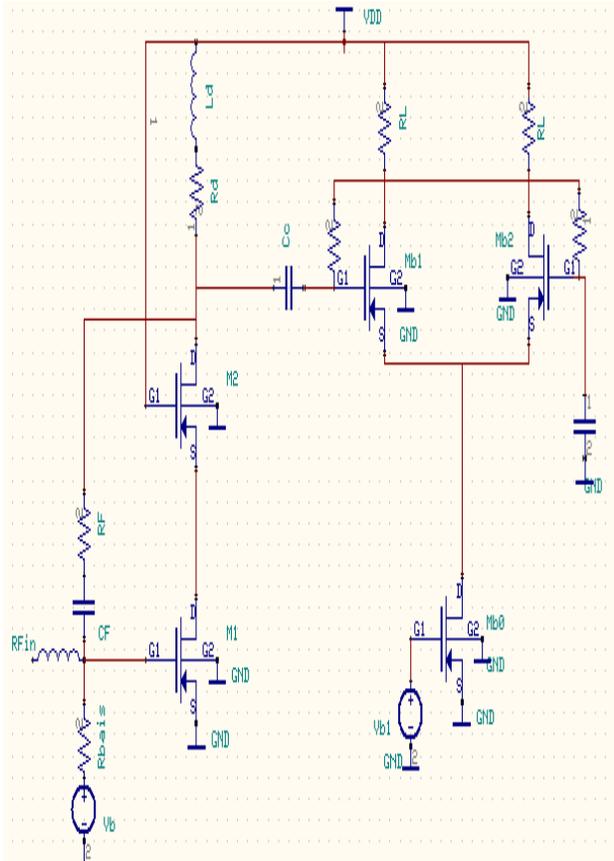


Figure 2: Proposed Schematic of LNA

III. SIMULATION AND PERFORMANCE OF LNA.

The proposed LNA is designed with 0.13 μm CMOS technology. The input port and output port are matched with 50 Ω resistances during simulation. To drive the parasitic capacitor at output pad and PCB board, a single to differential buffer is used. The complete LNA is shown in Figure 3.5. The width of $M1$ is 260 μm , $R_d = 50 \Omega$ and $L_d = 2 \text{ nH}$. In order to tune out C_{eq} , the value of inductor L_g is 600 pH. S_{11} is shown in Figure 3.8. From 3.1 GHz to 10.6 GHz, S_{11} is less than -13 dB. From equation (3.6), noise figure is 1.8 dB. The width of cascaded transistor $M2$ is 200 μm , which is smaller than $M1$ to reduce the capacitors at LNA output. The lengths of $M1$ and $M2$ are the minimal size.

III.1 INPUT MATCHING

Figure 3 (a, b) shows the input equivalent circuit of the proposed LNA. Capacitor C_{gs} is the gate source capacitor of input transistor $M1$ and R_s is the source resistor. As shown in figure 3(a), the input impedances Z_{in} is

$$Z_{in} = 1/(1/R_{in} + j\omega C_{gs}) \quad (1)$$

$$\text{Where } R_{in} = (R_F + R_d)/(1-A_0) \quad (2)$$

As illustrated in Figure 3 (b), the circuit input impedance Z_{eq} is given by

$$Z_{eq} = sL_g + R_s + 1/C_{gs} \quad (3)$$

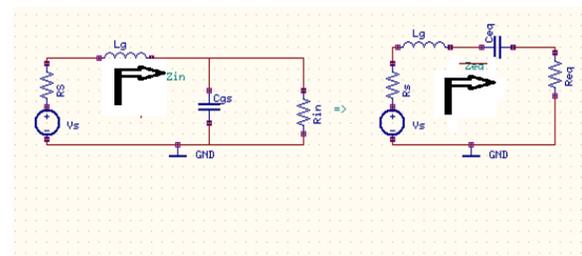


Figure3: (a, b) Input equivalent circuit of shunt resistor LNA & and its equivalent series circuit.

When inductor L_g and capacitor C_{eq} is resonance, Z_{eq} is equal to resistor R_s . Hence the input Impedance matches to the resistance of antenna [5].

As seen in Figure 4 the input reflection coefficients (S_{11}) remain below -11dB in the band of 3.5-10.5GHz.

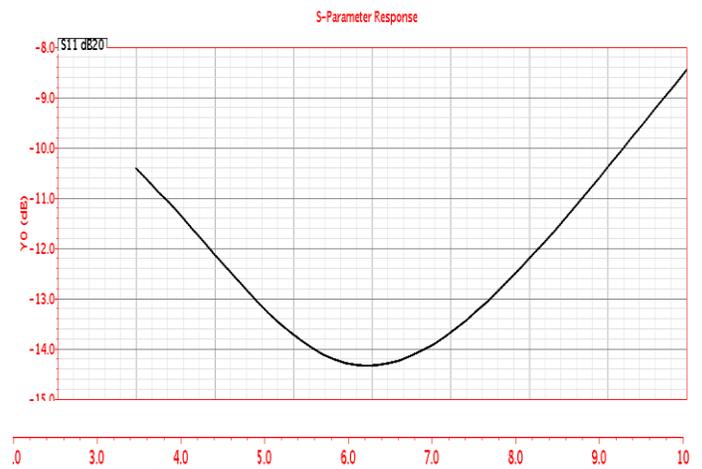


Figure 4: Input reflection coefficients (S_{11})

III.2 GAIN

Since the UWB LNA is used in a direct conversion receiver, it is the voltage gain which is important at the input of the mixer. However, S_{21} is measured as a standard figure of merit. In order to measure S_{21} , an single to differential amplifier is used after LNA such that it provides 50Ω matching to the output port as well [6]. Voltage gain of the LNA can easily be calculated by adding 6dB to S_{21} . The first stage contributes 10 dB voltage gain and the second stage 5 dB. The total maximum gain is 15 dB. However, the output buffer can attenuate 3-4 dB. One negative effect of the second stage is the introduction of noise. Figure 5 shows the gain versus frequency graph. For a receiver chain, high voltage gain of LNA can release the noise requirement of the next stage. However, in CMOS technology, it is difficult to provide enough gain. In this work, a second amplifier stage is cascaded, which also can transform single-ended input to differential outputs. This is also suitable to integrate Mixer at the output of LNA.

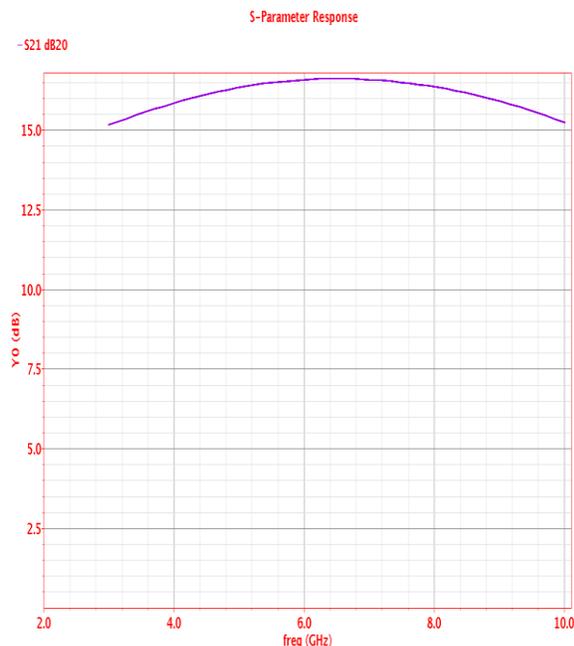


Figure.5: Gain versus Frequency graph (S_{21})

III.3 NOISE FIGURE ANALYSIS

Not including any losses associated with a pre-select filter, the budget link in the MB-OFDM proposal for IEEE 802.15.3a standard specifies that an overall noise figure for the RF receiver chain should be less than 2.9 dB [7]. Therefore, since an adequate gain of 15.4 dB was achieved, a noise figure for the LNA of less than 4dB should be adequate as well. For example, consider a subsequent stage after the LNA with a noise figure of 8 dB. The cumulative noise figure and the input of this LNA would be approximately 1.8 dB, which is still less than the needed 4 dB and given in the figure 6.

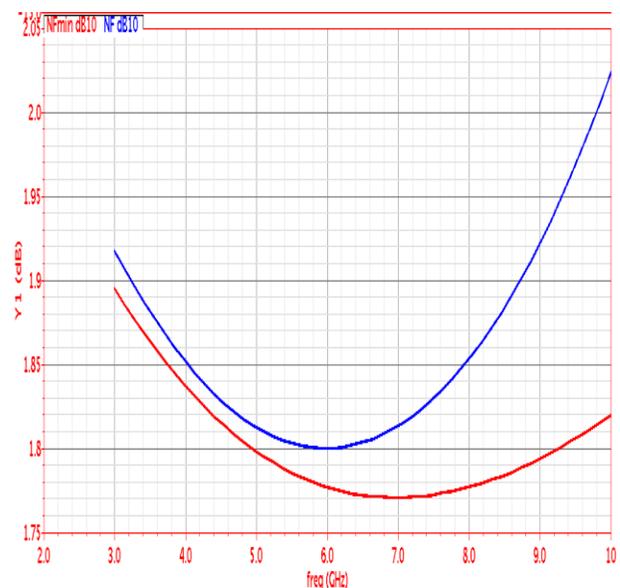


Fig.6 Noise figure of the UWB LNA

III.4 IIP3

Input referred IP3 (IIP3) is measured by applying two-tone test to the LNA input. Frequencies of the two tones should be very close to each other and can be anywhere in the pass-band [8]. However, since IIP3 does not vary a lot because of relative gain flatness, for the purpose of measurement, only mid band frequencies are chosen.[9]

Figure 7 show IIP3 measurements for capacitance load.

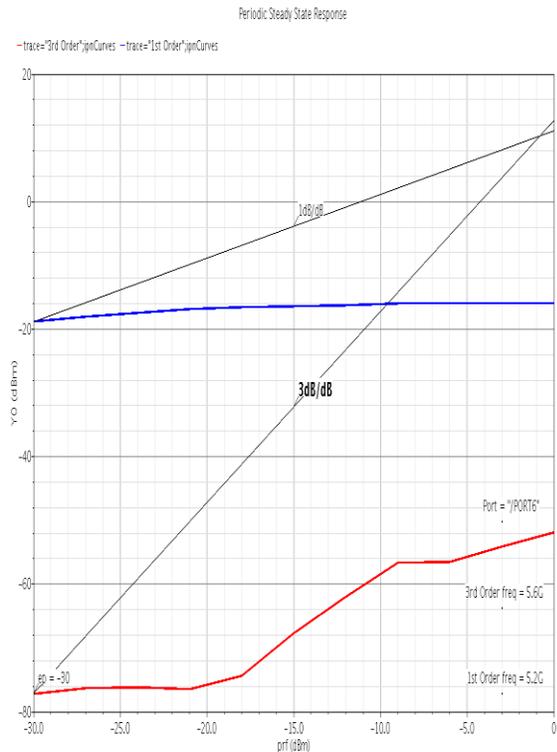


Figure 7: IIP3 with capacitance as a load

III.5 PERFORMANCE COMPARISON WITH RECENT UWB LOW NOISE AMPLIFIER.

| Design | Gain (dB) | S11 (dB) | NF (dB) | BW (GHz) |
|-------------------------------|-------------|--------------|---------------------|--------------------|
| 0.13um (Proposed work) | 16.2 | -14.6 | 1.76 to 1.96 | 3.1 to 11.5 |
| 0.18um (Ref. 2) | 10.4 | -11 | 4 to 9.2 | 2.4 to 9.4 |
| 0.18um (Ref. 3) | 9.8 | -7 | 2.3 to 5.2 | 2 to 4.6 |
| 0.18um (Ref. 4) | 9.7 | -12 | 4.5 to 5.1 | 1.2 to 11.9 |

4. CONCLUSIONS

The proposed LNA consists of two cascaded amplifier stages. The first one is a shunt resistor feedback amplifier consisting of a cascade transistor pair M1 and M2, as shown, Resistor R_F is the feedback resistor, and capacitor C_F blocks the DC voltage to the gate of M1. The bias voltage V_b provides DC bias for input transistor M1. The cascade transistor M2 improves the isolation and reduces Miller capacitance while the voltage gain of input transistor M1 should be small. Band wire inductor L_g performs a series resonant with C_{gs} of M1 for input impedance matching. To broaden -3 dB bandwidth to cover 10.6 GHz, the LNA employs a shunt peaking load constructed by resistor R_d and inductor L_d . Resistive feedback LNA architectures suited for wideband operation are investigated. Broadband input matching is achieved by using passive component [10]. New output network is proposed which results in high gain with maximum gain flatness. LNA is implemented resistive feedback circuit with bond-wire effects taken into account. The proposed work is compared with the references [2], [3] & [4] and in simulation results there is improvement in the Gain, Noise Figure, Reflection coefficient and the Bandwidth also.

APPENDIX

Component Values of LNA

| | | | |
|-------------------|-------------|-----------------------|---------------|
| $M_1(W)=390\mu m$ | $L_s=4.4nH$ | $R_{BIAS}=1.1K\Omega$ | $V_{DD}=1.2V$ |
| $M_2(W)=70\mu m$ | $L_g=10nH$ | $R_{REF}=250\Omega$ | $C_B=10pF$ |
| $M_3(W)=70\mu m$ | $L_d=4.4nH$ | $C_L=1pF$ | |

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