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IMPACT OF ASPECT RATIO ON THE LOGIC PERFORMANCE OF STRAINED $In_{0.53}Ga_{0.47}As$ METAMORPHIC HEMT

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ABSTRACT
The scaling behavior of strained $Al_{0.50}In_{0.50}As/In_{0.53}Ga_{0.47}As/Al_{0.50}In_{0.50}As$ m-HEMT is investigated using two-dimensional TCAD simulator for the perspective of logic applications. The $Al_{0.50}In_{0.50}As$ buffer incorporates 0.15% compressive strain in the device active layer. The effects of strain are also incorporated into the simulation. The device is calibrated against experimental findings of a similar device using simulation models. It is then applied to investigate the digital performance of scaled devices. Logic figure of merits (threshold voltage, sub-threshold slope, drain induced barrier lowering, and I_{ON}/I_{OFF} ratio) are extracted from the simulation. These results suggest that this device architecture and material, exhibit potential logic characteristics which can be further optimized for digital applications. Scaling results show an evident degradation in logic performance characteristics when the device aspect ratio is not standardized along with gate length scaling.
Keywords: TCAD, HEMT, logic, III-V, InGaAs, strain

I. INTRODUCTION

High Electron mobility Transistors have emerged as a potential device to explore the efficacy of III-V semiconductors for future high speed and low power digital applications. Also ITRS which had previously focused on Silicon technology has included the III-V in its technology roadmap [2]. Recently, a large number of experimental investigations of InGaAs HEMTs and related III-V materials for future logic applications have been carried out [3]. Along with such experimental investigations, numerical drift–diffusion simulation [4] has shown that InGaAs HEMTs can be ideal for future high speed, low power digital applications. These analyses have shown impressive logic ability with comparable results as that of silicon MOSFETs.

In order to reduce R&D cost and fabrication complexity, TCAD can be used as a predictive tool for engineering III-V logic prototypes and analyzing their performance for 'More Moore' applications. According to industry report, discussed in ITRS 2008, an estimated one-third reduction in cost and time can be obtained by using TCAD tools.

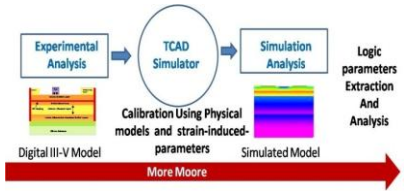


Figure 1: Approach towards digital III-V analysis

Our approach in this work is to use an existing fabricated logic compatible HEMT from literature to calibrate the III-V HEMT model in TCAD simulator and then to use the calibrated device for logic performance and device scaling analysis (figure 1).

In this approach, a systematic simulation study of the logic characteristics of a 300 nm gate length strained $Al_{0.50}In_{0.50}As/In_{0.53}Ga_{0.47}As/Al_{0.50}In_{0.50}As$ m-HEMT having a similar structure as in [5] is provided. The lattice mismatch between the channel and buffer incorporates strain in the active epilayer. The effects of strain on the electronic properties are incorporated into the simulation. Gate length and aspect ratio scaling effects have been studied that suggests the use of standardized aspect ratio for reducing short channel effects.

II. DEVICE STRUCTURE AND SIMULATION

Figure 2 presents the schematic of metamorphic $Al_{0.50}In_{0.50}As/In_{0.53}Ga_{0.47}As/Al_{0.50}In_{0.50}As$ HEMT structure similar to those reported in [5]. The channel consists of 32 nm strained $In_{0.53}Ga_{0.47}As$ layer on $Al_{0.50}In_{0.50}As$ buffer layer. The $Al_{0.50}In_{0.50}As$ barrier is delta-doped with a concentration of 5×10^{12} cm^{-2}. The barrier is placed 5 nm above the channel using $Al_{0.50}In_{0.50}As$ spacer layer to prevent scattering due to dopant atoms. The 15 nm $In_{0.53}Ga_{0.47}As$ cap layer is heavily doped at $5x10^{18}$ cm^{-3}.The spacing between the source-gate and drain-gate is 1μm.The work function of the gate material is taken as 4.8 eV. The source and drain contact resistances have been

taken as 65 Ω-μm as per experimental data. The influence of the surface charge was also considered by introducing positive defect charge on top of the recess layers.

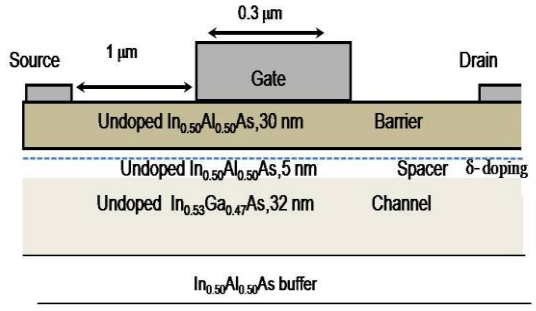


Figure 2: Schematic of 300 nm HEMT

III. CALIBRATION AND METHODOLGY

III.1. Simulated Device Calibration

Drift-Diffusion 2D physical simulations were carried out using the commercially available ATLAS/BLAZE module from SILVACO [6]. The HEMT structures are simulated using high quality triangle mesh representation and fine meshing was used in the channel and gate region for simulation accuracy.

III.2. Material Parameters and Models

The models that are utilized in simulation are concentration dependent mobility, field dependent mobility, and Shockley-Read-Hall (SRH) models. The model parameters are determined by matching the simulation results to the experimental results. The physical material parameters for the alloys were obtained from literature and Vegard's interpolation method from generally accepted values for the binary compounds.

III.3. Strain Modeling

Strain is incorporated in the active layer due to the lattice mismatch between the buffer and the channel. In the device under consideration, the lattice constants for $In_{0.53}Ga_{0.47}As$ and $Al_{0.50}In_{0.50}As$ are 0.58687 and 0.58597 nm respectively. As the epitaxial layer of $In_{0.53}Ga_{0.47}As$ grows on lattice mismatched $Al_{0.50}In_{0.50}As$ buffer, the strain energy in the layer also increases. At some critical thickness, it becomes energetically favorable to relax the strain by producing misfit dislocations. This value of film thickness is referred to as critical thickness. Here, strained $In_{0.53}Ga_{0.47}As$ thickness is 32 nm which is well below the measured critical thickness determined by Mathews and Blacklese force balance model. Figure 3(a) shows the lattice constant variation along the <100> growth direction from the middle of the gate contact. Figure3 (b) illustrates pseudomorphic growth of channel on a lattice mismatched buffer and the effect of strain creating misfit dislocations above critical layer thickness growth. Figure 3(c) shows the variation of critical thickness with different compressive strain values simulated using C-code.

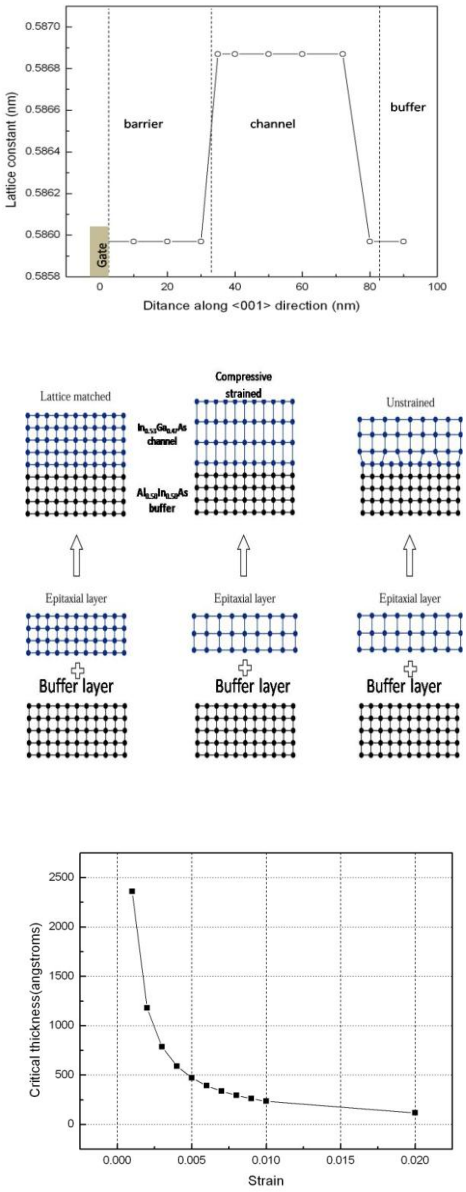


Figure 3(a): lattice constant variation along the <100> growth direction **Figure 3(b):** Schematic of strained heterolayer epitaxy **Figure 3(c):** Mathews and Blacklese critical thickness model

The mole fraction of Al in AlInAs buffer tunes the magnitude and type of strain in the $In_{0.53}Ga_{0.47}As$ channel whose value for $In_{0.53}Ga_{0.47}As$ /$In_{0.50}Al_{0.50}As$ is 0.15% and is biaxial compressive in nature. The value of uni-axial

strain is 0.0022981 which is calculated by using the parameters summarized in table 1.

The bandgap shift due to compressive strain is obtained from the following set of equations using the k.p framework. The k.p model accounts for the band splitting of light and heavy holes.

The energy correction in the conduction band induced by the strain can be described by the equation [7]:

$$\Delta E_{con} = [2a' \frac{(C_{11} - C_{12})}{C_{11}}]\varepsilon_{\|} \quad (1)$$

Here a' is the hydrostatic deformation potential for the conduction band

Table 1: Parameters for strain evaluation

Parameter	Symbol	InAs	GaAs
Elastic stiffness constant	C_{11}	8.3	11.8
Elastic stiffness constant	C_{12}	4.5	5.4
Hydrostatic deformation potential for conduction band	a	4.1	6.8
Hydrostatic deformation potential for valence band	a'	2.5	2.7
Shear deformation potential for valence band	b	−1.8	−1.7

The energy corrections in the heavy and light hole valence bands are

$$\Delta E_h = [2a \frac{(C_{11} - C_{12})}{C_{11}} + b \frac{(C_{11}+2C_{12})}{C_{11}}]\varepsilon_{\|} \quad (2)$$

$$\Delta E_l = [2a \frac{(C_{11} - C_{12})}{C_{11}} - b \frac{(C_{11}+2C_{12})}{C_{11}}]\varepsilon_{\|} \quad (3)$$

Here a and b are the hydrostatic deformation potential and shear deformation potential for the valence band, respectively. The effect of compressive strain is to reduce the electron mobility and to increase the bandgap. According to [7], the shifts in the energy bandgap of $In_{0.53}Ga_{0.47}As$ with a compressive strain of 0.15 % is +0.0094. The electron mobility is extracted from the model given by C.Kopf et.al. The band edge energies from the k.p model and mobility parameters are then fitted in the drift diffusion simulator and the poisson-schrodinger equations are solved self-consistently using Newton method as shown in figure 4.

After the models and strain induced parameters have been fitted in the simulator, the electrical characteristics of the simulated structure are compared to a similar fabricated device for efficient calibration. The comparative results are illustrated in figure 5 and figure 6. The simulated device has a maximum drain current and transconductance of 830 mA/mm and 612 ms/mm respectively measured at V_{GS}=0 V and V_{DS}=1.0 V.

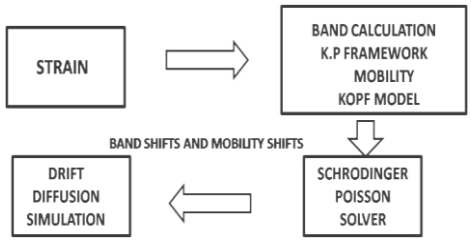


Figure 4: Simulation flow for strain modeling

III.4 Methodology for evaluating logic figure of merits

The logic parameters are evaluated by an optimized method proposed by Chau et.al and demonstrated in [3]. Table 2 below illustrates the methodology utilized in parameter extraction. V_{CC} (V_{DS}) is maintained at 0.5 V for all calculations. The sub-threshold slope (S) is determined as the inverse of the slope of log I_{DS} and V_{GS} characteristic curve at V_{CC}.

Table 2: Methodology for logic evaluation

Parameter	Unit	Methodology
V_T	V	V_{GS} for which the I_{DS} is 1 mA/mm at V_{DS} =V_{CC}
I_{ON}	mA/mm	I_{DS} (V_{GS}=V_T+2/3V_{CC}, V_{DS}=V_{CC})
I_{OFF}	mA/mm	I_{DS} (V_{GS}=V_T-1/3V_{CC}, V_{DS}=V_{CC})
DIBL	mV/V	[V_T (V_{DS}=V_{CC})-V_T V_{DS}=0.05)] / (V_{CC}-0.05).

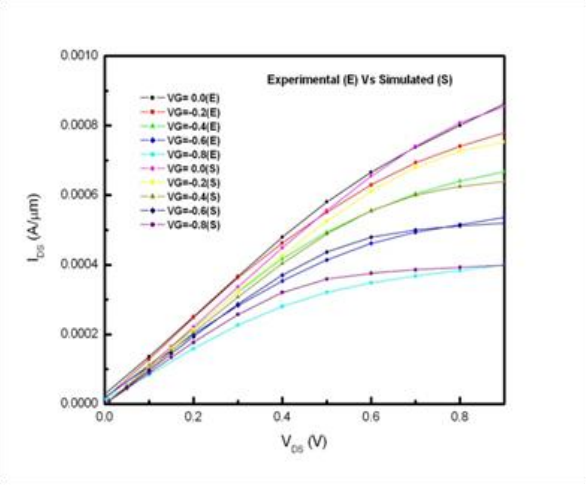


Figure 5: Comparison of output characteristics of simulated and investigational 300 nm device

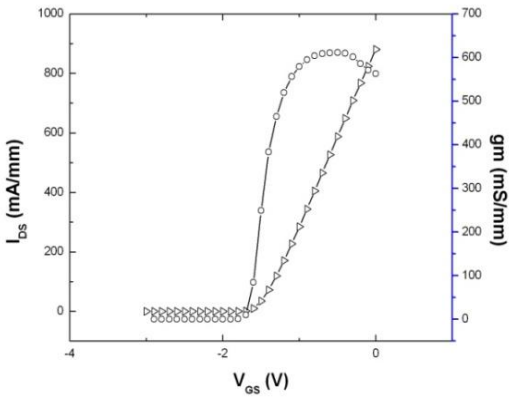


Figure 6:. Simulated transconductance and transfer characteristics for 300 nm HEMT

IV. RESULTS AND DISCUSSIONS

Three different gate length (300,200,100 nm) HEMTs have been simulated and their logic characteristics have been determined. The gate length scaling is not accompanied by the preferred barrier scaling and the affect of non-optimization of aspect ratio (A) of the device on the logic figure of merits is demonstrated. The drain characteristics of the three devices at V_{GS}=0 V is shown in figure 7.

An increase in the drain current is observed as the gate length is scaled from 300 nm to 100 nm.

The transfer characteristics for different gate length devices illustrated in figure 8 shows a prominent shift in the threshold voltages.

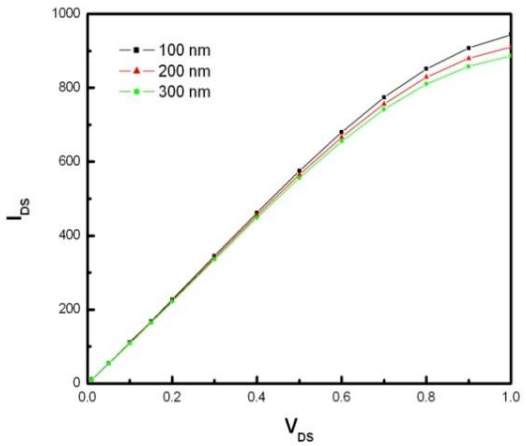


Figure 7: Comparison of drain characteristics for different gate lengths

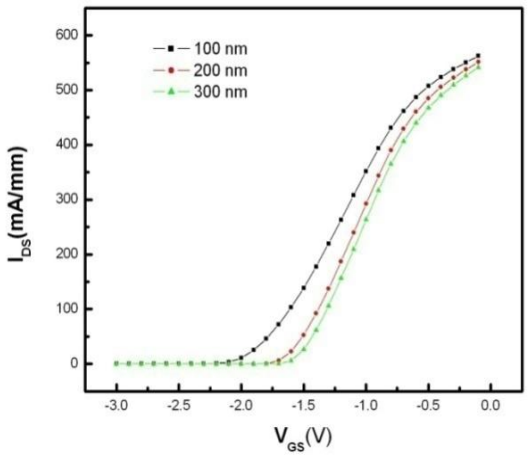


Figure 8: Comparison of transfer characteristics for different gate lengths

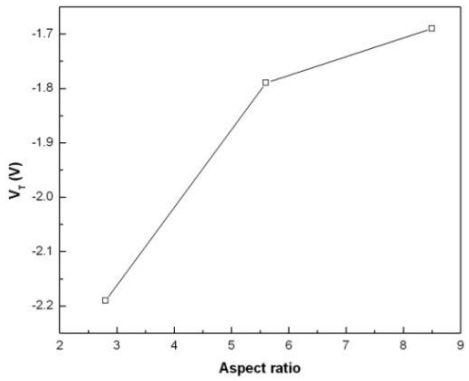
The threshold voltage shift can be attributed to short channel effects as the gate length is scaled. The short channel effects are also enhanced as the aspect ratio is not maintained at a standard value. In practice vertical scaling of the layer structure must go along with reduction of the gate length. The standard aspect ratio is governed by an aspect ratio model ($A=L_G / \lambda$) suggested by Yan et.al which is given as

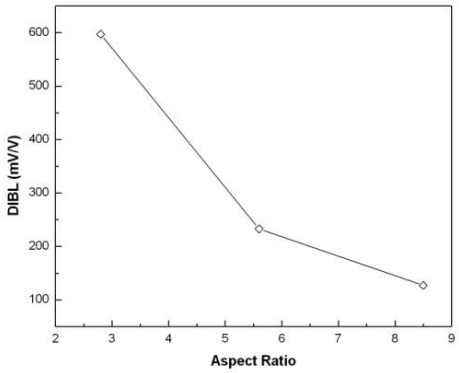
$$\lambda^2 = (t_{barrier}t_{channel})(\varepsilon_{channel} / \varepsilon_{barrier}) \quad (4)$$

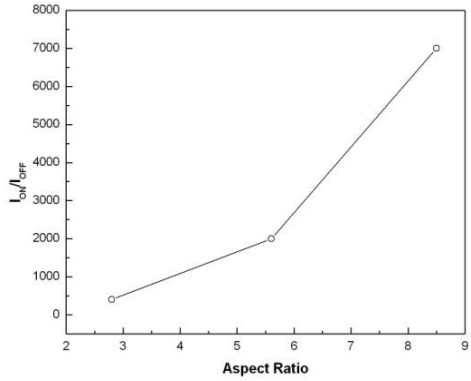
Here $t_{barrier}$ and $t_{channel}$ are the thickness of the barrier and the channel, and $\varepsilon_{channel}$ and $\varepsilon_{barrier}$ are the dielectric constant of the barrier and the channel respectively.

Using this model the aspect ratio is calculated as 8.4 for the 300 nm device which is agreeable to the value used in the simulation structure. To maintain a suitable logic performance the aspect ratio of the device should be designed at least at 5 and higher [3] [8]. The 300 nm device is therefore an optimized device and shows potential logic characteristics for next generation digital III-Vs. Figure 9 compares the V_T roll-off, I_{ON}/I_{OFF}, DIBL, and sub-threshold slope for the three devices at V_{CC}=0.5 V as a function of aspect ratio. I_{ON}/I_{OFF} ratio that determines off state leakage is higher for 300 nm device and degrades as the aspect ratio decreases. As the gate length is scaled there is degradation in the DIBL and the sub-threshold slope of the devices. The threshold voltage, DIBL and sub-threshold slope degrades severely for 100 nm device when compared to 300 nm and 200 nm devices. This is attributed to enhanced short channel effects as the device is designed with a very low aspect ratio conflicting with the standard architecture of a HEMT.

The standard value of aspect ratio for HEMT should be at least five or higher while it is only 2.8 for the 100 nm device. This results in severe short channel effects and degradation of logic performance.







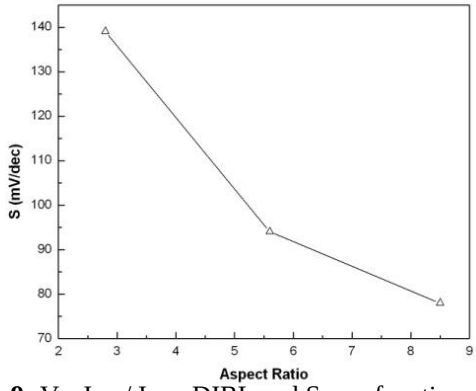


Figure 9: V_T, I_{ON} / I_{OFF}, DIBL and S as a function of aspect ratio

The simulation results of logic parameters are summarized in table 3.

Table 3: Summary of extracted parameters

L_G	A	V_T	I_{ON} /I_{OFF}	DIBL	S
nm	-	V	-	mV/V	mV/dec
300	8.5	1.69	7.0×10^3	127	78
200	5.6	1.79	2.0×10^3	233	94
100	2.8	2.19	0.4×10^3	597	139

V. CONCLUSION

We have investigated the scaling performance of strained $Al_{0.50}In_{0.50}As/In_{0.53}Ga_{0.47}As/Al_{0.50}In_{0.50}As$ HEMT. The device has been simulated by incorporating the effect of 0.15% compressive stain material parameters using SILVACO TCAD. The 300 nm device shows potential for logic applications which are attributed to the superior electronic properties of InGaAs channel and standardized aspect ratio. However as the device is scaled, an evident degradation in logic performance is observed. This is attributed to short channel effects in the channel due to poor aspect ratio of the scaled devices. The logic parameters of 100 nm device show severity in degradation as its aspect ratio is below the standard value. This highlights the significance of maintaining an optimized value of aspect ratio as gate length is reduced for digital applications.

Acknowledgement

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