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SUPPRESSION OF GATE INDUCED DRAIN LEAKAGE CURRENT (GIDL) BY GATE WORKFUNCTION ENGINEERING: ANALYSIS AND MODEL

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ABSTRACT

Leakage current reduction is of primary importance as the technology scaling trends continue towards deep sub-micrometer regime. One of the leakage mechanisms which contribute significantly to power dissipation is the Gate Induced Drain Leakage (GIDL). GIDL sets an upper limit on the VLSI MOSFET scaling and may even lead to device breakdown. Thus, in order to improve performance, static power consumption becomes a major concern in such miniaturized devices. With the CMOS technology in the nanometer regime, metal gates emerge as a powerful booster over the poly-Si gates, keeping the leakage mechanisms in control. This work presents a systematic study of the Gate Induced Drain Leakage current reduction by changing the gate workfunction. In this work, an attempt has been made to model the metal gates in the field equations in the gate-drain overlap region. The modeling has been accomplished by taking the physical property of the metals into account i.e. the workfunction. The analytical model has been used to study the impact of gate workfunction engineering on GIDL. The model includes the calculation of band bending, the resultant electric field in the gate-drain overlap region and the GIDL current. It has been observed that the electric field and the GIDL current decreases as the gate workfunction is increased continuously from 4.0~5.2 eV. Further, the results are more interesting at low applied voltages where the decrease in the current is of about 6 orders of magnitude as compared to that at higher voltages.

Key words: Band, Tunneling, Metal gate, Sub-micron, MOSFET, Workfunction, Engineering

I. INTRODUCTION

The scaling of the MOS devices in the deep sub-micrometer regime has undoubtedly increased the chip density per unit area and hence speed. But this has also aggravated the problems of Poly-Si gate depletion, boron penetration, and high gate resistance. Also the threshold voltage (V_{TH}) of novel device structures like Ultra Thin Body (UTB) and double gate devices fabricated on Silicon-On-Insulator (SOI) wafers cannot be achieved by increasing the channel doping otherwise the performance benefits of reduced short-channel effects (SCE's) offered by these thin-body devices will deteriorate [1] [2]. In order to tailor the V_{TH}, alternative approaches have to be used. One of the alternatives is that the gate material should have a tunable work function. The metal gates with wide range of workfunctions have been used for V_{TH} adjustment of these devices [3]. Further, metal gates offer many advantages over the poly-Si gates. Metal gates do not suffer from poly-Si gate depletion [4] [5]. The inversion charge density is thereby increased resulting in large drive currents. Metal gates have reduced sheet resistance, thus more suitable at deep sub-micron channel lengths. With the conventional gate oxide (SiO_2) reaching its physical limits, alternative high-k gate dielectrics with large physical thickness are being introduced to suppress gate leakage and increase the gate capacitance. Metal gates are generally more compatible with high-k gate dielectrics and also alleviate the mobility degradation problem [6]. It has been reported that the metal gates can lower the gate leakage by one to two orders of magnitude over poly-Si gated devices [7]. Further, metal gates show improved transconductance and reduced sub-threshold slope [8].

With the device technology reaching nanometer node, Low-Power design has become a major concern in digital VLSI design. This is especially important for portable and high performance devices, so the static power dissipation is of prime concern. The leakage currents predominating at deep sub-micron channel lengths need to be controlled in the miniaturized devices. One of the leakage mechanisms which contributes significantly to power dissipation in small-sized devices is the Gate Induced Drain Leakage (GIDL) [9] [10]. The GIDL is independent of channel length but as the channel length is scaled down, the contribution of GIDL to off-state leakage current becomes increasingly important because the drain dimension is not as scalable as the channel dimension.

In this paper, we have proposed the use of metal gates to control GIDL. Section II presents a brief review of the GIDL mechanism. The main aim of section II is to explain the

geometry which exists in the gate-drain overlap region and hence the field conditions. In Section III the impact of metal gates on the GIDL has been modeled. The analytical model includes the calculation of resultant electric field in the gate-drain overlap region responsible for GIDL. The model takes into account the metal gates by their corresponding workfunction. This is followed by a systematic study on how the change of metal gate workfunction affects the electric field and the GIDL current in section IV.

II. PHYSICAL PHENOMENON OF GIDL

GIDL is a band to band tunneling phenomenon and an off-state leakage current mechanism. When the drain is connected to a positive bias and the gate is in the vicinity of zero bias or to a negative bias, the n+ drain region under the gate is depleted and even inverted under the influence of vertical electric field (E_{si}) acting in the x direction as shown in figure 1. Since drain is heavily doped, the depletion region formed is narrower. This causes crowding in electric field lines [11]. The high electric field causes band bending between the Poly-Si gate and the n+ silicon drain. Physically, BTBT is characterized by electron tunneling across the silicon bandgap from the inverted drain surface into the quasi-neutral drain, as illustrated in figure 2 [12] [13]. These electrons move towards the drain as GIDL current. Valence band holes, left behind by the tunneling process, are then free to transport into the body region of the device under the influence of the lateral electric field (E_y) as shown in figure 1, giving rise to substrate related reliability issues and thus completing the path for GIDL current. Because the holes would not accumulate in the overlap region due to the lateral field acting in y direction, the overlap region would not form an inversion layer and be in deep-depletion [11] [13] [14].

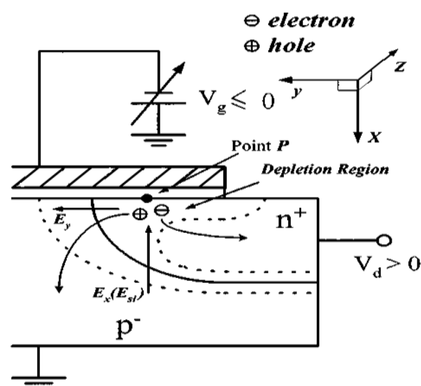

Figure 1: Cross-sectional view of the gate-drain overlap junction. region under depletion conditions.

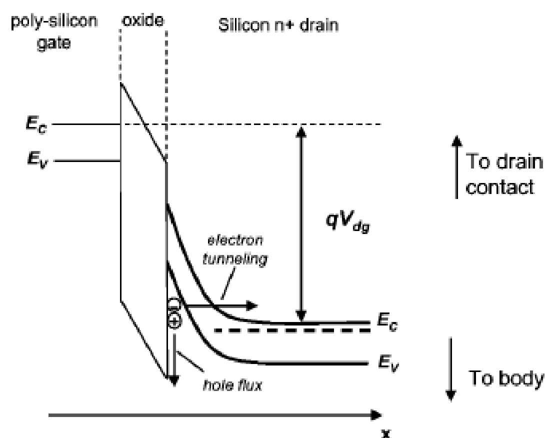

Figure 2: BTBT process across the drain-body

Under very high field conditions, the generated electrons may become hot and may get trapped in the oxide leading to oxide breakdown. The high energy electrons may easily pass through the gate oxide resulting in gate leakages [11]. This effect may be more dominant in deep sub-micron devices where oxide thickness is less than 2 A°.

GIDL is more serious in SOI MOSFET devices as it gets amplified by the lateral parasitic BJT. The holes moving out from the drain accumulate in the body activating parasitic bipolar junction transistor (pBJT) and a current of βI_{GIDL} flows to the drain terminal. The GIDL current (I_{GIDL}) is independent of channel length, whereas the current gain β of the lateral pBJT increases as the base width (channel length) decreases. This implies that in SOI MOSFET devices, the GIDL current gets amplified with channel length scaling, because of the increase in the gain of pBJT [15].

III. GATE WORKFUNCTION ENGINEERING ON GIDL: ANALYTICAL MODEL

For bulk CMOS, metal gates with workfunctions corresponding to poly-Si conduction and valence band edges of Si are desirable for n and p-MOSFET's, respectively [16]. In bulk CMOS, there also exists possibility to engineer the workfunction of metal gates to some extent around the poly-Si workfunction [17]. In this section, we present a mathematical analysis incorporating gate workfunction in the equation for GIDL current which has been neglected in the previous models [12]. A simple analysis is presented to model the dependence of electric field in the gate-drain overlap region on the gate workfunction. This section provides a description of equations and the related parameters to model the impact of using metal gates on the electric field and hence the GIDL current.

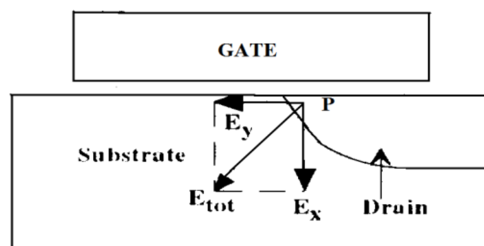

Figure 3: Resultant electric field acting at any point P in the drain depletion region.

At any point P in the drain depletion region as shown in figure 3, the total electric field acting at that point is given by the vector sum of vertical and lateral fields as already discussed in section II.

$$E_{TOTAL}^2 = E_{VERT}^2 + E_{LAT}^2 \quad \ldots (1)$$

The vertical field (E_{ox}) across oxide or E_{si} across the Si-SiO_2 interface is given by [11][12]:

$$E_{ox} = \frac{\left(V_{DG} - V_{FB} - \psi_s\right)}{T_{OX}} \quad \ldots (2)$$

Where V_{DG}= V_D-V_G i.e. the difference between drain and gate voltages, V_{FB}= (Φ_M- Φ_{si}) is the flat-band voltage, Φ_M is the gate work function, Φ_{Si} is the silicon substrate work function, T_{ox} is the thickness of gate oxide, and Ψ_S is the potential drop across the silicon for band-to-band tunneling and accounts for band-bending.

Using depletion approximation the vertical electric field E_{Si} can be expressed as [12]:

$$E_{Si} = \frac{qN_D}{\varepsilon_{Si}}\sqrt{\frac{2\varepsilon_{Si}\psi_S}{qN_D}} \quad \ldots (3)$$

where N_D is impurity doping concentration in the drain region, ε_{Si} is dielectric constant of the silicon, q is electron charge, and x is the coordinate normal to the Si-SiO_2 interface. According to the Gaussian law, the electrical displacement across the Si-SiO_2 interface must be continous [11] [12]. It can be expressed as

$$\varepsilon_{Si}E_{Si} = \varepsilon_{ox}E_{ox} = \varepsilon_{ox}\frac{V_{DG} - V_{FB} - \psi_S}{T_{ox}} \quad \ldots (4)$$

Combining equations (3) and (4) the band bending ψ_S can thus be calculated as:

$$\psi_S = V_{DG} - V_{FB} + \frac{qN_D T_{OX}^2 \varepsilon_{Si}}{\varepsilon_{OX}^2} - \sqrt{\left(\frac{qN_D T_{OX}^2 \varepsilon_{Si}}{\varepsilon_{OX}^2} + \left(V_{DG} - V_{FB}\right)\right)^2 - \left(V_{DG} - V_{FB}\right)^2} \quad \ldots (5)$$

The lateral field (E_Y) can be expressed as [11]:

$$E_{Lat} = \frac{V_{DG}}{\left(\frac{\varepsilon_{Si}}{\varepsilon_{ox}} T_{ox} h\right)^{1/2}} \quad \ldots (6)$$

where ε_{ox} is the permittivity of oxide, h is the parameter related to junction depth as $h \approx 10^{-4} r_j^{2/3} L^{2/5} / T_{ox}^{3/4}$ for T_{OX}<150A^o, r_j is the junction depth, and L is the channel length.

Using equations (2) and (6) in (1),

$$E_{TOTAL}^2 = \frac{(V_{DG} - V_{FB} - \psi_S)^2}{T_{OX}^2} + \frac{V_{DG}^2}{\frac{\varepsilon_{si}}{\varepsilon_{ox}} T_{OX} h} \qquad \text{... (7)}$$

$$E_{TOTAL}^2 = \frac{(V_{DG} - V_{FB} - \psi_S)^2}{T_{OX}^2} + \frac{V_{DG}^2}{\gamma T_{OX} h}$$

where $\gamma = \frac{\varepsilon_{si}}{\varepsilon_{ox}}$

$$E_{TOTAL} = \sqrt{\frac{\left[\frac{V_{DG}}{T_{OX}}\left(1 - \frac{V_{FB} - \psi_S}{V_{DG}}\right)^2 + \frac{V_{DG}^2}{\gamma h}\right]}{T_{OX}}} \qquad \text{... (8)}$$

Equation (8) gives the resultant electric field responsible for GIDL acting at any point in the gate-drain overlap region. The metal gate workfunction can now be incorporated in the flat-band voltage and the equation (8) can be modified as

$$E_{TOTAL} = \sqrt{\frac{\left[\frac{V_{DG}}{T_{OX}}\left(1 - \frac{\left[(\Phi_M - \Phi_{Si}) + \psi_S\right]}{V_{DG}}\right)^2 + \frac{V_{DG}^2}{\gamma h}\right]}{T_{OX}}} \qquad \text{... (9)}$$

The effect of gate workfunction engineering on the resultant electric field in the gate-drain overlap region can be analyzed from equation (9) by substituting the work function of the metal being used as gate electrode as Φ_M in above equation. It should be noted that Φ_{Si} in all the above equations refers to the Si drain workfunction. According to the tunneling theory, the GIDL current can be expressed as [18],

$$I_{GIDL} = A E_{GIDL}^2 \exp\left(\frac{-B}{E_{GIDL}}\right) \qquad \text{... (10)}$$

where E_{GIDL} is the field responsible for GIDL current, A and B are constants for indirect phonon assisted tunneling. Substituting the value for E_{GIDL} from equation (9) in equation (10), we get

$$I_{GIDL} = A\left[\frac{\frac{V_{DG}}{T_{OX}}\left(1-\frac{(\Phi_M-\Phi_{Si})-\psi_S}{V_{DG}}\right)^2+\frac{V_{DG}^2}{\gamma h}}{T_{OX}}\right]\exp\left(\frac{-B}{\sqrt{\frac{\left[\frac{V_{DG}}{T_{OX}}\left(1-\frac{(\Phi_M-\Phi_{Si})-\psi_S}{V_{DG}}\right)^2+\frac{V_{DG}^2}{\gamma h}\right]}{T_{OX}}}}\right) \quad \ldots (11)$$

Equation (11) shows that GIDL current has both a quadratic and an exponential dependence on gate workfunction. The above equation can be applied to bulk as well as SOI CMOS alike. The modeled equation can hence be used to study the impact of using metal gate electrodes with wide range of work functions on the GIDL current as presented by the modeling predictions in the next section. Equation (10) is also the model for BTBT being currently used in the ATLAS device simulator. Though it does not take into account the lateral electric field and the gate workfunction, but is enough for evaluating dependence of GIDL on various parameters as explained in section iv.

IV. GIDL SIMULATION and MODELING PREDICTIONS

The GIDL current has been simulated in the ATLAS device simulator [17]. The simulations were carried out to verify that GIDL is an off-state leakage mechanism and further its dependence on various parameters. The simulated device was nMOS with channel length of 0.1 μm, gate length of 0.12 μm, gate-drain overlap length of 0.01 μm and drain doping of 5E19 /cm^3. Figure 4 shows a plot of drain current with gate voltage for different values of V_{DS}. When the gate voltage is negative, the MOSFET is in the off-state and the drain current obtained is the off-state current. At V_{DS} =1V, BTBT occurs at much higher values of gate voltage and sub-threshold current dominates. At high values of V_{DS}=2V and 3V, the BTBT dominates the off-state current as shown in the graph. This BTBT current is the GIDL current and is dependent on the gate voltage as well as the drain voltage which justifies the parameter V_{DG} in equation (11).

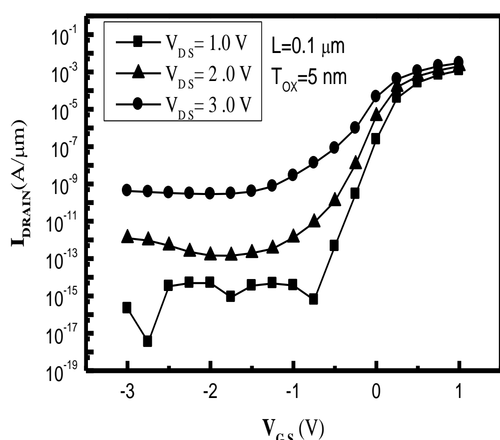

Fig. 4 Drain current (I_{DRAIN}) versus gate to source voltage source (V_{GS}) at different drain to source bias (V_{DS}).

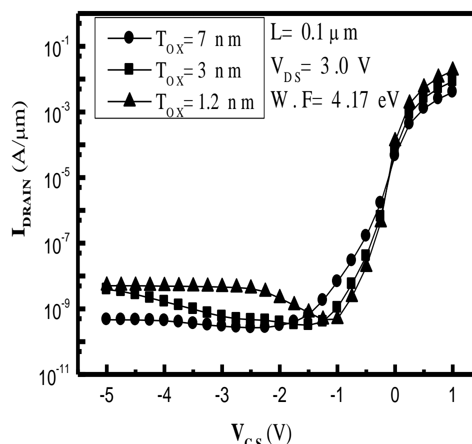

Fig. 5 Simulated drain current versus gate to voltage at different oxide thickness (T_{OX}).

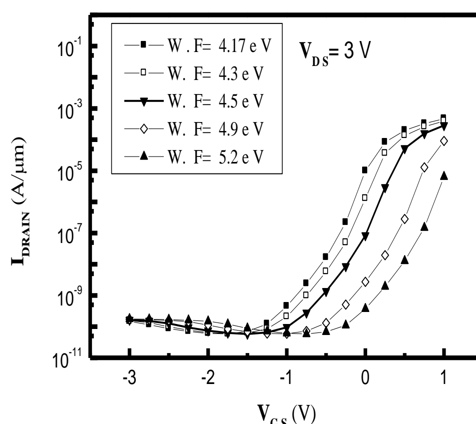

Fig. 6 Drain current (I_{DRAIN}) versus gate to source voltage at V_{DS}=3V for different gate workfunction.

The increase in the gate-drain voltage increases the electric field and hence band-to-band tunneling also increases. GIDL current also shows a dependence on T_{ox} as shown in figure 5. It is evident from figure 5 that the drain current increases by almost a magnitude as T_{ox} goes from 7 nm to 3 nm to 1.2 nm. The simulated results in figure 4 and figure 5 predict V_{DG} and T_{OX} as important parameters for GIDL variation. Further, the device simulations for GIDL show similar set of curves with different gate workfunctions as shown in figure 6. This is because the BTBT model for GIDL in ATLAS device simulator does not take into account the gate workfunction. Figure 6 shows that as V_{GS} goes more negative, the GIDL current for various workfunctions converges, i.e. the effect of the flat-band voltage is not taken into account for the GIDL current.

The dependence of GIDL on gate workfunction has been evaluated by the modeling predictions. The analytical model for the GIDL current incorporating gate workfunction presented in section III has been evaluated for nMOS with Φ_{Si}=4.17 eV i.e. the work function of n+ drain because we are concerned with the field conditions at the gate-drain overlap region and ε_{Si}=3.9, ε_{ox}=12. The results have been evaluated for value of A=4E14 $V^{-2}s^{-1}cm^{-1}$ as per Klassen's BTBT model in ATLAS and B= 44 MV/cm obtained for indirect transitions [18] [19]. Figure 7 shows the band-bending variation with gate workfunction as per equation (5). Figure 7 shows that the band bending increases with increasing drain-gate bias. At any value of V_{DG}, ψ_s decreases with the increase in gate workfunction. The graph shows the accurate values for band bending at any value of V_{DG} which can then be used in equation (9) instead of taking arbitrary value of 1.12 eV for BTBT process in earlier models. The decrease in band bending beyond silicon band gap of 1.12 eV with high workfunction gates will reduce BTBT and hence leakage. Figure 8 shows the variation of the electric field in the gate-drain overlap region with the gate workfunction. As per equation (9) E_{DG} increases with the increase in the V_{DG}. As shown in figure 8, the electric field decreases with increasing the gate workfunction. The electric field is highest at Φ_G=4.1 eV i.e. the gate workfunction for conventionally used n+ poly-Si gates. The variation of electric field with gate workfunction at different values of T_{OX} is shown in figure 9. Figure 9 shows that the electric field increases at small values of T_{OX} but shows a decrease with the increase in gate workfunction. These results have been replotted in figure 10 which shows that the decrease in electric field is more

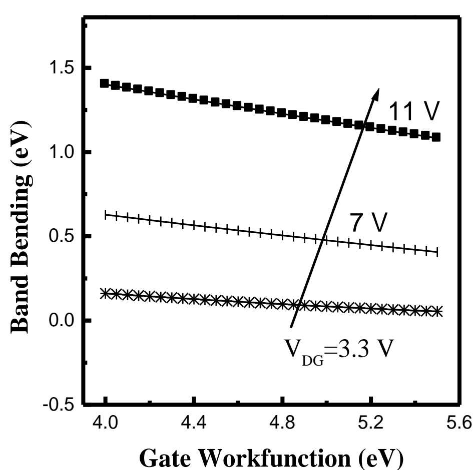

Fig. 7 Band-bending versus gate workfunction at different drain-gate voltages (V_{DG}).

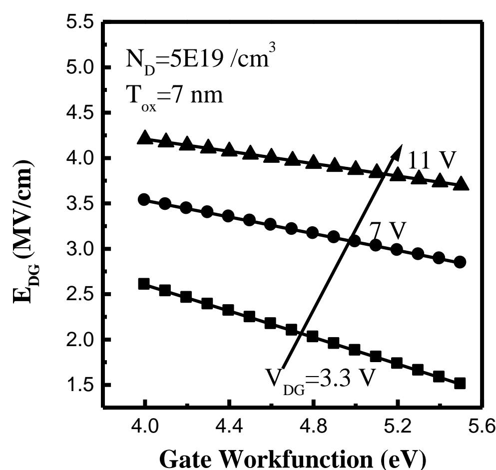

Fig. 8 Drain to gate electric field (E_{DG}) variation with gate workfunction.

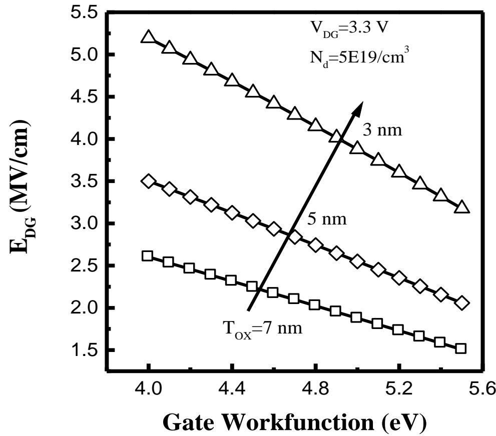

Fig. 9 Drain gate (E_{DG}) variation with Gate workfunction at different oxide thickness.

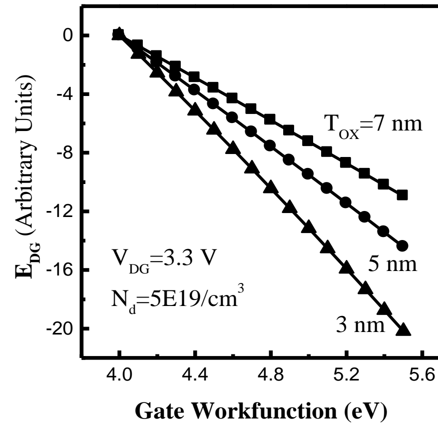

Fig. 10 Normalized electric field variation with gate workfunction at different oxide thickness.

more for T_{ox}= 3 nm as compared to T_{ox}= 5 nm and 7 nm. This result is particularly important for the deep sub-micron devices where T_{OX} is below 3 nm and the electric fields are high. The GIDL current obtained in equation (11) is plotted as a function of gate workfunction for different drain-gate voltages in figure 11. Figure 11 shows that I_{GIDL} decreases with the increase in the gate workfunction. At high drain-gate voltages, I_{GIDL} decreases by 1~2 orders of magnitude. At low values of V_{DG}, the decrease is exponential and is about 6 orders of magnitude as compared to the decrease of only 1-2 orders of magnitude at V_{DG}=7 V and V_{DG}=11 V. The result is particularly useful for low power sub-micron devices where the applied voltages are also small. I_{GIDL} is plotted as a function of gate workfunction for different T_{OX} as shown in figure 12. Figure 12 shows that I_{GIDL} increases at small values of T_{OX} because of the increase in E_{DG}. I_{GIDL} decreases by almost two magnitudes as the gate workfunction increases continuously from 4.0~5.6 eV at a particular value of T_{OX}.

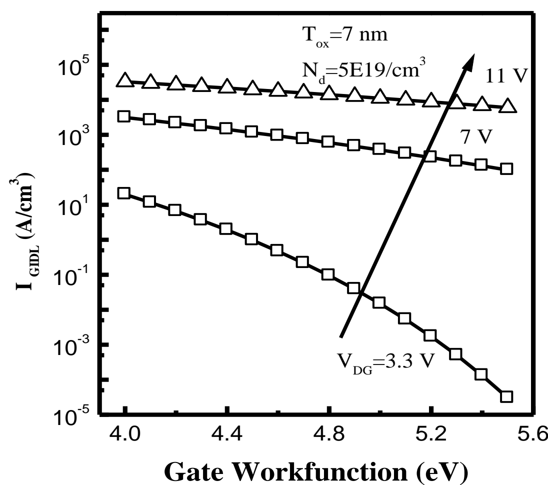

Fig. 11 GIDL current (I_{GIDL}) variation with Gate workfunction at different drain-gate voltages.

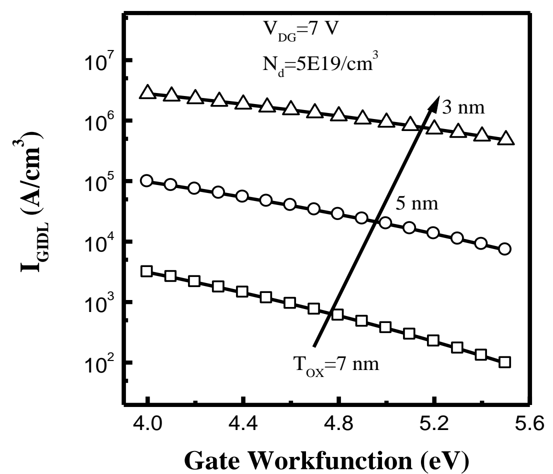

Fig. 12 Drain leakage current variation with gate workfunction for varying oxide thickness.

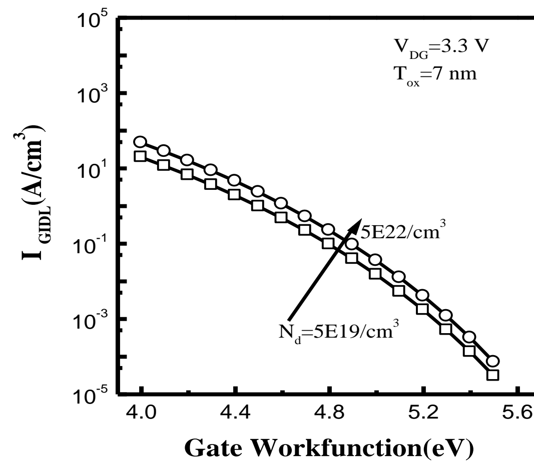

Fig. 13 GIDL current variation with Gate workfunction at different drain dopings.

The parameter N_D has an impact on the band bending only as per equation (5) and therefore I_{GIDL} curves for two different values of drain doping does not vary much from each other as shown in figure 13. The deviation may be larger for small doping values, but practically the drain doping below 1E19 /cm^3 is not used.

V. CONCLUSION

The gate workfunction engineering which is becoming an innovative advent with the deep sub-micron technology has been implemented analytically for the control of GIDL current in this paper. The results have predicted that the gate workfunction is an important parameter for the control of BTBT process and hence the GIDL current. The device simulations may show further improved results if the BTBT models incorporating gate workfunction are designed. The models incorporating gate workfunction engineering may also provide some control on the gain β of the pBJT in SOI technology. The use of high-k gate dielectric with metal gates will have higher performance results as compared to using SiO_2 gate dielectric as metals are generally more compatible with high-k gate dielectrics. The decrease in the resultant field and the GIDL current at high values of gate workfunction suggests the use of gate workfunction of 5.2 eV and higher if other methods of V_{TH} control are used. Further, the results suggest that metal gate technology may become a performance booster for deep sub-micron low power operating devices.

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